Table of Contents

High-Level Synthesis of Hardware Accelerators for Deconvolution Engines 1
Cristian Sestito, Robert Stewart, and Stefania Perri

Processing Speed Impact of the Pipeline-Length on a Custom RISC-V CPU for FPGAs 5
Julian Weihe, Timm Bostelmann, and Sergei Sawitzki

Design of Novel Integrated Data Acquisition System for Multi-Channel Sensing in Landing Gear 9
Esteve Hassan