CENICS 2011

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CENICS 2011

Foreword

The Fourth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS 2011), held between August 21-27, 2011 in Nice/Saint Laurent du Var, France, continued a series of events initiated in 2008, capturing the advances on special circuits, electronics, and micro-electronics on both theory and practice, from fabrication to applications using these special circuits and systems. The topics cover fundamentals of design and implementation, techniques for deployment in various applications, and advances in signal processing.

Innovations in special circuits, electronics and micro-electronics are the key support for a large spectrum of applications. The conference is focusing on several complementary aspects and targets the advances in each on it: signal processing and electronics for high speed processing, micro- and nano-electronics, special electronics for implantable and wearable devices, sensor related electronics focusing on low energy consumption, and special applications domains of telemedicine and ehealth, bio-systems, navigation systems, automotive systems, home-oriented electronics, bio-systems, etc. These applications led to special design and implementation techniques, reconfigurable and self-reconfigurable devices, and require particular methodologies to be integrated on already existing Internet-based communications and applications. Special care is required for particular devices intended to work directly with human body (implantable, wearable, ehealth), or in a human-close environment (telemedicine, house-oriented, navigation, automotive). The mini-size required by such devices confronted the scientists with special signal processing requirements.

We take here the opportunity to warmly thank all the members of the CENICS 2011 technical program committee as well as the numerous reviewers. The creation of such a broad and high quality conference program would not have been possible without their involvement. We also kindly thank all the authors that dedicated much of their time and efforts to contribute to the CENICS 2011. We truly believe that thanks to all these efforts, the final conference program consists of top quality contributions.

This event could also not have been a reality without the support of many individuals, organizations and sponsors. We also gratefully thank the members of the CENICS 2011 organizing committee for their help in handling the logistics and for their work that is making this professional meeting a success.

We hope the CENICS 2011 was a successful international forum for the exchange of ideas and results between academia and industry and to promote further progress in the area of circuits, electronics, and micro-electronics.

We hope Côte d'Azur provided a pleasant environment during the conference and everyone saved some time for exploring the Mediterranean Coast.

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Efficient Implementations of Radix-4 Parallel-Prefix Trees

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***Abstract*—This paper presents novel dynamic circuits purpose-designed to realize parallel-prefix adder trees with computational delay and power consumption lower than the conventional domino logic implementations. The proposed circuits increase speed by reducing the complexity of the pull-down networks of each dynamic gate; and save power by reducing the number of dynamic stages within the overall structure of the generic parallel-prefix tree. When the ST 45nm 1V CMOS technology is used, 32-bit radix-4 Brent-Kung, Han-Carlson and Ladner-Fischer trees designed as proposed here achieve, respectively, a computational delay of 148ps, 129.6ps and 117.2ps; dissipate 194fJ, 240fJ and 209fJ; and shows a silicon area requirement of 160um^2, 190um^2 and 170um^2.**

Keywords- Adders; VLSI circuits; parallel-prefix trees.

I. INTRODUCTION

Addition is the basic operation of any digital system. Therefore, the design of high-speed, low-power and area efficient binary adders always receives a great deal of attention. Among the hundreds adder architectures known in the literature, when high performances are mandatory, parallel-prefix trees are generally preferable [1-12].

Optimizing a parallel-prefix tree architecture and its transistor-level implementation for a specific design is not trivial since the designer has to choose: i) the radix-of the carry tree (i.e. the number of carries grouped in each step of the computation); ii) the tree architecture; iii) the logic style. As is well known, all these choices are crucial for both speed and power. In fact, higher radices determine a lower number of stages needed in the tree to compute the output carry signals, but they require more complex gates. Furthermore, at a given radix *r*, dense architectures, such as the Kogge-Stone tree [13], reach the minimum logic depth, but they require a large number of gates and consume a large amount of power. On the contrary, sparse trees, like the Brent-Kung [14], the Han-Carlson [15] and the Ladner-Fischer [16], do not assure obtaining the minimum logic depth, but they save hardware resources and power. Last but not least, logic style significantly affects delay and energy. As shown in [5-7, 12], parallel-prefix trees realized using dynamic domino logic achieve higher speed performances at the expense of consumed energy; whereas, using static logics lowers power consumption, but sacrifices computational speed.

This paper proposes a novel approach to optimize the implementation of the basic logic modules, namely the preprocessing stage and the associative dot operator, typically used within parallel-prefix adders. The basic idea exploited in the proposed designs consists of: 1) increasing speed by reducing the complexity of the pull-down networks (PDNs) of each dynamic gate; and 2) saving power by reducing the number of dynamic stages within the overall structure of the generic parallel-prefix tree.

Further advantages are taken by using the compound domino logic (CDL) [17]. The latter was used as an efficient alternative to the purely dynamic and static logic design styles also in [1], [5], [6], and [12]. The CDL replaces the inverter stages used in common domino circuits to invert the precharged nodes with more complex inverting static CMOS gates.

Purpose-designed CDL gates are proposed to realize efficient radix-4 parallel-prefix adder trees. Gates designed with the approach proposed here are implemented using the ST 45nm 1V CMOS technology.

The novel circuits were used to implement 32-bit parallel-prefix trees based on the Brent-Kung, Han-Carlson and Ladner-Fischer architectures. Comparison with conventional domino counterparts demonstrate that, due to the innovations introduced, up to ~40% lower computational delay is achieved with up to ~44.7% lower energy consumption and up to ~44.8% lower silicon area requirement.

The paper is organized as follows: in Section 2, a brief background on the parallel-prefix adder trees is provided and conventional domino gates implementations are also shown; the novel circuits are then described in Section 3 where comparison results are also presented and discussed; finally, conclusions are drawn.

II. BACKGROUND

Let us consider two *n*-bit addends $A = a_{n-1} \dots a_0$ and $B = b_{n-1} \dots b_0$. A parallel-prefix adder computes the sum $S = A + B = s_{n-1} \dots s_0$ through the following three steps: i) the preprocessing stage computes the auxiliary signals propagate and generate; ii) the carry propagation stage groups the propagate and generate signals *r* by *r*, with *r* being the radix of the adder; iii) the produced carries are then used by the final stage to calculate the sum bit s_i, with $i=n-1,\dots,0$.

In Fig.1, examples of 32-bit radix-4 parallel-prefix trees are depicted. By observing these examples and others numerous trees known in the literature, it can be easily seen that the basic modules needed to design a parallel-prefix tree are those indicated as Group1, Group2, Group3 and Group4.

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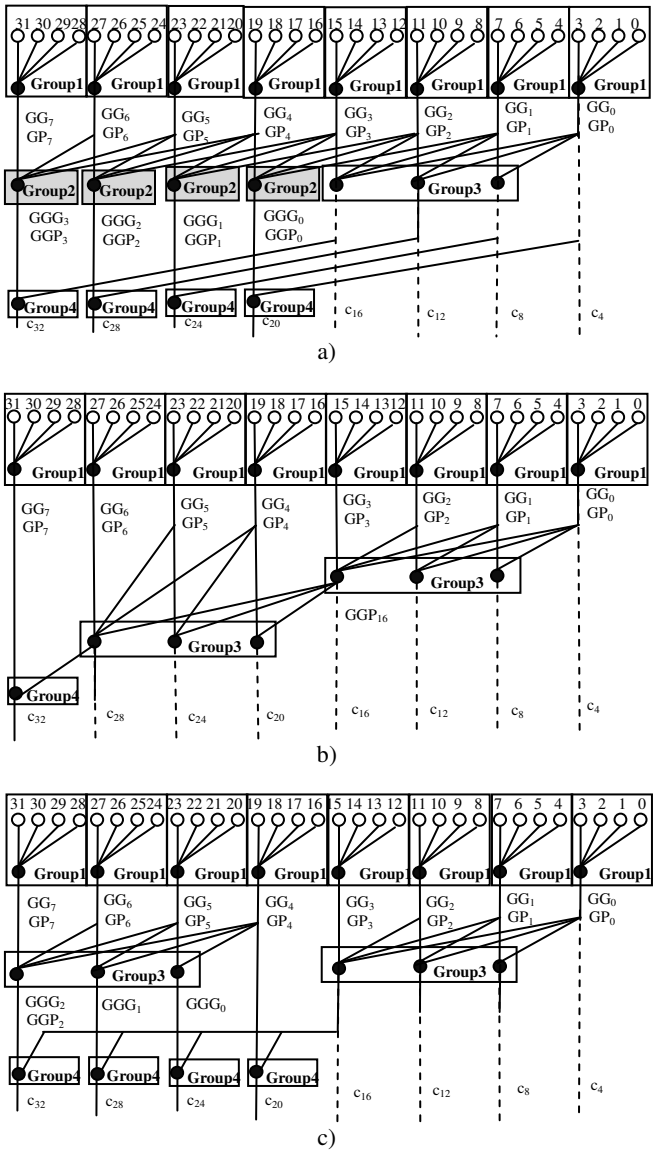

Figure 1. Examples of parallel prefix adders: (a) Han-Carlson; (b) Brent-Kung; (c) Ladner-Fischer.

Their conventional domino logic implementations are shown in Fig.2 that also reports transistor widths referred to the ST 45nm 1V CMOS technology. They were obtained considering that 0.12um is the minimum transistor width allowed by the technology used. The minimum size criterion was applied to the elementary 2-input OR and AND gates that are not shown in the Figure, whereas the progressive transistor sizing with a 1.5 tapering factor was exploited within the Manchester carry-chains and gates with higher fan-in. All the inverters on the dynamic nodes are minimum sized with an aspect ratio of 4/3.

The module Group1 of Fig.2a preliminary computes propagate and generate signals at the *i*-th bit position as shown in (1), where *i=0,..., n-1*.

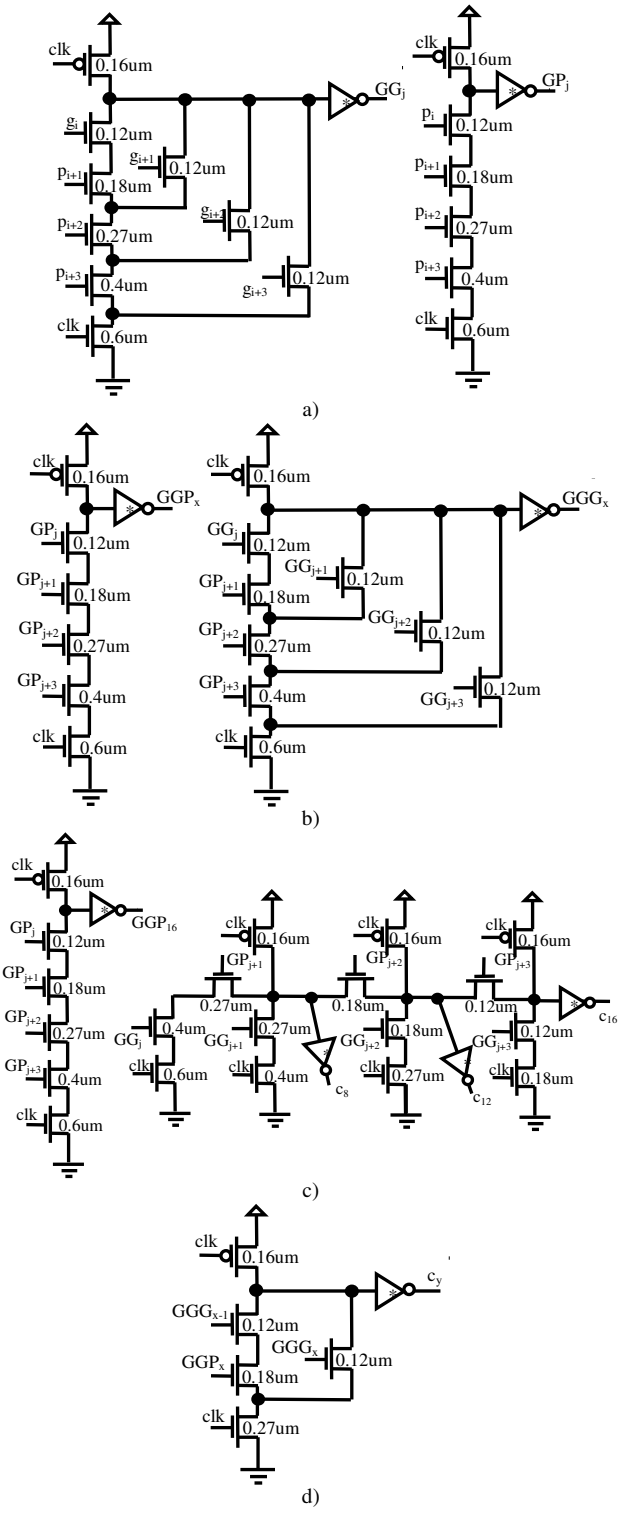

Figure 2. Conventional implementations of the modules: (a) Group1; (b) Group2; (c) Group3; (d) Group4.

$$p_i = a_i + b_i$$
$$g_i = a_i \cdot b_i \qquad (1)$$

Propagate and generate signals are then grouped four by four implementing the classical carry-look-ahead equations reported in (2), where $j = \frac{i}{4}$, and $j=0,...,7$.

$$\begin{aligned} GP_j &= p_{i+3} \cdot p_{i+2} \cdot p_{i+1} \cdot p_i \\ GG_j &= g_{i+3} + p_{i+3} \cdot g_{i+2} + p_{i+3} \cdot p_{i+2} \cdot g_{i+1} + \\ &+ p_{i+3} \cdot p_{i+2} \cdot p_{i+1} \cdot g_i \end{aligned} \quad (2)$$

The module Group2 is used to implement equations (3), where $x=j-1$, and $x=0,...,3$ for the tree in Fig.1a.

$$\begin{aligned} GGP_x &= GP_{j+3} \cdot GP_{j+2} \cdot GP_{j+1} \cdot GP_j \\ GGG_x &= GG_{j+3} + GP_{j+3} \cdot GG_{j+2} + \\ & GP_{j+3} \cdot GP_{j+2} \cdot GG_{j+1} + GP_{j+3} \cdot GP_{j+2} \cdot GP_{j+1} \cdot GG_j \end{aligned} \quad (3)$$

For all the referred tree architectures, the carry signals c_8, c_{12} and c_{16} are computed by the module Group3 that, as illustrated in Fig.2c, also provides the grouped propagate signal GGP_{16}. The same module is used in the Ladner-Fischer sparse tree of Fig.1c also to compute the grouped generate signals GGG_2, GGG_1, GGG_0 and the grouped propagate signal GGP_2, and in the Brent-Kung architecture of Fig.1b to compute the carry signals c_{20}, c_{24} and c_{28}.

Some of the final carries of the referred 32-bit trees are computed further grouping the signals GGG_x and GGP_x two by two following the classical carry-look-ahead logic shown in (4) and implemented by the module Group4 depicted in Fig.2d.

$$c_y = GGG_x + GGP_x \cdot GGG_{x-1} \quad (4)$$

Equations (1)-(3) are specialized for 32-bit radix-4 trees. However, they can be easily extended to different wordlengths and radices.

III. THE NOVEL CIRCUITS

This Section proposes novel transistor-level implementations of the basic modules used within parallel-prefix trees. The novel circuits are purpose-designed to increase speed performance and to reduce energy consumption with respect to their conventional domino logic counterparts. The main innovations here introduced consist in: i) reducing the number of dynamic nodes within each module with the objective of reducing the power consumption and ii) simplifying the pull-down networks (PDNs) of each dynamic stage to reduce the computational delay.

The number of dynamic nodes within each module is reduced mainly by avoiding the computation of useless intermediate signals. To better explain how this is possible let us examine the module Group1 implemented with the conventional domino logic as illustrated above in Fig.2a. It is easy to verify that the computation of the generic GG_j and GP_j signals involves ten dynamic nodes: four belong to the 2-input OR gates computing the propagate signals p_i, p_{i+1}, p_{i+2} and p_{i+3}; further four dynamic nodes belong to the 2-input AND gates producing the generate signals g_i, g_{i+1}, g_{i+2} and g_{i+3}; finally, two dynamic nodes are used within the gates required to group 4 by 4 the propagate and generate signals.

The novel module Group1_new was designed to produce only one propagate and one generate signal by each two bit positions. As visible from the transistor-level implementation illustrated in Fig.3, in this way only two propagate intermediate signals, $\overline{P_{32\_J}}$ and $\overline{P_{10\_J}}$, and two generate intermediate signals, $\overline{G_{32\_J}}$ and $\overline{G_{10\_J}}$, are required, thus reducing the overall number of dynamic nodes involved in the computation of the signals GG_j and GP_j to four. It can be observed that, in order to simplify the PDNs of dynamic stages, the CDL style is exploited and static CMOS inverters used in conventional dynamic circuits to achieve the domino behavior are replaced with more complex static CMOS gates.

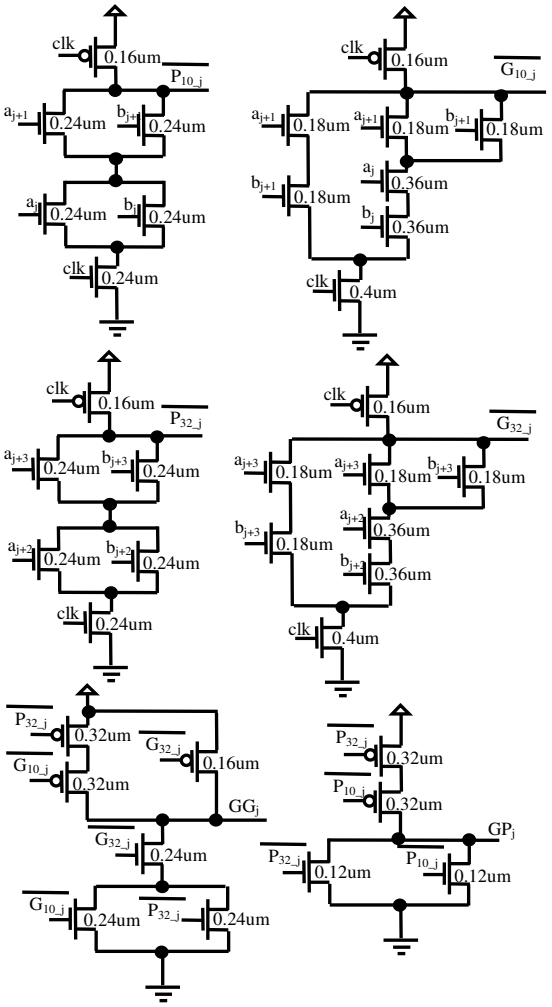

Figure 3. The Group1_new module.

The basic gates used in the novel modules Group2_new and Group3_new are illustrated in Fig.4. There, GGG_x and GGP_x correspond to c_{16} and GGP_{16} in Group3_new. The latter also uses the gates enclosed in the dashed box to compute the carry signals c_8 and c_{12}. The approach used to design these gates does not reduce the number of dynamic nodes with respect to the conventional implementations, but it allows the PDNs of dynamic stages to be simplified. In fact, from Fig.4 it can be seen that the PDNs of dynamic stages inside the modules Group2_new and Group3_new contain no more than three series transistors, whereas the conventional modules Group2 and Group3 of Figs.2b and 2c use PDNs with up to five series transistors.

Due to its simplicity, for the module Group4 depicted in Fig.2d a CDL implementation does not make sense.

Finally, it is worth emphasizing that the transistors of the novel circuits are sized ensuring that the input capacitances of a parallel-prefix tree designed as proposed here are mainly unchanged with respect to the conventional implementation. In this way, front-end modules providing the operands *A* and *B*, are not influenced by the adopted innovations.

A. *Parallel-prefix trees implementation and comparison results*

The novel modules described above were exploited to realize the 32-bit radix-4 architectures depicted in Fig.1. In the following, the Han-Carlson, Brent-Kung and Ladner-Fischer trees realized using the novel modules are named HC_new, BK_new and LF_new, respectively.

For purposes of comparison, conventional domino logic implementations of the referenced trees (in the following named HC_conv, BK_conv and LF_conv) were also carried out and they were compared to the novel implementations in terms of worst-case delay T_W and energy consumption. Pre-layout Corner Analysis was performed loading each carry output signal with a 1fF capacitance. The latter was chosen referring to the input capacitance of a positive edge-triggered D flip-flop with 9x drive strength available within the standard cells library of the used 45nm technology.

TABLE I. PRE-LAYOUT SIMULATION RESULTS

Tree	T_W [ps]			Energy [pJ]		
	TT	FF	SS	TT	FF	SS
HC_conv	126.4	100.3	158.5	0.296	0.332	0.282
HC_new	115	89.7	145.7	0.214	0.255	0.192
BK_conv	179	142.1	225	0.262	0.295	0.249
BK_new	134.6	104.6	170.8	0.185	0.223	0.165
LF_conv	129	101.8	161.4	0.27	0.303	0.257
LF_new	103.3	80.2	130.9	0.193	0.231	0.173

TABLE II. POST-LAYOUT SIMULATION RESULTS

Tree	T_W [ps]			Energy [pJ]			Area
	TT	FF	SS	TT	FF	SS	[um^2]
HC_conv	175.7	138.3	223.8	0.392	0.416	0.381	320
HC_new	129.6	101	164	0.24	0.29	0.231	190
BK_conv	248	196.6	313.5	0.351	0.373	0.341	290
BK_new	148	115	188.5	0.194	0.221	0.186	160
LF_conv	175.4	139.2	222.3	0.36	0.383	0.351	306
LF_new	117.2	91.5	148.5	0.209	0.248	0.2	170

Simulation results reported in Table I demonstrate that, for all the examined trees, the novel circuits lead to consistent speed improvement and energy reduction.

All the above compared parallel-prefix trees were laid out using the full-custom layout approach. Results obtained through the post-layout Corner Analysis are reported in Table II, which demonstrates how the advantages introduced by the novel circuits are maintained also in the laid out trees. As an example, the BK_new tree exhibits computational delay, energy consumption and silicon area occupancy ~40%, ~44.7% and ~44.8% lower than the conventional domino implementation BK_conv. Similar improvements are achieved also for the Han-Carlson and Ladner-Fischer parallel-prefix trees, thus demonstrating that the proposed circuits are advantageous in several parallel-prefix architectures.

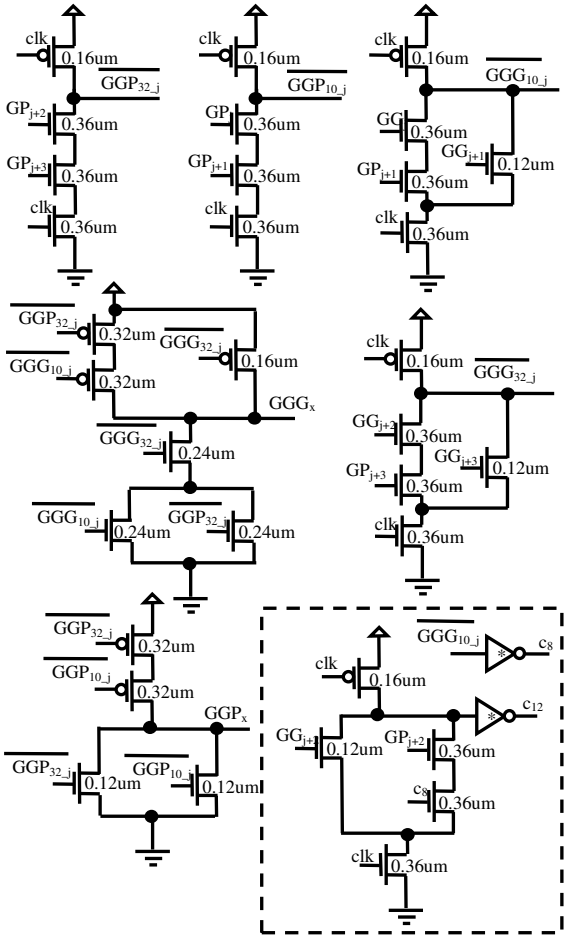

Figure 4. The novel modules Group2_new and Group3_new.

IV. CONCLUSIONS

A novel design approach was presented to implement efficient sparse parallel-prefix adder trees using nanometer technologies. The basic idea exploited in the proposed designs consists of: 1) reducing the complexity of the pull-down networks (PDNs) of each dynamic gate; and 2) minimizing the number of dynamic nodes within the overall structure of the generic parallel-prefix tree. The innovations

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here introduced allow reducing both the computational time and the average power consumption with respect to conventional domino logic implementations.

As an example, a 32-bit radix-4 Brent-Kung tree designed as proposed here achieves a computational delay of only 148ps, dissipates just 194fJ and occupies a 160um^2 silicon area, that are ~40%, ~44.7% and ~44.8% lower than the conventional domino implementation.

REFERENCES

[1] J.Park, H.C.Ngo, J.A.Silberman, S.H.Dhong, "470ps 64bit Parallel Binary Adder", *Proc. IEEE Symposium on VLSI Circuits*, June 2000, Honolulu, Hawaii, pp.192-193.

[2] P.Corsonello, S.Perri, M.Margala, "Efficient Addition Circuits for Modular Design of Processors-in-Memory", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol.52, n°8, pp.1557-1567, 2005.

[3] F.Frustaci, M.Lanuzza, P.Zicari, S.Perri, P.Corsonello, "Designing High-Speed Adders in Power-Constrained Environments", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol.56, n°2, pp.172-176, 2009.

[4] S.Das, S.P.Khatri, "A Novel Hybrid Parallel-Prefix Adder Architecture With Efficient Timing-Area Characteristic", *IEEE Transactions on VLSI Systems*, Vol.16, n°3, pp.326-331, 2008.

[5] V.G.Oklobdzija, B.R.Zeydel, H.Q.Dao, S.Mathew, R.Krishnamurthy, "Comparison of High-Performance VLSI Adders in the Energy-Delay Space", *IEEE Transactions on VLSI Systems*, Vol.13, n°6, pp.754-758, 2005.

[6] R.Zlatanovici, S.Kao, B.Nikolic, "Energy-Delay Optimization of 64-bit Carry-Lookahead Adders with a 240ps 90nm CMOS Design Example", *IEEE Journal of Solid-State Circuits*, Vol.44, n°2, pp.569-583, 2009.

[7] J.Grad, J.E.Stine, "Low Power Binary Addition Using Carry Increment Adders", *Proc. of the IEEE International Symposium on Circuits and Systems*, May 2006, Island of Kos, Greece, pp.17-20.

[8] G.Dimitrakopoulos, D.Nikolos, "High-Speed Parallel-Prefix VLSI Ling Adders", *IEEE Transactions on Computers*, vol.54, n°2, pp.225-231,2005.

[9] F.Liu, F.F.Forouzandeh, O.A.Mohamed, G.Chen, X.Song, Q.Tan, "A Comparative Study of Parallel Prefix Adders in FPGA Implementation of EAC", *Proc. of the EUROMICRO Conference on Digital System Design, Architetcures, Methods and Tools*, August 2009, Patras, Greece, pp.281-286.

[10] S.Das, S.P.Khatri, "A Novel Hybrid Paralle-Prefix Adder Architecture With Efficient Timing-Area Characteristic", *IEEE Transactions on VLSI Systems*, vol.16, n°3, pp.326-331, 2008.

[11] S.Ghosh, K.Roy, "Novel Low Overhead Post-Silicon Self-Correction Technique for Parallel Prefix Adders Using Selective Redundancy and Adaptive Clocking", *IEEE Transactions on VLSI Systems,* Forthcoming.

[12] B.R.Zeydel, D.Baran, V.G.Oklobdzija, "Energy-Efficient Design Methodologies: High-Performance VLSI Adders", *IEEE Journal of Solid-State Circuits*, vol.45, n°6, pp.1220-1233, 2010.

[13] P.M.Kogge, H.S.Stone, "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", *IEEE Transactions on Computers*, Vol.C-22, n°8, pp.786-793, 1973.

[14] R.P.Brent, H.T.Kung, "A regular layout for parallel adders", *IEEE Transactions on Computers*, vol.C-31, n°3, pp.260-264, 1982.

[15] T.Han, D.A.Carlson, "Fast area-efficient VLSI adders", *Proc. IEEE Symposium on Computer Arithmetic*, May 1987, Como, Italy, pp.49-56.

[16] R.E.Ladner, M.J.Fischer, "Parallel Prefix Computation", *Journal of the ACM*, Vol.27, n°4, pp.831-838, 1980.

[17] K.Bernstein, K.M.Carrig, C.M.Durham, P.R.Hansen, D. Hogenmiller, E.J.Nowak, N.R.Rohrer, *High-Speed CMOS Design Styles*, Kluwer Academic, 1998.

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Design and Analysis of a Dual Loop CDR using Maneatis Delay Cell VCO

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Abstract — **Clock and Data Recovery (CDR) circuits have been used extensively in the receivers of optical communication systems, and a variety of applications of inter and intra chip communications. The primary design/performance metrics of CDR circuits are clock jitter, lock range, acquisition time, power consumption, silicon area, and noise immunity. The main source of jitter is the power supply noise. The present paper investigates the effects of power supply noise on the jitter performance of the well known dual loop architecture of CDR system. In order to improve the jitter performance of the dual loop CDR system, the VCO alone is replaced by the self-biased Maneatis VCO which is well known for its immunity to power supply noise and process variations. The Maneatis VCO is widely used for microprocessors PLL systems but it is rarely used in CDR systems. The combination of the dual loop architecture and self-biased Maneatis VCO together provides the benefits of both schemes.**

Simulations were then carried out systematically to determine the capability of the proposed CDR circuit to tolerate power supply noise. The results presented in this paper show that while the conventional dual loop architecture cannot tolerate more than 20mV@10MHz noise on power supply terminal, the proposed CDR architecture can tolerate up to 200mV@10MHz noise on the power supply without degradations in jitter performance.

Keywords- CDR, PLL, VCO, Jitter, Power Supply Noise.

I. INTRODUCTION

During the past few decades, the CDR circuits have played an important role in a wide range of applications such as Gigabit Passive Optical Network (GPON), Gigabit Ethernet Passive Optical Network (GEPON), Synchronous Optical Network (SONET), optical transmission receiver, chip-chip interconnections, DDR, System on Chip (SOC), serial link communications, and PCI. The CDR circuits are normally used to extract the clock embedded in the received data and used to re-time and re-sample the received (distorted) data for further synchronous processing.

The most important metric of CDR system performance is the jitter on the recovered clock, and it represents the deviations of the clock transitions from the ideal one. The state of the art CDR circuit architectures, and the trade-offs and techniques for reducing the jitter are discussed in recent tutorials [3]-[6]. Of late, with the increased integration of analog and digital functions on the same chip, immunity to power supply noise has emerged as a very important design constraint. Several studies on the mitigation of power supply noise on PLLs have been reported in [7]-[10]. In addition to using differential topologies, some of these studies suggest the use of regulators as common techniques used to mitigate the power supply noise. The design of PLLs considering immunity to power supply noise as a design constraint is presented in [9] and considers variants of the Maneatis VCO [11, 12] in the context of PLLs and their sensitivities to power supply noise. A fast Matlab simulation procedure for evaluating the impact of power supply noise on CDR system has been described in [10].

Very few studies on the mitigation of power supply noise for CDRs have been reported in the literature. The present work addresses this particular aspect of CDR circuits, specifically in the context of dual loop delay interpolating architectures. Although there are many architectural choices, the dual loop delay interpolating CDR described in [1]-[3] is chosen for the present study since this is considered as one of the important architectures for realizing CDR circuits with a wide operating frequency range while at the same time providing low jitter.

The symmetric load, self-biased Maneatis VCO proposed by [11, 12], is well known for its ability to mitigate power supply noise and for this reason and is widely used in many of the state of the art of microprocessor PLLs. The present study investigates the possibilities of using this VCO in CDR circuits. It was observed that the Maneatis VCO as proposed in [11, 12] could not be used as such in the original dual loop CDR architecture since the former had only one control voltage input while the latter required a VCO with a coarse as well as fine control voltage inputs. Hence, in the present study, the bias generator of the self-biased Maneatis VCO from [11, 12] was suitably modified and then was incorporated into the CDR circuit. It is demonstrated in this paper that the modified Maneatis VCO is capable of providing improved performance with respect to power supply noise. Specifically, simulation results show that the proposed scheme tolerates up to seven times the power supply noise than in the conventional dual loop CDR for similar jitter performance.

The present paper is organized as follows. Section 2 presents a brief description and design details of the well-known dual loop delay interpolation CDR. Section 3 discusses the proposed modification of the Maneatis VCO for incorporation into the dual loop CDR design. Section 4 gives the simulation results of noise performance for the delay interpolation dual loop CDR as well as for the proposed modified Maneatis dual loop CDR and in Section 5, the conclusions are presented.

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II. THE DUAL LOOP CDR SYSTEM DESIGN

The block diagram of the dual loop delay interpolating CDR is shown in Fig. 1 and is the same as the one presented in [1, 2]. This system will be considered as a reference system against which the performance of the proposed modifications will be compared. The system shown in Fig. 1 consists of a coarse FLL and a fine PLL which operate together on the input data sequence and recover the clock which could be subsequently used for retiming the data.

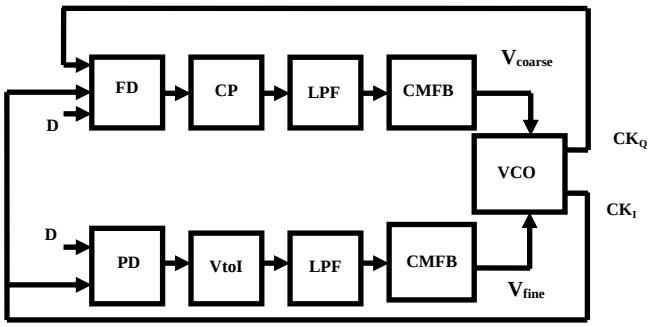

Figure 1. The Complete CDR System Block Diagram

The FLL provides a coarse acquisition of the clock and operates over a wide frequency range. It comprises of the Frequency Detector (FD), the Charge Pump (CP), the Low Pass Filter (LPF), Common Mode Feedback (CMFB), and a delay interpolating VCO. The FD is realized using a digital quadricorrelator and detects the frequency difference between the input data rate and the internally generated clock by the VCO. The outputs of the FD are the "UP" and "DOWN" pulses that have constant pulse durations and the number of pulses generated in a given time interval depends on the frequency difference. These pulses are fed to the charge pump, where they are converted into proportional charging and discharging currents for the LPF. The details of circuit design for individual blocks of the FD are given in [1, 2] and the same procedure has been adopted for the present work.

The design equations given below are from [1, 2, 13] and are used to determine the LPF parameters of the FLL.

$$\omega_c = \frac{I_{cp}.K_{VCO}.k_p}{2.\pi} \quad (1)$$

$$\omega_z = \frac{\omega_c}{5} = \frac{1}{R_p.C_p} \quad (2)$$

$$\omega_p = 5.\omega_c = \frac{C_p + C_s}{C_p.C_s.R_p} \quad (3)$$

$$C_s = \left[\omega_p.R_p - \frac{1}{C_p}\right]^{-1} \quad (4)$$

The symbols ω_c, ω_z, ω_p, ζ, and K_{VCO} in the above equations represent the crossover frequency, pole frequency, zero frequency, damping ratio, and VCO gain, respectively. The symbols R_p, C_p, and C_s represent the shunt resistor, capacitor and parallel smoothing capacitor, respectively.

The PLL in Fig. 1 has a much smaller capture range and operates after the FLL has acquired lock and this combination of FLL lock followed by PLL lock reduces the jitter in the recovered clock considerably. The PLL loop consists of a Phase Detector (PD), a Voltage-to-Current converter (V/I), and the LPF. The PD is an analog sample and holds system which consists of a two sample and hold circuits and a multiplexer. The output of the PD is a differential voltage proportional to the input phase difference. These voltages are converted to proportional currents by the V/I converter and are used as the charging and discharging currents of the LPF of the PLL block.

The VCO is a ring oscillator which is common to both FLL and PLL is realized with four delay cells and uses the delay interpolation concept with two paths, the fast path and the slow path. Fig. 2 shows the delay interpolation concept realized in the delay cell. The fast path consists of a differential stage, while the slow path consists of a constant delay stage and a differential stage. The two paths share the same output load. The output current is the sum of the slow and fast currents and is constant. The slow and fast currents are steered differentially depending on the control voltages to maintain constant sum.

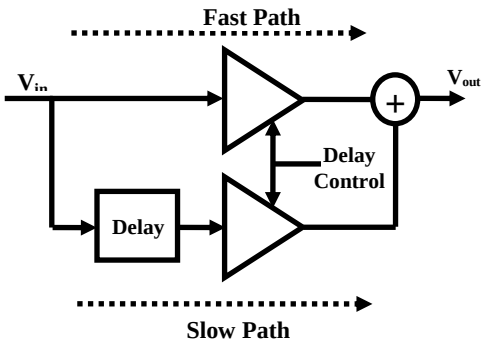

Figure 2. Shows the Delay Interpolation Concept

As in the case of the LPF of the FLL, the design procedure for determining the PLL loop filter parameters are adopted from [1, 2, 13] and the design equations are listed below:

$$\tau_2 = \frac{2.\zeta}{\omega_n} \quad (5)$$

$$K = K_{pd}.K_{VCO}.\frac{\pi}{4} \quad (6)$$

$$K = 2.\zeta.\omega_n.\sqrt{\frac{\tau_1}{\tau_2} + 1} \quad (7)$$

$$\tau_1 = \left(R_{f1} + R_{f2}\right).C \quad (8)$$

$$\tau_2 = R_{f2}.C \quad (9)$$

Where the symbols τ_1, τ_2, R_{f1}, R_{f2}, and c are represent the time constants, series resistor, shunt resistor and capacitor, respectively, of LPF of the PLL. The symbols ω_n, ζ, K, K_{PD}, K_{VCO} are the natural frequency, damping ratio, open loop gain, phase detector gain, and VCO gain, respectively and these values can all be determined once the operating frequency, bias currents and technology node of the CMOS process are chosen.

Detailed simulations have been carried to determine the performance of the dual loop delay interpolation CDR with respect to power supply noise. Though the details and quantitative results of these simulations are presented subsequently in Section 4, the conclusion that clearly emerged from these simulations was that the performance of the dual loop delay interpolation CDR was very sensitive to power supply noise, and that one cannot possibly use this CDR without dedicated regulators providing clean power supply to the whole system.

III. THE MANEATIS DELAY CELL-BASED VCO AND ITS MODIFICATION

It is well known from the PLL literature that the major contribution to jitter (or phase noise) due to power supply noise comes from the VCO block of the PLL, and this was true in the present CDR case as well (quantitative results given in the next section). Since the Maneatis Delay Cell-based VCO is well known for its immunity to power supply noise, the adaptation of this VCO to the dual loop CDR is described next.

The block diagram of the original Maneatis VCO and its associated bias generator are shown in Fig. 3 and Fig. 4, respectively. The Maneatis VCO shown in Fig. 3 basically comprises of four symmetric load delay cells for which the control voltages come from the bias generator circuit in Fig. 4. The Maneatis Delay cell-based VCO posses two salient features, first is its high supply immunity, and the second is its symmetric load resistance based delay element. The latter enables the VCO to have a wide operating frequency range. The symmetric load resistance can also reject the supply noise (dynamic supply noise rejection) and is obtained by having the lower limit of the voltage swing to be equal to the control voltage itself. Further, for static supply noise rejection, it is required that $V_{control}$ track the supply voltage variations and hence it is referenced to (V_{DD}) in [11, 12]. From this $V_{control}$, one has to generate two bias voltages V_{bp} and V_{bn} to be fed to the VCO of Fig. 3. Of these, V_{bp} tracks the supply voltage changes to keep the load resistance of the delay cell and hence, the output frequency constant. On the other hand, V_{bn} is kept independent of supply voltage changes in order to keep the tail current constant. It can be seen that the conventional bias generator shown in Fig. 4 can accept only one control voltage $V_{control}$, and hence cannot be directly incorporated directly into the dual loop CDR of Fig. 1.

To provide an option for accepting coarse and fine control voltages, the bias generator of the Maneatis VCO has been modified and is shown in Fig. 5. In this modified circuit, the coarse and fine control voltages are provided as gate voltages to two NMOS transistors which act as voltage controlled current sources (tail sources). These currents are summed up to form the drain current of a single PMOS transistor. Since the source of this diode connected PMOS transistor is connected directly to the supply rail, its gate voltage tracks the changes in supply voltage while maintaining the current set by the bottom tail transistors. This gate voltage of the PMOS is then used as part of a feedback loop containing the half replica delay cell to generate the bias voltages V_{bp} and V_{bn} which are used finally by the delay elements of the VCO. The final block diagram of modified Maneatis delay cell VCO is shown in Fig. 6. The voltage, V_{bp}, produced by the bias generator tracks the supply voltage and sets the lower limit of the oscillation swing (and the load resistance) to fix the output frequency. On the other hand, since the course ($V_{bn\text{-}coarse}$) and fine control voltages ($V_{bn\text{-}fine}$) are referenced to the ground terminal, the final voltage V_{bn}, which determines the tail current in the delay element, keeps the tail current constant.

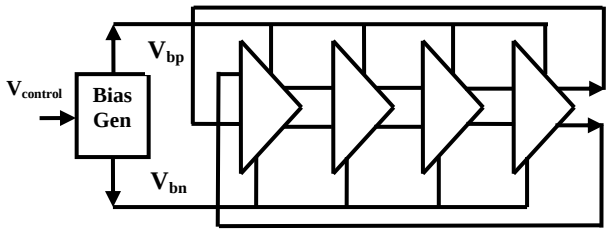

Figure 3. The original Maneatis VCO

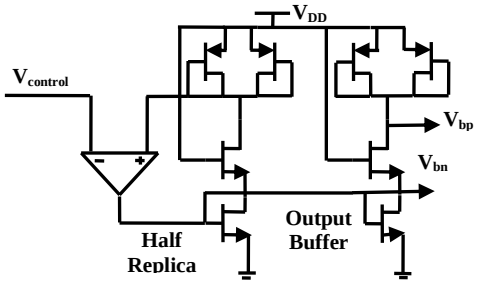

Figure 4. Original Bias Generator

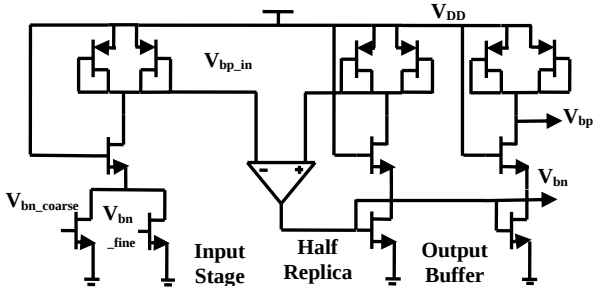

Figure 5. Modified Bias Generator

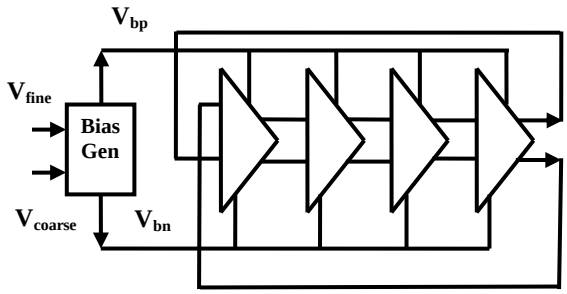

Figure 6. The proposed modified VCO

The simple modification proposed above for the bias generator provides a method for combining the coarse and fine control voltages while retaining the robustness of the original Maneatis VCO. The sensitivity of this VCO to power supply voltage variations were first assessed and then the VCO was incorporated into the original dual loop CDR scheme of Fig. 1. Using the same system specifications and design equations described earlier in Section 2, the parameters of the LPFs for the FLL and PLL have been determined and are listed in Table I. These parameters are different from those of the delay interpolation VCO because the coarse and fine gains of the modified Maneatis VCO are different from that of delay interpolation VCO.

IV. Simulation Results And Discussion

In this section, first, quantitative results related to the supply noise performance of the delay interpolating VCO based CDR are presented. Next, simulations results are presented to validate the modification carried out on the Maneatis VCO and also to demonstrate that it can indeed replace the delay interpolation VCO in the original dual loop CDR. Finally, for the modified dual loop CDR, simulation results related to its performance with respect to power supply noise are presented.

All simulations have been carried out using the Cadence Spectre tool. The devices chosen for the simulations are from the 0.35µm CMOS technology libraries from Austriamicrosystems and the various over-drive voltages and bias currents are chosen accordingly. For the present work, a nominal data rate of 833 Mbps is chosen for the CDR, the FLL cross over frequency is chosen as 30MHz, and the charge pump current of the FLL is found to be 125µA. The PLL loop natural frequency ω_n, and damping ratio ζ are chosen to be 0.5 MHz and 4, respectively. The FLL and PLL LPF parameters have been determined for the above system specifications and given in Table I. For clock recovery simulations, PRBS data of length 2^{14} were used as input data to the CDR system.

First, the delay interpolation VCO characteristics are given in Fig. 7 where the output frequency dependence on coarse and fine control voltages is shown. The coarse and fine gains are found to be 506MHz/V and 65.9MHz/V, respectively. Similarly, the modified Maneatis VCO circuit was simulated and Fig. 8 shows the corresponding VCO gains plots. The coarse and fine gains were found to be 3GHz/V and 230MHz/V, respectively.

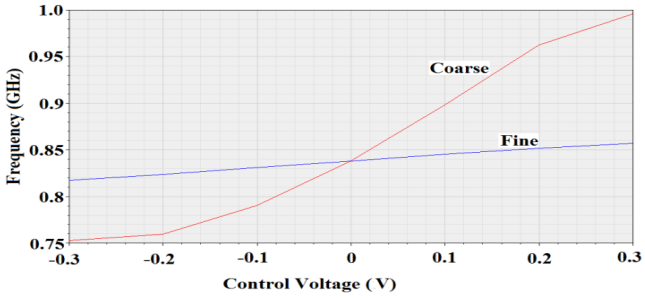

Figure 7. Coarse and Fine Gains of the Delay Interpolation VCO

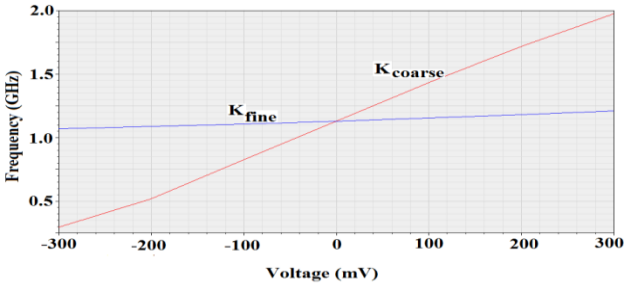

Figure 8. Coarse and Fine Gains of the Modified Maneatis VCO

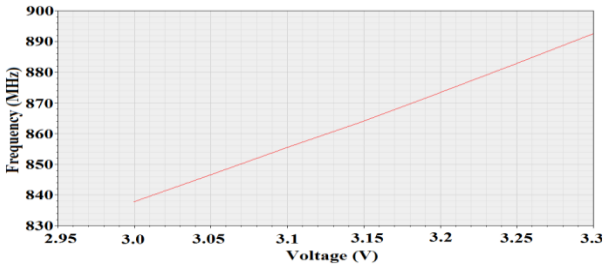

Figure 9. The Delay Interpolation VCO Sensitivity to Power Supply Noise

The static supply sensitivity of the delay interpolation VCO is shown in Fig. 9. For a nominal control voltage (Vc=0.74V, Vf=0.74V), it is found to be 185MHz/V and represents 6.6% frequency change for 10% change in the supply. The corresponding static supply sensitivity of the modified Maneatis VCO is shown Fig. 10.

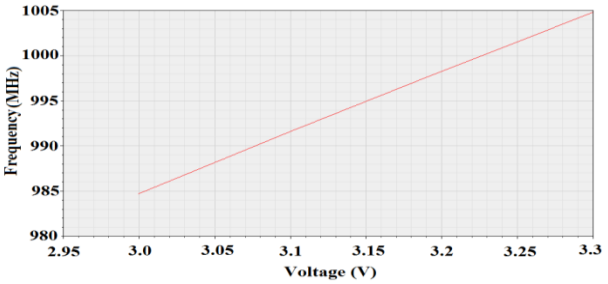

Figure 10. The Modified Maneatis VCO Sensitivity to Power Supply Noise

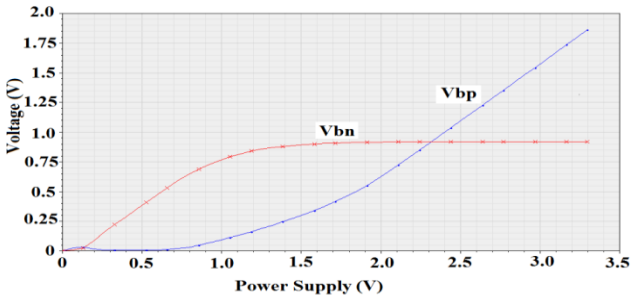

Figure 11. Variations of Vbn and Vbp versus Power Supply Voltage

For a nominal control voltage (Vc=0.95V, Vf=1.05V), it is found to be 67MHz/V and represents 2.4% frequency change for 10% power supply change. The reduction in sensitivity of the modified Maneatis VCO is to be expected and is due to the ability of the bias generator to track the variations of the power supply voltage and is demonstrated in Fig. 11. The variations of V_{bn} and V_{bp} with respect to V_{DD} are plotted in Fig. 11 while maintaining the coarse and fine voltages constant and it can be seen V_{bn} is independent of V_{DD} while V_{bp} tracks V_{DD} for static power supply variations. Incidentally, the modified Maneatis VCO also has better power supply sensitivity of 67MHz/V as compared to the value 158MHz/V reported recently in [14], though the latter is for a PLL and for a somewhat higher frequency.

Next, with PRBS data input, clock recovery was carried using two the CDR schemes using clean power supplies. The capture transient showing the evolution of coarse and fine control voltages of the dual loop delay interpolation CDR and the dual loop modified Maneatis CDR are depicted in Fig. 12 and Fig. 13, respectively. For the dual loop delay interpolation CDR, the lock time, the steady state ripple on the fine control voltage, and the recovered clock jitter are 1µsec, 50mV and 4.3psec (0.4%UI), respectively. The corresponding quantities are for the dual loop modified Maneatis CDR are 0.6 µsec, 10mV, and 8.4 psec (0.7%UI), respectively.

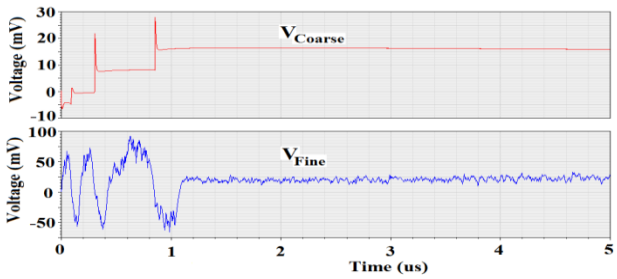

Figure 12. CDR Coarse and Fine Control Voltages with Clean Power Supply for Delay Interpolation VCO

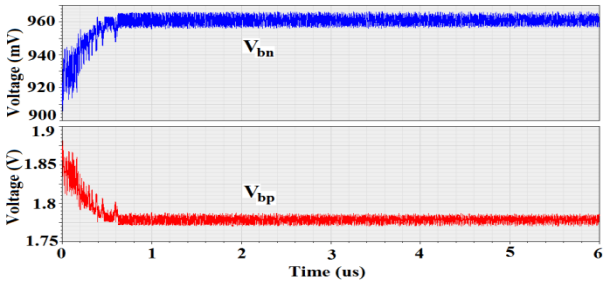

Figure 13. CDR Control Voltages with Clean Power Supply for Modified Maneatis VCO

Immunity of the two CDR schemes to power supply noise is characterized by adopting the procedure followed in [11, 12]. Noise sources in the form of sinusoidal signals of different frequencies and amplitudes were superposed on the VDD supply node. The effects of this noise source on the CDR system are measured by two ways. First by measuring the ripple on the differential fine control voltage and the second one is measuring the rms jitter on the recovered clock.

Table II provides the jitter performance of the dual loop delay interpolation CDR with noise injected individually into the power supply node of the different blocks of the CDR. Each column of the table indicates the ripple on the control voltage (after lock) of the dual loop CDR and the jitter on the recovered clock for a specific noise amplitude. It can be seen that the VCO is the most sensitive block and causes maximum degradation of performance. It was also found that the system fails to lock if the noise amplitude is increased beyond 30mV. Fig. 14 shows the differential fine control voltages of the dual loop delay interpolation CDR with noise of 20mV@10MHz on power supply terminal. For comparison, the same parameters are plotted for the dual loop modified Maneatis CDR in Fig. 15 but with a power supply noise of 200mV@10MHz.

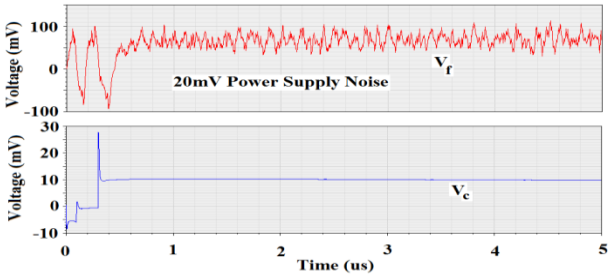

Figure 14. CDR Control Voltages with 20mV@10MHz Power Supply Noise for Delay Interpolation VCO

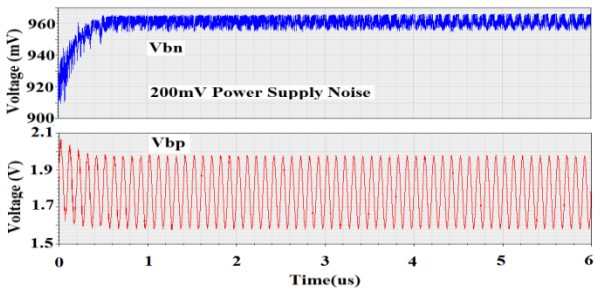

Figure 15. CDR Control Voltages with 200mV@10MHz Power Supply Noise for Modified Maneatis VCO

Finally the jitter performance of the integrated dual loop delay interpolation CDR and the proposed dual loop modified Maneatis CDR are given in Table III. It can be seen that the performance of the latter with 200mv noise is comparable to that of the former with a 30 mV noise on the supply line. The ripple voltage on the control voltage is not listed for the proposed CDR since this tracks the noise on the supply voltage as it is supposed to.

Since the Maneatis VCO and the delay interpolation VCO of the original dual loop scheme are both differential delay cell-based ring oscillators, their power consumption is nearly the same. Since the loop parameters for the proposed scheme have been chosen to be the same as that of the original dual loop scheme, the acquisition time is also nearly the same. Maneatis VCO is inherently known to have a wide range of operating frequencies.

V. CONCLUSIONS

While it is noted in the literature that the dual loop CDR architecture has certain important desirable features not available in other architectures (see [15] for example), there are no studies reporting its jitter performance with respect to power supply noise. While this might not have been an issue in the older technologies where dedicated external regulators providing clean supplies to the CDR can be assumed, in the context increased integration and System on Chip (SOC) schemes, on chip power supply noise often becomes a serious issue. The results presented in this paper provide three important conclusions. The first is that the original dual loop CDR as proposed in [1] is very sensitive to power supply noise and may require dedicated power supply regulators. The second conclusion is that the original Maneatis delay VCO can indeed be easily modified for incorporation into the dual loop CDR. The third conclusion is that the resulting modified dual loop CDR is capable tolerating nearly 200 mV noise on the supply line without degradation in performance. This in turn indicates that it can be easily integrated onto (SOC) architectures without requiring dedicated supply regulators.

TABLE I. THE PLL AND FLL LPF PARAMETERS

CDR in Ref. [5]				**CDR with proposed VCO**			
PLL		***FLL***		***PLL***		***FLL***	
R1 (kΩ)	996	***Rp (kΩ)***	3	***R1 (MΩ)***	4	***Rp (Ω)***	503
R2 (kΩ)	107	***Cp (pF)***	9	***R2 (kΩ)***	107	***Cp (pF)***	53
C (pF)	150	***Cs (fF)***	371	***C (pF)***	150	***Cs (pF)***	2

TABLE II. JITTER ON RECOVERED CLOCK OF THE CDR WITH VCO OF REF. [5]

Parameters	**with Noisy Power Supply**		
Noise amplitude at 10MHz (mV)	10	20	30
Jitter on Recovered clock ps, (%UI)	25, (2)	52, (4)	63, (5)
Ripple on Vfine (mV)	50	55	60

TABLE III. BLOCKWISE NOISE PERFORMANCE OF THE CDR WITH VCO OF REF. [5]

Parameters	**With Noisy Power Supply Only On**				
Noise of 20mV at 10MHz	**VCO**	**FD**	**PD**	**CP**	**VtoI**
Jitter on Recovered clock ps, (%UI)	50, (4)	11, (1)	11, (1)	8, (1)	16, (1)
Ripple on Vfine (mV)	75	50	45	50	40

TABLE IV. JITTER ON RECOVERED CLOCK OF THE CDR WITH PROPOSED VCO

Parameters	**with Noisy Power Supply**		
Noise amplitude (mV) at 10MHz	50	100	200
Jitter, ps (%UI) on Recovered clock	23, (2)	34, (3)	57, (5)

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REFERENCES

[1] Seema Butala Anand and Behzad Razavi, “A CMOS Clock Recovery Circuit for 2.5-Gb/s NRZ Data”, (2001), IEEE Journal of Solid-State Circuits, Vol. 36, No. 3, pp. 432-439.

[2] Yi-Ju Chen and Monuko du Plessis, “An integrated 0.35 µm CMOS optical receiver with clock and data recovery circuit”, (2006), Microelectronics Journal, pp. 985-992.

[3] Ming-ta Hsieh and Gerald E. Sobelman, “Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery”, (2008), IEEE Circuit & System Magazine, pp. 45-57.

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[4] Bryan Casper and Frank O'Mahony, "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links—A Tutorial", (2009), IEEE Transaction Circuit and System—I: Regular papers, 56(1), pp. 17-39.

[5] Behzad Razavi, "Phase-Locking in Wire line Systems: Present and Future", (2008), IEEE Custom Integrated Circuits Conference, pp. 615-622.

[6] Zuoguo (Joe) Wu and Evelina Yeung, "Multi-Gigabit I/O Link Circuit Design Challenges and Techniques", (2007), Electromagnetic Compatibility Symposium.

[7] Abhijith Arakali, Nema Talebbeydokthi, Srikanth Gondi, and Pavan Kumar Hanumolu, "Supply- Noise Mitigation Techniques in Phase-Locked Loops", (2008), European Solid-State Circuits Conference, pp. 374-377.

[8] Tzung-Je Lee and Chua-Chin Wang, "A Phase-Locked Loop with 30%Jitter Reduction Using Separate Regulators", (2008), VLSI Design, pp. 1-8.

[9] Josh Carnes, Igor Vytyaz, Pavan Kumar Hanumolu, and Kartikeya Mayaram, Un-Ku Moon, "Design and analysis of noise tolerant ring oscillators using Maneatis delay cell", (2007), IEEE International Conference on Electronics, Circuits, and Systems, pp. 494-497.

[10] Marcus van Ierssel, Hisakatsu Yamaguchi, Ali Sheikholeslami, Hirotaka Tamura, and William W. Walker, "Event-Driven Modeling of CDR Jitter Induced by Power-Supply Noise, Finite Decision-Circuit Bandwidth, and Channel ISI", (2008), IEEE Transaction on Circuits And Systems—I, Vol. 55, No. 5, pp. 1306-1315.

[11] John G. Maneatis and Mark A. Horowitz, "Precise Delay Generation Using Coupled Oscillators", (1993), IEEE Journal Solid-State and Circuits, VOL. 28, NO. 12, pp. 1273-1282.

[12] John G. Maneatis, "Low jitter process independent DLL and PLL based on self-biased techniques", (1996), IEEE Journal of Solid-State and Circuits, Vol. 31, No. 11, pp. 1723-1732.

[13] Keiji Kishine, Kiyoshi Ishii, and Haruhiko Ichino, "Loop-Parameter Optimization of a PLL for a Low-Jitter 2.5-Gb/s One-Chip Optical Receiver IC with 1: 8 DEMUX", (2002), IEEE Journal of Solid-State Circuits, Vol. 37, No. 1, pp. 38-50.

[14] Xiong Liu, Alan N. Willson, and Jr., "A 3 mW/GHz Near 1-V VCO with Low Supply Sensitivity in 0.18-µm CMOS for SoC Applications", (2009), IEEE International Midwest Symposium on Circuits and Systems pp. 90-93.

[15] Ming-ta Hsieh, Gerald E. Sobelman, "Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery", Fourth Quarter (2008), IEEE Circuits and Systems Mag., pp. 45-57.

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A Flexible Sensor-mat to Automate the Process of People Counting

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***Abstract*—Real data on the peoples mobility are an essential input for decision-makers of city and regional planning. They allow for various optimizations like traffic routes, public places or safety measures at public events. Obtaining such data in an automated and reliable way is a burdensome task since usually the requirements on the respective solutions depend on the actual situation (e.g., indoors, outdoors, different counting cross-sections). This paper reports on the work-in-progress of the development for a flexible, low-power sensor-mat that automates people counting.**

***Keywords*-sensor-mat; people counter; mobility; wireless networks.**

I. Introduction

Accurate and representative mobility data, especially for motorized traffic is a vital information for our daily life. It allows for up-to-date traffic control and provides input for spatial planning and resource optimizations of the public infrastructure, see, e.g., [8]). In fact, many automated counting techniques (e.g., [12], [11]) are in use today and have superseded almost all manual counting's. In fact permanent, fully automated counting solutions are installed at many street sections of high interest, delivering reliable traffic data that is used for dynamic speed control information systems, navigation systems, etc.
Respective mobility data for non-motorized traffic, so far, is primarily used by operators of infrastructures like railway stations, airports or shopping malls for various optimizations. For example, using this data one can optimize train schedules and respective transfer times to enhance the attractiveness of public transportation. Likewise, a shopping mall operator can influence the habitual buying behavior and thus better the overall property value. The same data can be used for safety measures in public buildings or at large events by, e.g., restricting access to certain regions when the number of people exceeds the respective capacity. There exist a multitude of automated people counting technologies, see, e.g., [2], [5], or [16]. At present, however, none satisfies all the diverse requirements commonly encountered in practice.

Section II highlights our motivation and lists requirements contributed in a project workshop by various infrastructure operators and urban planners. Next, section III elaborates on related work, before we highlight the challenges and our first concepts in section IV. Finally, we present our status quo before we conclude the paper with an outlook of our next steps.

II. Motivation and Requirements

Manual people counting's using some sort of tally counter are still frequently performed in practice to gather information on the non-motorized traffic patterns. This manual approach suits short counting's and low to medium traffic densities; especially since almost no installation/setup overhead is required. For longer durations or dense traffic, however, the data gathered using a manual approach is often either not representative or inaccurate. To overcome this issue, many automated people counting approaches exist, see Section III for an overview. However, many of these solutions only fit part of the requirements on an automated people counting system as listed below:

Costs: Some solutions for automated people counting necessitate rather high equipment investments (e.g., many solutions based on laser technologies), require elaborate software for data analysis and are costly in terms of extra on-site installations (power and/or network access).
Flexibility: Restriction due to local geometries (e.g., at entrance situations) or due to size restrictions of the measurement technology frequently limit the flexibility of existing methods in practice. Furthermore, most automated people counters require dedicated on-site installations.
Quality: Especially in dense traffic or extreme environmental situations the automatically gathered data is often inaccurate. Furthermore, for almost all commercial-off-the-shelf people counters no explicit measuring error probability is available, limiting the use of collected data in such situations.
Environmental Influences: Several sensors have problems with fluctuations in temperature or lighting – e.g., at entrances – and eventually wind-up delivering incorrect data. Furthermore, only a sub-set of the available solutions can be used out-doors.
Mobility: For temporal people counting's spanning several days/weeks (e.g., to optimize pedestrian traffic lights) an autonomous, almost energy self-sufficient system is required. Existing, solutions that fit this requirement are only available

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for counting individuals (e.g., using active infra-red sensors).

Data collected via sensor fusion addresses most of the aforementioned requirements, increases, however, the system complexity and costs, cf. [14]. In the project Flexicount we are developing an outdoor capable sensor-mat that enables plug&play counting of people crossing a defined intersection.

III. Related Work

In recent years different technologies for counting people have been developed and used. The following list gives a short overview and provides an informal assessment of the respective strengths and weaknesses:

Counters based on *active infrared sensors* are typically low-cost, have low power consumption, allow for a simple installation and are portable. These devices, however, are not able to discern between pedestrians and other moving objects (e.g., raindrops) and cannot separate multiple pedestrians crossing a given line-of-sight at the same time.
Passive infrared counters, see e.g., [7] and [9], using thermal images are available at moderate costs, feature low energy consumption and are operable in humid or foggy weather conditions. Furthermore, these systems are legally defensible with regard to data privacy. Drawbacks of these devices are their rather limited usability in dense traffic situations, the requirement for over-head installation, the limited co, see [3]verage of widths where counting is feasible and their dependence on temperature differences.
Better counting accuracy is obtained by relying on *laser-scanners*, see [15], [6]. These counters work reasonably well even in crowded areas, allow separation of individuals, usually are simple to setup and can operate on wider cross-sections. Their drawback is mainly due to the high initial costs, their limited usage under different weather conditions and their rather bulky and heavy construction.
Vision based counting solutions, see [10], [13], can operate on larger cross-sections, and give somewhat accurate results – some even under varying lighting conditions (stereo vision based systems) and when recorded allow for further post-analysis. These systems are usually simple to setup and require only moderate installations. Drawbacks are influences of the operation on different environmental conditions, legal issues with respect to data privacy, and are often only available for indoor scenarios.
The company eco-counter (http://www.eco-compteur.com) distributes an *acoustic counting solutions* where plates are buried about $5cm$ below the surface. Individuals crossing the respective section get counted by acoustic means. This outdoor capable solution operates in an almost energy self-sufficient way for several years, allows, however, to count only one crossing person per plate. Thus this method is only usable for low traffic density scenarios. Multiple plates are required for bi-directional counting and significant installation overhead is required. Hence, the solution is best suited for fixed installations.
A solution measuring the change in the *magnetic field* is distributed by the company Future Shape (http://www.future-shape.com) under the product name *SensFloor*. This technology, however, has only limited use for actual people counting's since it was specifically developed for the domain of *ambient assistive living*.

A detailed overview and evaluation of existing people counting solutions was presented in [1] and [4]. Despite all the advances, manual counting's using *tally counters* are still used most of the times, see [3], [4]. For small samples this method is cost-effective and allows high accuracy for low traffic densities. However, bidirectional counting's, higher people traffic densities, and the short time-spans that can be covered in this way limit this method.

IV. Flexicount - Development of a flexible sensor-mat for people counting

A flexible solution that enables an automated counting of passenger traffic delivering reliable data is needed with growing urbanization and ever increasing traffic. In particular, such a solution should be mobile, allowing to count for several days or weeks, cost effective and require only a minimum of installation and maintenance overhead. In addition it must be adaptable for various different cross-sections (counting widths) and robust against environmental influences for outdoor use.

A. Aims

In the project Flexicount we are developing a sensor-mat with integrated sensors that register people traversing the mat. The gathered measurement values are relayed via a wireless sensor network to a host computer that performs the actual analysis and counting. The mats are self-sufficient and can be simply placed beneath each other, hence one can flexibly cover different cross-sections. Figure 1 illustrates the prospective approach.

The following functional requirements will be addressed in Flexicount:

(r1) sensors to identify people crossing in any direction (ability to discern between people and most other objects)
(r2) temporal referenced, multi-directional counting's
(r3) real-time wireless data transmission (plug&play operation)
(r4) high accuracy with known error probability
(r5) ability to calibrate the electronics
(r6) energy self-sufficient operation for multiple weeks
(r7) polymer-matrix that provides a reasonable load and pressure distribution (e.g., to handle stilettos)

Furthermore, we will address the following non-functional aspects:

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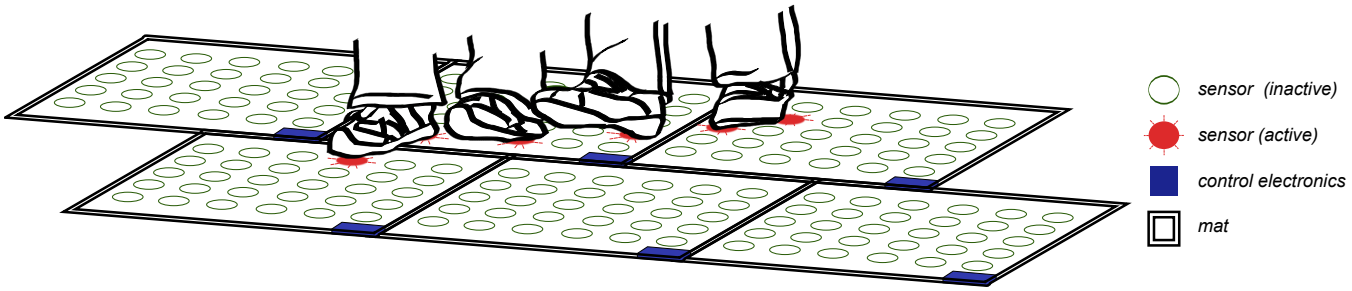

Figure 1. Multiple Flexicount mats in operation

(r8) small weight
(r9) simple adaption to different cross-section
(r10) minimum installation and maintenance overhead
(r11) usable for in- and out-door applications (waterproof, wide temperature range, robustness)
(r12) safety related features (skid-proof, small mat heights, markings, etc.)
(r13) hardened against vandalism and denial-of-service
(r14) low cost

B. Status Quo

So far, we have developed the sensors with respective control electronics, evaluated some commercial-off-the-shelf wireless radios for our application, and performed a polymer integration with a first prototype.

The sensors – addressing requirements (r1-r2) – basically consist of a multiplexed switch array where contacts are placed at regular intervals ($30mm$ apart) on a $0.15mm$ thick printed circuit board with a dimension of $450x450mm$. On top of this PCB we use a separate contact plane; currently we are evaluating and testing different options with regard to their long-term behaviour (>100.000 load cycles):

(a) a microwave absorbing elastomer with a volume resistivity of 4-5Ω/cm
(b) an array of snap-disks with constant force-displacement characteristics
(c) an elastomer treated with a conductive coating

For the case when we select options (b) or (c) we will complement this sensor array with a number of equidistantly distributed force-sensors. In case option (a) will be selected we are able to omit the latter sensors since the force canöah be directly measured via the contact resistance between the elastomer and the contacts on the printed circuit board. In this case all multiplexed rows must be analog-to-digital converted. First experiments seem promising in this regard, however, a careful long-term evaluation is still under way. Figure 2 shows the mat build-up sequence of an early prototype peeled apart.

For the wireless network we have currently opted for a low-power commercial-off-the-shelf, meshed ZigBee solution; mainly to satisfy the required bandwidth required to handle the worst-case data volume, cf. requirement (r3). For an end-product, we will eventually be able to replace ZigBee with ANT — in case we can reduce the transmitted data volume — in order to optimize for low power consumption. Our prototypes' power is currently supplied via a rechargeable battery that is charged occasionally (after some weeks of operation) via an inductive loop (similar to the principle widely employed in electrical tooth-brushes), cf. (r6).

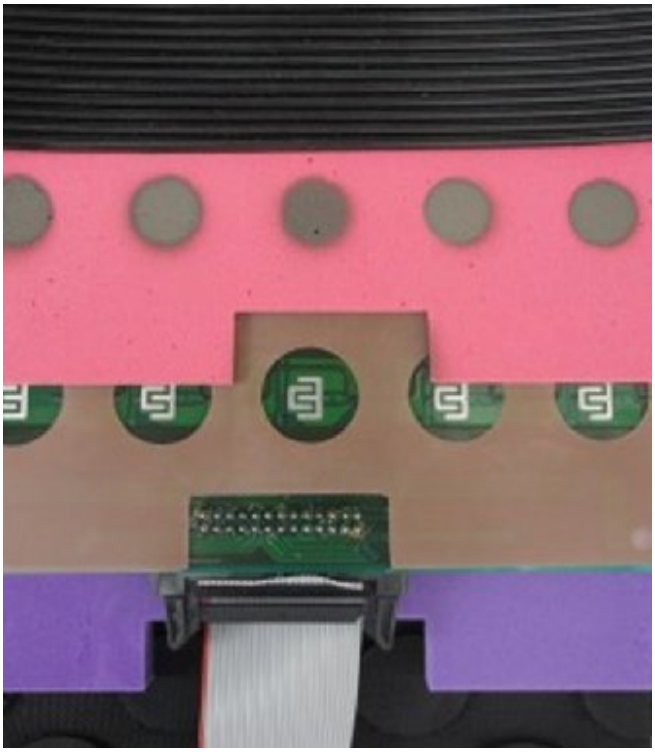

Figure 2. Mat buildup sequence of an early prototype

The polymer integration of our prototype is presently build from a $3mm$ thick viscous elastic polymer at the bottom to accommodate for various different surfaces (e.g., stone chips). Above we use an elastomer to embed the electronic circuitry; this layer must incorporate the various different heights of the devices. On top of this layer we place our contact plate (options (a)-(c) from above) followed by a

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$3mm$ thick elastomer that provides the desired load and pressure distribution and serves as protective layer. The top-most layer is made of a sunfast abrasive wear that provides the visible surface finish. The entire polymer embedding is waterproof and enables an outdoor use.

V. CONCLUSION

This paper presents a work-in-progress report of the development of a sensor-mat that will eventually facilitate an automated counting of peoples traversing the mats. The approach has the potential for use even in dense traffic scenarios both in- and outdoors and will eventually provide a solid data basis for regional planners.
Our next steps are to finalize the long-term evaluations and analysis of our contact planes, before we are able to produce the first prototypes. The latter will than be used for field tests in order to optimize the sensor-mats for the given requirements in a follow-up re-design.

ACKNOWLEDGMENT

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REFERENCES

[1] Bu F., Greene-Roesel R., Diogenes M.C., and Ragland D.R.: *Estimating Pedestrian Accident Exposure: Automated Pedestrian Counting Devices Report*, Transportation Research Report (TRB 2007), p. 31, March 2007.

[2] Crabtree M.R.: *Smart pedestrian counter system (SPECS)*, 11^{th} International Conference on Road Transport Information and Control, pp. 100–104, 2002.

[3] Diogenes M., Greene-Roesel R., Arnold L., and Ragland D.: *Pedestrian counting methods at intersections: A comparative study*, Transportation Research Report (TRB 2007), p. 12, April 2007.

[4] Greene-Roesel R., Diogenes M., Ragland D., and Lindau L.: *Effectiveness of a commercially available automated pedestrian counting device in urban environments: Comparison with manual counts*, Proceedings of the 2008 Transportation Research Board 87^{th} Annual Meeting: Conference Recordings, pp. 1–17, 2008.

[5] Gasparini L., Manduchi R., and Gottardi M.: *An Ultra-Low-Power Contrast-Based Integrated Camera Node and its Application as a People Counter*, Seventh IEEE International Conference on Advanced Video and Signal Based Surveillance (AVSS), pp. 547–554, 2010.

[6] Huijing Z. and Shibasaki R.: *A novel system for tracking pedestrians using multiple single-row laser-range scanners*, IEEE Transactions on Systems, Man, and Cybernetics, Vol. 35, Iss. 2, pp. 283–291, 2005.

[7] Hao Q., et al: *Human tracking with wireless distributed pyroelectric sensors*, IEEE Sensors Journal, Vol. 6, No. 6, pp. 1683–1694, Dec. 2006.

[8] Haihong F., Jiang P., Shuijin S., and Anke X.: *Research on a New Type of City Intelligent Traffic Lights*, Control Conference (CCC 2006), pp. 1733–1736, 2006.

[9] Li N. and Hao Q.: *Multiple walker recognition with wireless distributed pyroelectric sensors*, Proceedings of SPIE Defense and Security, pp. 694034(1-12), March 2008.

[10] Rabaud V. and Belongie S.: *Counting Crowded Moving Objects*, Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pp. 705–711, 2006.

[11] Tanaka M.: *Development of traffic counters by laser range scanners*, Proceedings of the SICE Annual Conference 2010, pp. 3128–3134, 2010.

[12] Tseng B.L., Ching-Yung L., and Smith J.R.: *Real-time video surveillance for traffic monitoring using virtual line analysis*, Proceedings of 2002 IEEE International Conference on Multimedia and Expo, 2002 (ICME '02), Vol. 2, pp. 541–544, 2002.

[13] Teixeira T. and Savvides A.: *Lightweight People Counting and Localizing in Indoor Spaces Using Camera Sensor Nodes*, ACM/IEEE International Conference on Distributed Smart Cameras, pp. 36–43, 2007.

[14] Weingand R. and Hehring T.: *Tipps zur Planung eines Personenzählsystems*, Artikel im POS Manager: Fachmagazin für IT-Lösungen und Management im Einzelhandel, Ausgabe 1, pp. 55-57, 2009. (in german)

[15] Zhao H. and Shibasaki R.: *A Real-Time System for Monitoring Pedestrians*, 7^{th} IEEE Workshop on Application of Computer Vision (WACV/MOTION'05), Vol. 1, pp. 378–385, 2005.

[16] Zhu Q., Tang L., Jiang Y., and Deng W.: *A novel approach of counting people based on stereovision and DSP*, The 2nd International Conference on Computer and Automation Engineering (ICCAE), Vol. 1, pp.81–84, 2010.

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Interaction of Semiconductor Laser Chirp with Fiber Dispersion: Impact on WDM Directly Modulated System Performance

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Abstract—In this paper, we have analyzed the interaction of semiconductor laser chirp with the fiber chromatic dispersion characteristics in order to study the impact on a Wavelength Division Multiplexing (WDM) directly modulated system performance. Also, we have demonstrated that the system transmission performance depends, strongly, on the Directly Modulated Laser (DML) output power and its adiabatic and transient chirp parameters. We have calculated by simulation, that the effect of DMLs chirp can be compensated by a negative dispersion fiber in a specific range of the DML output power. In addition, a pulse broadened by the positive dispersion fiber can be equalized using self-phase-modulation (SPM) in the optical fiber. The majority of metro and access networks are made up of conventional single-mode fibers (SMF) which are positive dispersion fibers. We have demonstrated that the optimum compensation is always feasible for such fibers by changing the optical output power in the DML laser. Furthermore, simulations suggest that this technique is able to enhance the performance of directly modulated wavelength division multiplexed systems if the power of each channel is chosen correctly.

Keywords- ***directly modulated laser; adiabatic and transient chirp; linewidth enhancement factor; adiabatic coefficient; fiber chromatic dispersion.***

I. INTRODUCTION

Direct modulation laser schemes have been used during last few years because of their intrinsic simplicity and cost-effectiveness, especially when applied to metro and access networks. However, frequency chirp characteristics of directly modulated lasers (DMLs) limit significantly the maximum achievable transmission distance over standard single-mode fibers (SMF).

A number of different approaches have been studied to improve transmission performance using DMLs, including cutting down the chirp externally using a narrow band-pass filter and the deployment of a negative dispersion fiber. With respect to this last approach, others authors have proposed their use (i.e., MetroCor^{TM} fiber) in order to take advantage of the positive transient chirp of DMLs to increase transmission distances, [1-4]. However, typical metro and access networks installations use conventional single-mode fibers (SMF) and because of the cost and difficulty (or lack of feasibility) in changing embedded fiber links, a method that enhances system performance requiring only the modification of one or both endpoints of a link is a critical requirement.

In this work, we have demonstrated that the transmission performance depends strongly on DML output power and on its adiabatic and transient chirp. We also demonstrated that systems using SMF fibers can achieve a good performance if the DML output power is properly chosen. We have found a mathematical expression that make an estimation for a power value to fix the laser power output for each channel in WDM systems.

Section II is dealing with a short theoretical background to understand the impact of the chirp, adiabatic and transient, in DML lasers; Section III points out the system of reference characteristics (16 channel WDM) for the simulations and the different cases considered and finally in Section IV comparisons after simulations of different cases in a 32 channel WDM system are commented.

II. THEORETICAL BACKGROUND

A Distributed Feed-Back (DFB) laser which oscillates in a single longitudinal mode, under CW (Continuous Wave) operation, may experience dynamic line broadening when the injection current is directly modulated. This line broadening is a frequency chirp associated with modulation-induced changes in the carried density [5-6]. The frequency variation, $\Delta\nu$, of a DFB-DML is related to the laser output optical power, *P(t)*, through the expression, [7]:

$$\Delta\nu(t) = \frac{\alpha}{4\pi}\left\{\frac{d}{dt}\left[\ln(P(t)\right] + kP(t)\right\} \qquad (1)$$

where α is the linewidth enhancement factor [8] and *k* is the adiabatic chirp coefficient. The first term of (1), related to transient chirp, causes variations in the pulse width, while the second term (adiabatic chirp) produces a timing shift between "1" and "0" levels, depending on the output power.

The frequency chirp, due to the adiabatic chirp and shown in Figure 1 (a), implies a shift in the wavelength emission, as

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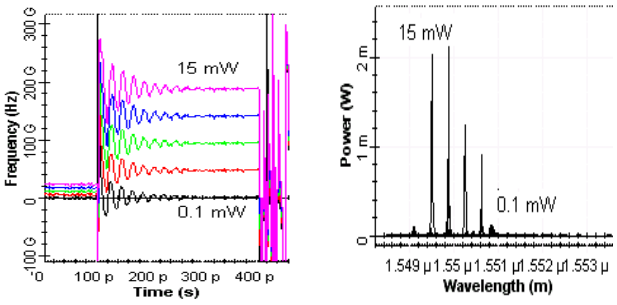
it shown in Figure 1 (b). The optical frequency shift from the actual laser output frequency is the principal cause of system performance variations.



(a) (b)

Figure 1. (a) Chirp and (b) Spectrum of the signal at the output DML for a power range 0.1-15 mW.

The α-parameter affects the laser bandwidth, so that large α-parameters cause increased laser spectral width. Figure 2 shows the output spectrum laser for α-parameters 1 and 10. A higher spectral width for α = 10 case is obtained.

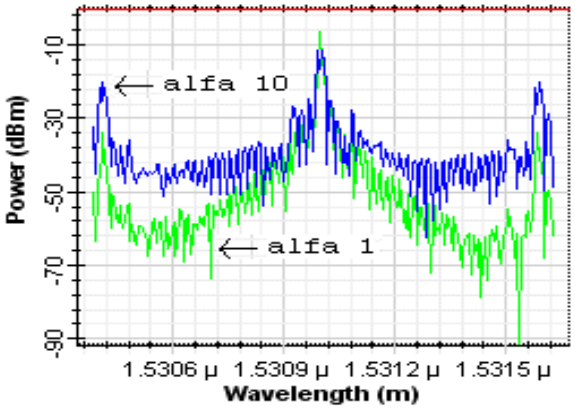


Figure 2. Output laser spectra for α = 1 and α =10.

This spectral bandwidth causes a pulse time broadening, T_1, when it goes through the fiber [9], which expression after a length z of fiber is:

$$b_f(z) = \frac{T_1}{T_0} = \left[\sqrt{\left(1 - \frac{\alpha \beta_2 z}{T_0^2}\right)^2 + \left(\frac{\beta_2 z}{T_0^2}\right)^2} \right] \quad (2)$$

where β_2 is the group velocity dispersion parameter (GVD) and T_0 is related with the FWHM (*full width at half-maximum*) as $T_{FWHM}=2(\ln 2)^{1/2}T_0 \approx 1.665\ T_0$.

In Fig. 3, the pulse broadening parameter variation is shown. The initial pulse width chosen is T_0 = 30 ps (T_{FWHM} = 50 ps), for 3 different values of the α-parameter: 0, 2 and 4. In all cases there is a minimum broadening of the pulse obtaining, for this case, the best behaviour of the system.

The *adiabatic coefficient*, κ, depends on the laser structure, being the figure that takes into account the output power and the generated chirp, (1). The relationship to the photon energy, $h\nu$, optical frequency, υ, and laser quantum efficiency, η_0 , confinement factor, Γ, cavity volume, V_0 and gain compression factor, ε, is in agreement with the expression:

$$\kappa = \frac{2\Gamma}{\eta_0 h \nu V_a} \varepsilon \quad (3)$$

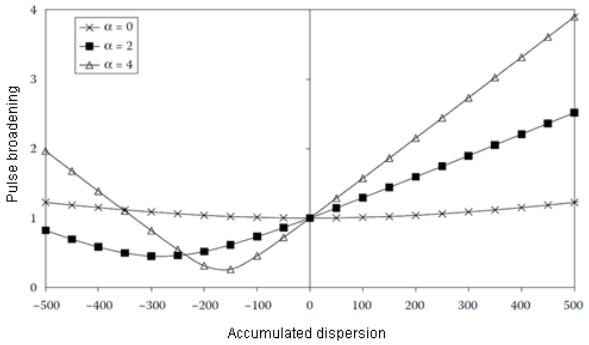


Figure 3. Pulse broadening parameter for transient chirp , at λ = 1550 nm, as a function of the accumulated dispersion, D.L

In Fig. 4 the optical spectrum for three lasers, with the same output power and different κ coefficient is shown. The wavelength of emission is 1551 nm. As bigger is the κ coefficient, wider is the spectrum and lower is the output power.

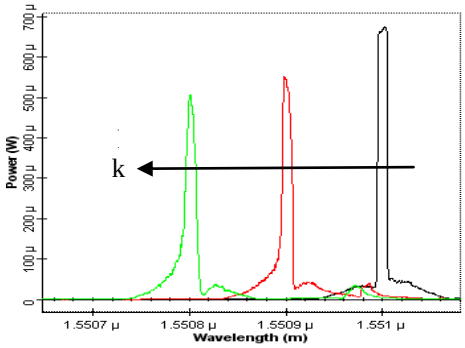


Figure 4. Laser spectrum shifting due to an adiabatic chirp with different values of κ

Laser chirping can lead to a significant dispersion effects for intensity-modulated pulses when the laser emission wavelength is displaced from the zero-dispersion wavelength of the fiber. In Fig. 5, the pulse chirp is plotted together with the pulse intensity. Whereas the input pulse is chirpless, the instantaneous frequency of the output pulse decreases from the leading to the trailing edge of the pulse. The reason for this is the Group Velocity Dispersion (GVD). In case of anomalous GVD, the higher frequency ("blue-shifted") components of the pulse travel faster than the lower frequency (or "red-shifted") ones, [10].

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The effect of GVD on the pulse propagation depends, mainly, on whether or not the pulse is chirped, the laser injection pulse shape, [11-12], and also on the fiber SPM (Self Phase Modulation). With the correct relation between the initial chirp and the GVD parameters, the pulse broadening (which occurs in the absence of any initial chirp) will be preceded by a narrowing stage (pulse compression). On the other hand, the SPM alone leads to a pulse chirping, with the sign of the SPM-induced chirp, being opposite to that induced by anomalous GVD. This means that in the presence of SPM, the GVD induced pulse-broadening will be reduced (in the case of anomalous), while extra broadening occurs in the case of normal GVD.

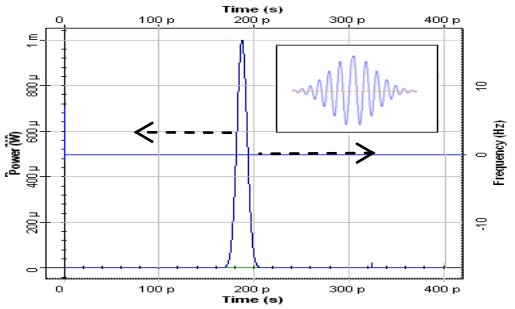

Figure 5. (a) Output pulse shape and chirp for free chirp Gaussian pulse (b) Output pulse shape and chirp after a fiber length

III. SYSTEM OF REFERENCE

We have to point out that the transmission performance of waveforms produced by directly modulated lasers, in fibers with different signs of dispersion, depends strongly on the characteristics of the laser frequency chirp.

TABLE I. VALUES AND RANGES OF DML PARAMETERS

Parameter	DML-T	DML-A
Alpha coefficient, α	5.6	2.2
Adiabatic chirp, κ (W.s)$^{-1}$	$1.5 \cdot 10^{12}$	$28.7 \cdot 10^{12}$
Output Power range	0.1 - 15 mW	
Extinction Ratio	9 dB	
RIN (Relative Intensity Noise)	- 130 dB/ Hz	

For this reason, to study the WDM system performance, a simple arrangement is proposed. It is made up of two kinds of DFB-DMLs lasers presenting extreme behaviors: DML-A is strongly Adiabatic chirp dominated and DML-T is strongly Transient chirp dominated. The parameter values for the two simulated DMLs are shown in Table I.

We have used two kinds of optical fibers; the already laid and widely deployed single-mode ITU-T G.652 fiber (SMF) and ITUT-T G.655 fiber Recommendations with a negative dispersion sign around C band, *Non-Zero Negative Dispersion Shifted Fiber* (NZ-NDSF) (see Fig. 6).

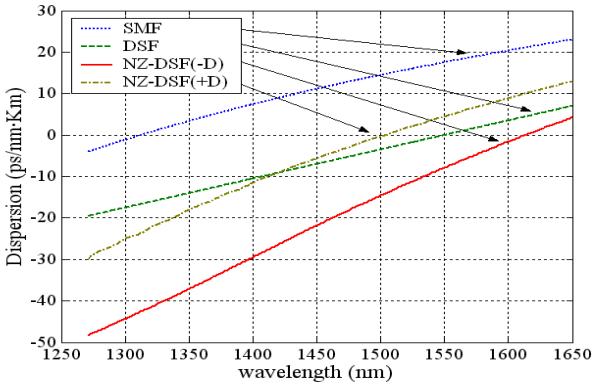

Figure 6. Dispersion Coefficient for different optical fibers

In a computer simulations, four different systems (*Cases A, B, C and D*) have been analyzed based on the optical system of Fig. 7. Table II summarize the different *Cases*.

TABLE II. ANALYZED CASES

Case	DML	Fiber
A	DML-A	SMF
B	DML-A	NZ-NDSF
C	DML-T	SMF
D	DML-T	NZ-NDSF

In this work, we are mainly interested in comparing the system performance based on the type of fiber and DML used; for this reason, the rest of link components have been modeled by considering ideal behavior. After 100 km of fiber transmission, channels are demultiplexed and detected using a typical *pin* photodiode. The system quality and its performance, in terms of *Q*-factor, is analyzed for each transmitted channel.

The *Q* factor is the signal-to-noise ratio at the decision point, in voltage or current units, and it is typically expressed by, [13]:

$$Q = \frac{|\mu_1 - \mu_0|}{\sigma_1 + \sigma_0} \qquad (4)$$

where μ_i and σ_i are average values and variances of the "1" and "0" values for each pattern. $Q \approx 7.03$ corresponds to a *BER* of 10^{-12}.

Fig. 8 shows the *Q*-factor dependence on the power of the channel for the wavelength channel centered at 1551 nm.

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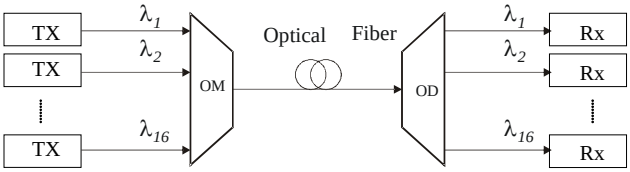
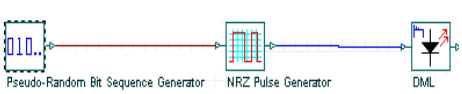
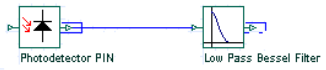
Independently of the *Case* and wavelength channels, the *Q*-factor always presents a maximum value for a specific DML output power. This behavior demonstrates the existence of an *optimum channel power* to be considered during the system design. As can be seen from Figure 8, this behavior is the same for all analyzed *Cases* but it is a result of different phenomena. For *Cases* which use adiabatic chirp dominated DML-A lasers (*A* y *B*), the Q_{max} value is reached at 0.3-0.46 mW, independently of the fiber type. In this case, the result of the interaction of the dispersion with the specific chirp characteristics produces a high intensity spike, at the front of the pulses for transmission along a fiber with positive dispersion (SMF) and, at the end for negative dispersion (NZ-NDSF) fibers. The absolute value of the dispersion (and not its sign) will play a major role in the transmission performance.



a) 16-channel WDM system



b)Tx



c) Rx

Figure 7. a) Schematic part of the complete arrangement set up; b) transmission side and c) reception side

Then, the performance corresponding to transmission along a SMF fiber will be worse than that corresponding to transmission through a NZ-NDSF fiber because of the larger absolute value of the dispersion. For small powers, the *Q*-factor increases with the power channel, $P_{ch.}$ because a large amount of power reaches the detector. For higher P_{ch} the optical pulse deformation arising from chirp induced by the DML becomes too large and causes an error in pulse reconstruction [14].

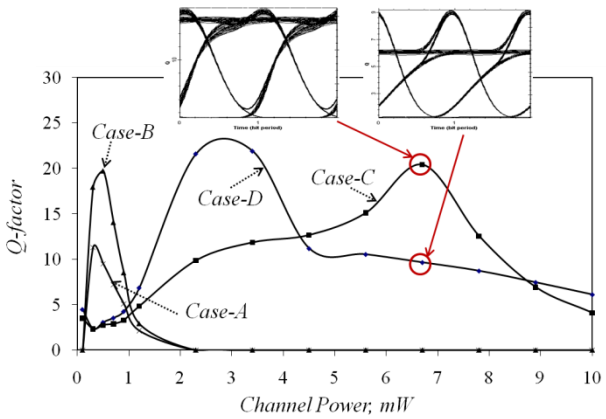


Figure 8. *Q*-factor dependence on channel power for λ = 1551 nm.

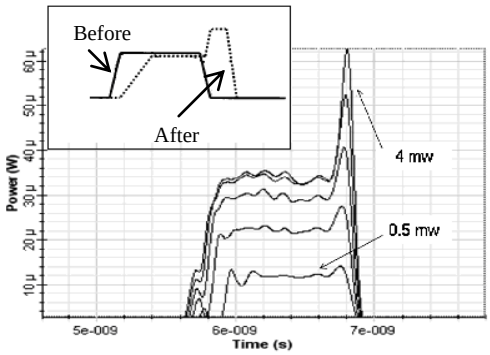


Figure 9. Shapes of optical pulses for different DML-A output powers, after transmission through a negative dispersion fiber.

Fig. 9 represents the power waveforms for five different optical output powers (from 0.5 to 4 mW) after transmission through a NZ-NDSF fiber. As can be seen, the increment of P_{ch} will result in a higher intensity spike at the trailing edge of the pulse. As a consequence the eye pattern after transmission will be severely closed. In *Cases* which use transient chirp dominated DML-T lasers, the Q_{max} value occurs for an output power of ~ 6.7 mW for *Case-C*, or the Q_{max} is around 2.3-3.4 mW in *Case-D*.

In DML-T, the wavelength shift by laser transient chirp is a blue shift during the pulse rise time and a red shift during the pulse fall time; exactly the opposite effects takes place with SPM (Self-phase-modulation). Therefore, the optical pulse chirped by direct modulation is compressed in fibers with negative dispersion, while that chirped by SPM is compressed in fibers with positive dispersion (SMF).

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Therefore, we can conclude that systems using an SMF fiber can have a similar or better performance to those systems that use an NZ-NDSF fiber if the DML is transient chirp dominated and its output power is properly chosen.

IV. 32-CHANNEL WDM SYSTEM

In order to analyze the influence of the number of channels on the relation between P_{ch} and Q_{max} in a WDM system, simulations with a number of channels from 1 to 32 have been carried out, using the same schematic arrangement set up shown in Fig. 7. The channel wavelengths are between 1531 and 1591 nm. Some channels were located at compatibles frequencies with CWDM ITU-T grid in order to, in the future, extend this work to whole useful fiber optic spectral range (1271-1611 nm). For every case, the *Q*-factor shows a maximum value for a given optical output power.

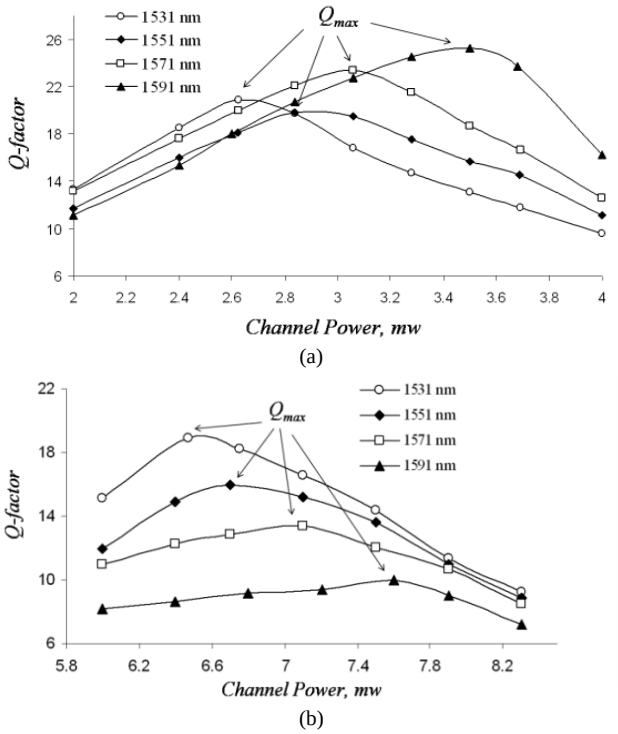

Figure 10. *Q*-factor versus channel power for channels centered at 1531, 1551, 1571 and 1591 nm, respectively, for a 32-Channel WDM system using (a) DML-T/SMF and (b) DML-T/NZ-NDSF.

As an example, if a 32-Channel WDM system is designed using DML-T and SMF with channel powers equal to the optimum $P_{ch.}$ all 32 channels will have a *Q* higher than 8, corresponding to a BER lower than 10^{-15}. In the contrary, if a system design with equal channel power is used some of channels (higher dispersive channels) will fail after propagation along a SMF fiber.

Fig. 10 shows the *Q*-factor versus channel power for channels centered at 1531, 1551, 1571 and 1591 nm, respectively, for a 32-Channel WDM system using (a) DML-T/SMF (*Case-C*) and (b) DML-T/NZ-NDSF (*Case-D*). In both cases, each channel presents a different optimum P_{ch}. Then, by the $P_{ch.}$ control of each channel it is possible to reach the Q_{max} and an enhancement of the WDM system performance can be achieved. This optimum P_{ch} is the conclusion of the following considerations: for low power levels, below the optimum power, the *Q-factor* increases with P_{ch} because a larger amount of power reaches the detector and the performance enhancement will be dependent upon the level power, so that the greater the power in the receiver, higher system performance is obtained; while, for P_{ch} higher than optimum power, the chirp increases with level power and it causes greater frequency shift and linewidth broadening which results in an error in pulse reconstruction.

Optimum P_{ch} depends on fiber optic dispersive characteristics as well as on link length. The optimum channel powers (P_{ch} to reach Q_{max}) are plotted as a function of dispersion in Fig. 11 (open circles in the case of transmission through positive dispersion fiber and solid circles for negative dispersion fiber).

In Figure 11, the results for a channel centered at 1551 nm as well as a potential CWDM channel centered at 1391 nm, after transmission over 100 km of SMF and NZ-NDSF fibers, are shown. Attenuation dependence with wavelength was taken into account in the calculation of optimum P_{ch} and, in all cases, a $Q_{max} > 7$ (BER < 10^{-12}) was obtained.

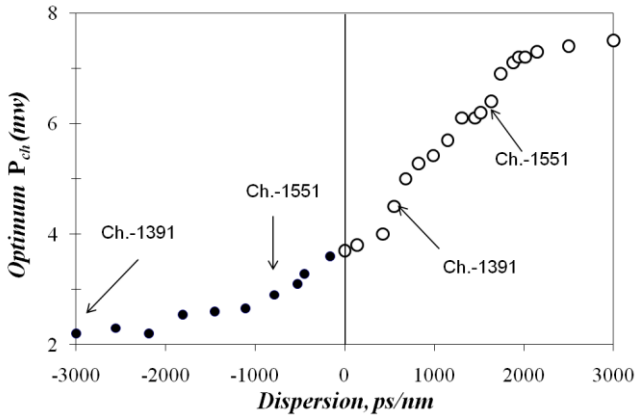

Figure 11. Comparison of Optimum Channel Power versus accumulated dispersion for a positive dispersion fiber (open circles) and negative dispersion fiber (solid circles)

A mathematical expression that fits this curve would be very useful, since it would make an estimation of the power value to fix the laser output for each channel. For this reason, using the Matlab simulation tool, this function has been estimated from a polynomial expression of degree 4 (Fig. 12):

$$f(x) = ax^4 + bx^3 + cx^2 + dx + e \quad (5)$$

$a = -3.482 \cdot 10^{-14}$; $b = -6.588 \cdot 10^{-11}$; $c = 4.202 \cdot 10^{-07}$;
$d = 0.001435$; $e = 3.673$

where x is the dispersion accumulated across the link.

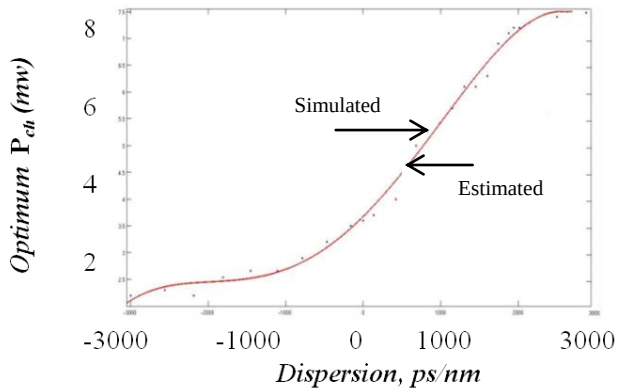

Figure 12. Estimated curve for optimum channel power

V. CONCLUSIONS

The performance of fibers relative to positive or negative dispersion characteristics is discussed for the case of directly modulated lasers. The effects of chirp and fiber nonlinearity in a directly modulated 2.5-Gb/s transmission system have been investigated by simulation. We can conclude that systems using SMF fiber can have a similar or better performance to those systems that use NZ-NDSF fiber if the DML is transient chirp dominated and its output power is properly chosen. From Fig. 8 we can conclude that DMLs transient dominated chirp are better controlled to compensate dispersion in both SMF and NZ-NDSF fibers.

Since the magnitude of chirp can be changed by controlling the optical power, the balance between SPM, chromatic dispersion and laser transient chirp can be controlled. Therefore, an optimum compensation condition can be achieved by controlling the optical DML output power. To analyze the effectiveness of this technique for WDM systems, simulations varying the number of channels from 1 to 32 have been carried out and checking. In every case, *Q*-factor shows a maximum value depending on the optical power of each channel and accumulated dispersion. This maximum value decreases depending on the number of channels used. Also, we have shown that the control of the channel power could improve the performance of each channel as well as the whole WDM system.

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REFERENCES

[1] H.S. Jang and Y.G. Chung, “Directly modulated CWDM/DWDM system using negative dispersion fiber for metro network application”. Optical Fiber Communication Conference, OFC 2004, vol. 1, WG5.

[2] J.A.P.Morgado and A.V.T. Cartaxo, ”Dispersion Supported Transmission Technique: comparison of performance in anomalous and normal propagation regimes”, IEE Proc. Opto-Electr., vol. 148, pp.107-116, 2001

[3] J.A.P. Morgado and A.V.T. Cartaxo, “Directly Modulated Laser parameters Optimization for Metropolitan Area Networks Utilizing Negative Dispersion Fibers". IEEE J. Select. Topics Quantum Electron., vol. 9, no. 5, pp. 1315 – 1324, 2003

[4] Tomkos et Al., “Demonstration of negative dispersion fibers for DWDM metropolitan Area networks”, IEEE J. of Select. Top. in Quan. Elec. vol. 7, no. 3, pp. 439-60, 2001

[5] Krelik P. “Characterization of semiconductor laser frequency chirp based on signal distorsion in dispersive optical fiber". Opto-electronics review. vol. 14, no.2, pp. 123-128, 2006

[6] Zhang Tao, Zhu Ning, Hua Zhang, and Bang Hong “Measurement of Chirp Parameter and Modulation Index of a Semiconductor Laser Based on Optical Spectrum Analysis”, IEEE Photon. Technol. Lett., vol. 19, issue 4, pp. 227-229, 2007

[7] P.J.Corvini and T.L.Koch. “Computer simulation of high bit rate optical fiber transmission using single-frequency lasers”, J. Lightw. Technol. Vol. 5, pp. 1591–1595, 1987

[8] C. H. Henry “Theory of the linewidth of Semiconductor Lasers”. IEEE J. Quantum Electron., vol.18, pp. 259 – 264, 1982

[9] C. del Río, P.R. Horche, and A. M. Minguez, “Analysis of Linewidth and Extinction Ratio in Directly Modulated Lasers for Performance Optimization in 10 Gbit/s CWDM Systems”. Optics Com., vol. 283, Issue 15, pp. 3058-3066, 2010

[10] G.P. Agrawal: Fiber-Optic Communication System. A John Wiley & Sons Ed., 2010.

[11] C. del Río, P.R. Horche, and A. M. Minguez, “Effects of Modulation Current Shape on Laser Chirp of 2.5 Gb/s Directly Modulated DFB-Laser”. Proc. Conf. on Advances in Circuits and Micro-electronics, pp. 51-55, CENICS 2010

[12] A. Consoli, C. del Río Campos, F.J. López Hernández, and P. R. Horche, "Transmission performance improvement of directly modulated 1.5 μm VCSEL: simulation and experiments", Proc. Conference on Ad. in Circuits, El. and Micro-electronics, , pp. 56-60, CENICS 2010

[13] Gerd Kaiser “Optical fiber Communications”. Mc Graw-Hill science, 4th Edit., 2010.

[14] Nobou Suzuki. “Simultaneous Compensation of Laser Chirp, Kerr Effect, and Dispersion in 10 Gp/s Long-Haul Transmission Systems”. J. Lightw. Technol., vol. 11. no 9, pp. 1486 – 1494, 1993

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Step-by-Step Design and EM Modeling of a 3D Solenoid-based 4 GHz Band-pass Filter (BPF) using Through Silicon Vias

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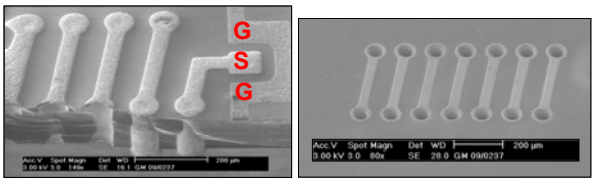
***Abstract*—In this paper, the design of an original fully integrated band-pass filter at 4 GHz using low-aspect ratio Through Silicon Vias (TSVs) is presented. Response of the filter has been simulated within a single BGA (Ball-Grid Array) package implemented on a Rogers substrate. Simulations have been performed with the help of a FEM (Finite Element Method) 3D EM (Electro-Magnetic) simulator. Prior to filter implementation, a comparison between simulated and measured data is proposed on both 3D solenoids and the package in order to calibrate the simulator and validate the simulation methodology. The obtained simulation results are successfully correlated to measurement results. Then the filter is built taking into account the previously defined building blocks (solenoids + packaging) and optimized by taking into account its global environment. The proposed solution allows a clear reduction of the filter footprint compared to discrete devices based implementation. The total area of the filter is 3.6 mm x 2.4 mm. The insertion loss and return loss at 4 GHz are about 2.6 dB and 16 dB respectively.**

Keywords - Finite Element Method, Through Silicon Via, passive integration, filtering, EM simulations.

I. INTRODUCTION

The concept of 3D packaging using TSV stacking is one of the most promising technologies. It can extend Moore's law by stacking and shortening the connection path between memory and logic [1]. Due to the increase in functional integration requirements, more and more assembly house and wafer foundries are looking into 3D TSV technology, which allows stacking of Large Scale Circuits (LSI's) thereby enabling products to be made smaller with more functionality. 3D technology realizes miniaturization up to 300-400% compared to the conventional packaging [2]. Furthermore TSVs are also relevant to develop "more than Moore" applications [3], where passive functions originally lying on the PCB (Printed Circuit Board) can be designed with the help of TSVs using original component architectures such as embedded solenoids (see Fig. 1). In that sense, distributed L, C filters based on TSVs can be investigated and implemented within interconnect dies.

Indeed, the increasing demand of the wireless communications applications requires the radio frequency (RF) receiver to be operated in multiple frequency bands so that users can access different services with a single handset. In designing the RF receivers, a band pass filter (BPF) is added to perform the filtering of unwanted signals and to pass the signal of the specific frequency from the antenna. Filters are either integrated on chip (using planar coils and Metal-Oxide-Metal (MOM) capacitors) or integrated in a hybrid application such as MCM (Multi-Chip Module) lying on a ceramic or organic substrate using a micro strip architecture.



(a) (b)

Figure 1. SEM pictures Top view (a) and bottom view (b) of the 3D solenoïds within GSG (Ground Signal Ground) pads – source IPDiA

Some well known structures have been already successfully implemented and reported [4]. For the former ones, they can suffer from their low quality factors (mainly due to the resistive losses within the planar coils) while the latter ones exhibit high performances but can deviate a lot from nominal behavior compared to silicon due to process spread. An other alternative also consists in implementing the filters on top of the carrier substrate (Printed Circuit Board for example) with the help of Surface Mounted Devices (SMDs). The main advantage of such approach is the high quality factor value that can be reached, but generally they have limited performances at higher frequencies, the total footprint is bigger and the lack of accurate and scalable electrical models limits their applications and implementation in view of a high selectivity of the signals.

In case of fully integrated filters within silicon IC processes, some passive integration dedicated processes have

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been already developed to tackle the low quality factor of the unit components. Devices are generally deposited on HRS (High Resistive Substrate) that clearly limits the effects of eddy currents [3]. Thick top metals are also implemented and copper is often used to reduce the resistive losses. Thickness up to 8 um can be considered in certain cases. Recent achievements have highlighted really good performances for band-pass filter for TV on Mobile applications [5]. For this application, coils exhibit regular planar shape, which provides a good compromise for designers between ease of layout and manufacturing and the electrical performances. On the other side, together with the emergence of new type of interconnects such as TSVs, embedded solenoid implementation within silicon or glass substrate [6] is now considered to easily build a coil-type structure. Several proposals have been done in that sense leading to very promising results [7][8]. In fact, integrated solenoids can be used to produce larger quality factor than in RF BiCMOS/CMOS planar technologies within a given footprint [9]. This increase in quality factor can be attributed to both metal thickness and the specific solenoid property of storing energy according to:

$$Q = \omega \cdot \frac{energy\ stored}{average\ power\ dissipated} \qquad (1)$$

So, in this paper, we propose to take advantage of TSVs implemented with thick patterned metals within an IPD (Integrated Passive Devices) process to design a band-pass filter at 4 GHz. The paper will be organized as follows: Integrated solenoid as well as MOM capacitance will be introduced in the first part; their performances will be presented from an electrical point of view together with their relative precision taking into account the process spread. Solenoid performances obtained from wide-band frequency 2-ports S-parameters measurements will be presented. EM (Electro Magnetic) modeling done with the help of a 3D FEM solver will be also described and compared to measurements.

As the effect of packaging plays a significant role on the device performances, the second part of this study will be devoted to the characterization of a conventional QFN package using a very single test-case. Measurement data will be then used to calibrate the EM simulator.

In the third part of this paper, we report the design methodology and the simulation results for a 4 GHz band-pass Chebyshev filter done using TSVs.

II. 3D INTEGRATED SOLENOIDS

A. Solenoid geometry description

We have already reported the fact that 3D TSV based solenoid can be implemented within a silicon die [9]. This process has been developed by IPDiA (formally NXP semiconductors). Our 3D solenoid uses the thickness of the silicon as the third dimension. Indeed each turn of our solenoid is fabricated with the TSV as the vertical sides. A front side and back side metallization of the bulk wafer leads to connect the top and the bottom tracks, thanks to the TSV, allowing creating loops embedded within the silicon. Thereby we obtain a square section 3D solenoid architecture. On the top side of the silicon, a second level of metal is also used to realize MOM capacitors with a density of 100 pF/mm^2.

Copper is deposited onto front and back sides of a 300 µm depth high resistivity silicon substrate (HRS) according to a pattern defined in Fig. 2. The vias are partially filled with the same metal on the external sides as highlighted by the SEM (Scanning Electron Microscopy) picture in Fig. 1b. Consequently N-turns 3D solenoids consist of N elementary spirals placed side by side and connected in the direction of the pitch between two consecutive vias. Due to the TSV technology process, parameters such as via diameter and via height are fixed and so can not be modified. In our case, the aspect ratio AR (height/diameter) is equal to 4. To avoid mechanical stress, the pitch between two vias is set to a minimum value equal to 125 µm. Nevertheless the dimension of the metal tracks in front and back sides can be modified in order to improve the intrinsic component electrical characteristics as suggested by [10]. Hence the solenoid is defined according to its number of turns N, its width Dy and the metal track width W (that can be different between top and bottom traces). A change in the metal tracks width will also impact the spacing SP between two consecutive metal tracks.

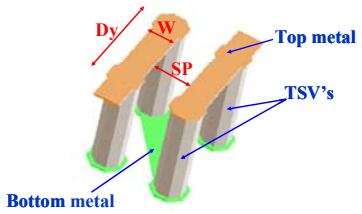

Figure 2. Synoptic representation of 2 turns 3D solenoid (silicon bulk is not represented on this picture)

B. Solenoid measurements

To support our theoretical investigations, solenoids with 1 to 5 turns were designed and grown on silicon. Then the designed test-case inductors have been placed within conventional GSG pads (Fig. 3) and measured using a network analyzer PNA8364B from Agilent Technologies, with high frequency micro-probes. Full two ports S-parameters were performed for each device up to 20 GHz. During the RF characterization, the wafer was stacked to a grounded chuck to ensure a global reference ground to the wafer, the network analyzer and the micro-probes. If no precautions are taken, a short circuit appears between the grounded chuck and the bottom metal tracks of the wafer. As a consequence, a sheet of glass fiber (~100 µm thick, εr = 4.5) has been placed between them. For each measured devices, self-inductance value and quality factor have been extracted on five crystals. In [9], we have already shown that the self-inductance variation versus the number of turns N was really close to a linear law, suggesting a very low inductive coupling between the loops. This is due to the

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minimum pitch defined by the process that is relatively large (=125 µm). As a consequence, the capacitive coupling is also reduced, which allows using the inductors at several GHz. Furthermore, due to the typical geometry of the solenoid, the quality factor is improved up to several GHz compared to classical planar IC coils either in CMOS or BiCMOS processes. A physical lumped elements electrical model was proposed also in [9] to simulate the device behavior versus frequency. This model is indeed really helpful to generate contour plots in order to pick-up the right solenoid parameters (N, W, Dy, SP) and thus decrease the design iterations. By the way, as any other compact model, it is not correlated to the global environment of the device (parasitic coupling, ground rails …). So in view of designing passive filters, we have developed an EM (Electro Magnetic) based model.

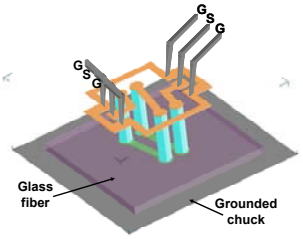

Figure 3. Illustration of the measurement test-bench used to guarantee a good ground reference together with an isolation between bottom metal traces and the chuck

C. 3D solenoid modeling

Dedicated test-cases presented in the previous paragraph have been simulated using the 3D FEM solver EMPro from Agilent. First, TSVs have been defined within the substrate stack taking into account the partial fill of the vias with copper, the barrier between the copper and the silicon bulk (to avoid copper diffusion in the silicon). Geometry of the vias is also simplified: the circular shape of the TSVs is converted to an octagonal one, in order to speed-up the mesh and thus the simulation time without losing any accuracy on the results. Bulk silicon has been described with the help of its relative dielectric permittivity (εr=11.9) and its resistivity - equal to 1000 Ω.cm. A comparison between both self-inductance value and quality factor against frequency is presented in Fig. 4. Self-inductance and quality factor values have been extracted according to the following relations:

$$L = \frac{imag\left(\frac{1}{Y_{11}}\right)}{2\pi \times freq} \quad (2)$$

$$Q = -\frac{imag\left(Y_{11}\right)}{real\left(Y_{11}\right)} \quad (3)$$

Where freq is the working frequency.

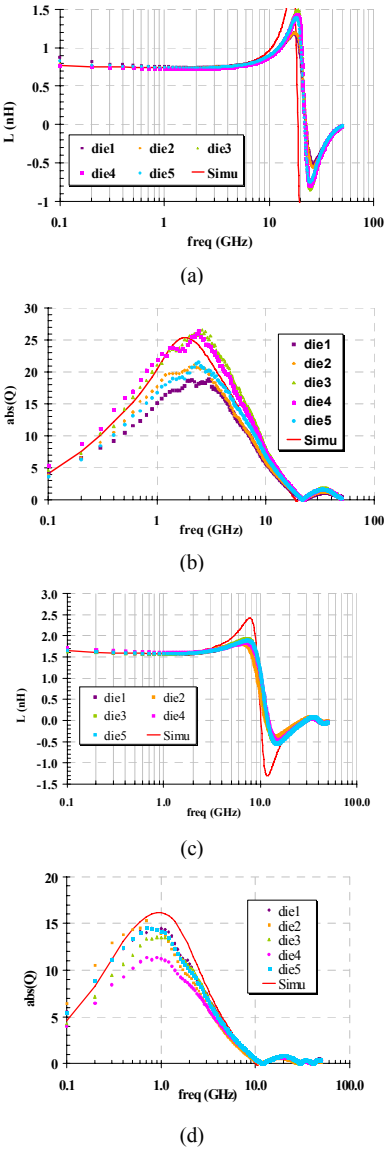

Figure 4. Comparison between measured and simulated data for 1-turn solenoïd (a): self inductance value (b) quality factor and 2-turns solenoid (c): self-inductance value (d) quality factor

From the available test-cases, a pretty good agreement is found for the self-inductance as well as the quality factor variations versus frequency. The SRF (Self-Resonant-Frequency) is also well predicted suggesting that the parallel capacitances are also well evaluated with the proposed approach. Typically, a difference of 3 % is observed on the self-inductance value and 10% on the overall variations of the quality factor. This validates our approach that will be used to design a 3D solenoid based passive filter. By the way, these measurements and simulations have been performed on-wafer without any coating on top of the substrate. In the following part of this paper, we propose to study a single test-case combining a chip, a package and a line on a board to validate our EM tool for packaging applications also.

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III. PACKAGE MEASUREMENTS AND MODELING

Indeed, the emerging applications of wireless communications require effective low-cost approaches to microwave and RF packaging to meet the demand of the commercial marketplace. In that sense, surface mountable packages and especially plastic packages are a cost effective solution for low-cost assembly and packaging. However, plastic packages, whatever their types (standard QFN or flip-chip based solutions such as BGA) contain unavoidable parasitic elements. As a consequence, development of characterization techniques for surface mounted packages is motivated by the need to predict the parasitic behavior of packages at microwave frequencies. In fact, the capability of accurately and easily characterizing packages provides a means to study and correctly model their high frequency behavior. Work in the literature relies mainly on EM simulations [11][12]. In this paper, we will present an "on-wafer" method of measuring the microwave performances of a chain containing a chip, a package and 50 Ω line on Rogers substrate. Final goal of this part is to calibrate the EM simulator (in our case EMPro from Agilent) based on this single test-case.

A. Test-case description and measurement

One of the main problems of package characterization is that the terminals of the lead-frame are not accessible without significant modification to the investigated structure. To overcome the need for this modification, we have divided the test-case into three main parts. A photograph of the test-case is provided on Fig. 5.

So the first part of the test-case is a BiCMOS (NXP in house process) silicon die containing a coplanar line. The line is designed in such a way that it allows GSG probing with conventional micro-probes from Cascade micro-tech. This line is then connected with the help of 4 bond wires (2 for the signal and 2 for each ground path) to the pins of the package. Classical 20 µm diameter gold bond-wires have been considered for this study. Then, to be able to measure the electrical characteristics of the package, it is mounted onto a RO4003C substrate from Rogers Corporation (thickness = 406 µm, εr = 3.38, tan δ = $2.7e^{-3}$). A specific coplanar access is also designed on the substrate allowing also GSG probing (bottom side of the photograph in Fig. 5).

In order to perform 2-ports S-parameters measurements, the package is then opened to access the GSG pads on the chip. Prior to measurements, a SOLT calibration is performed. Four test-cases have been measured up to 50 GHz to ensure a good reproducibility of the measurements. Results are presented in Fig. 6.

The first results clearly show a good reproducibility between the measurements. Insertion and Return loss of the total chain are respectively equal to -1.3 and -10 dB at 4 GHz, which makes such a package suitable for several GHz applications. Of course, many improvements can be considered to improve these performances (ground connection, wire loop profile, down bonds implementation). But, these techniques won't be addressed in this paper.

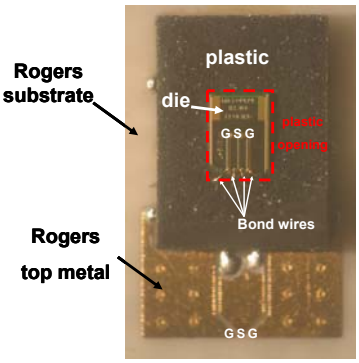
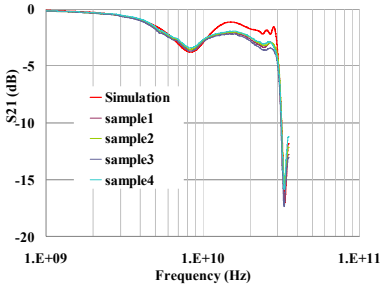
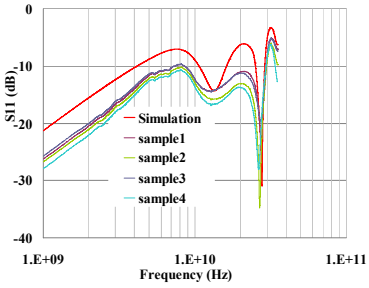


Figure 5. Photograph of the designed test-case suitable for microwave package characterization and modeling



(a)



(b)

Figure 6. Comparison between measurements and simulated data vs. frequency on the package test-case – (a) transmission parameters, (b) reflection parameter

B. Package modeling

The aim of this paragraph is to calibrate the 3D FEM solver EMPro from Agilent to correctly handle the S-parameters variations of the previously measured test-case. The 3D EM model should estimate the electrical performances of the package as accurately as possible, but on the other hand, should not be too complex for the EM simulations of more complex block. The following methodology has been applied:

- Bond wires cross-section have been first described with a square shape. Generally speaking, all round shapes should be avoided as much as possible as they are really time consuming for the simulations and the 3D mesh generation.
- Bond wire profiles were estimated based on a circle shape assumption as proposed by Alimenti and al. [13].

- Package terminals are defined into two equal steps (each is 100 µm thick) to have accurate modeling of the thick metal. One should try also to approximate their geometries with a few corner points as possible but the modifications should not affect the electrical response of the simulator.
- Coplanar ports have been used on both the chip and substrate lines.
- All dielectrics are defined with finite bricks taking into account their relative permittivity and the loss tangent or the conductivity. Plastic brick is open with an "Air" brick in order to stick as much as possible to the measurement configuration.
- The common ground reference was set to the bottom metal of the Rogers substrate

Both reflection and transmission S-parameters obtained from EM simulations are plotted on Fig. 6 together with measured data. The simulated data corroborates the measured ones with a good accuracy up to several tenth of gigahertz. To conclude this part, the EM simulation tool enables relatively accurate and complex package analysis. So based on these two previously studied test-cases (solenoid and package) the FEM solver is calibrated and ready for embedded filter design with TSVs.

IV. FILTER DESIGN AND MODELING

Based on the previous building blocks that have been studied here before (i.e., package and solenoid measurements together with EM modeling), this part will focus on the design feasibility of a 4GHz band-pass filter. Objective is to design a band pass filter with a maximum of 4dB insertion loss.

A. Schematic design

In a first time, a third order Chebyshev architecture has been considered to design the filter prototype. By the way, taking into account coefficient in [14] and applying the well known transform from low-pass to band-pass filter, lead to an inductor value in the serial electrical path that is equal to 9.13 nH. Such an inductor will have a high serial electrical resistance that will seriously affect the insertion loss of the overall filter and will also have a Self-Resonant Frequency to close to operating frequency clearly limiting its usage. So, a choice has been made to split the filter into two different parts as shown on Fig. 7 and already proposed in [5]. The first part is a 5th order low-pass filter while the second one is a 3rd order band-stop filter. Both are Chebyshev filters. By doing this, only MOM capacitors and small inductances values (i.e., 451 pH for L6 and L10) will be present in the serial path of the filters. This approach allows reaching the specified level of insertion loss.

All inductors will be designed with the help of TSVs with the same architecture as the ones presented in the first part of this document. The quality factor of inductors L6/L10 have been simulated prior to implementation and are equal to 10, which is sufficient for the targeted application. For inductors placed on the parallel paths (i.e., L1, L3, L5 and L9) their impact is really low regarding the insertion loss.

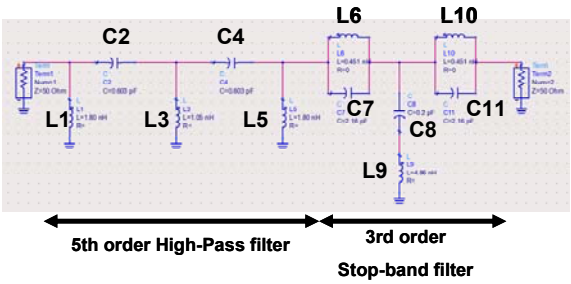


Figure 7. Schematic view of the band-pass filter considered for this study

For the capacitors, a choice has been made to use the "free" MOM capacitor offered by the process. In fact two metallization are present and can be patterned as well on the top-side of the wafer. They are separated by a classical oxide with a density of 0.1 nF/mm^2. A very low serial resistance value induced by the capacitor is expected to results from the use of two thick copper layers as device electrodes. Furthermore, very precise values of capacitance can be obtained since its relative precision is driven by the oxide thickness, which is really low (+/- 5%).

All these components will of course interact one with another leading to a change in the frequency response of the filter. That's why, a top level EM simulation is required to adjust and optimize the topology of the overall filter taking into account the interconnections as well as the ground return path.

B. Layout implementation

Special care has been taken to optimize the electrical resistance on the serial path. Wherever possible, the RF path was designed by stacking both levels of metallization connected together with the help of vias. Orientation and aspect ratio of capacitors have been chosen in such a way to minimize the resistive losses. A view of the simulated filter is shown on Fig. 8.

First order dimensions of the solenoids (Dy, N) have been deduced from the analytical model provided in [9]. The value of the ground path inductance (metal tracks + bumps) is then taken into account as they participate to the self-inductance value from the RF path to the ground (inductors L1, L3, L5 and L9). The metal track inductances have been calculated in reference to partial inductance concept proposed by Ruehli and Zhong [15][16]. Electrical parameters of the bumps have been evaluated by calculation and single EM simulations as proposed in [17].

LC tanks (L6, C7 and L10, C11) in the stop-band filter have been realized with one-turn solenoids. Then prior to top simulations, each solenoid of the filter is placed with care in order to avoid as much as possible coupling between them. Typically the maximum space is considered, and an orientation of 90° between each inductor is applied to minimize magnetic coupling. Dimensions of the whole filter are 3.6x2.4 mm^2 and clearly outperform conventional microwave structures such as hairpin filter for similar application [18]. The full structure is then simulated within

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the package with the bump connection to the Rogers substrate. Results are presented on Fig. 9.

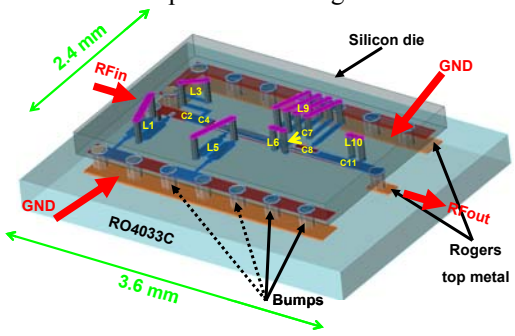

Figure 8. Top view of the simulated band-pass filter. Plastic of the package is not represented on the picture for clarity reason

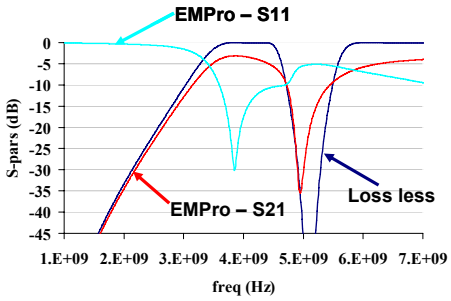

Figure 9. Simulations results of the proposed filter. Dark blue line corresponds to loss-less schematic filter simulated with ADS© schematic

From the available results, the filter exhibits insertion and return loss of 2.6 and 16 dB respectively. Insertion losses are clearly within the specifications even if they are higher than classical micro strip filters. The main contributions to the insertion losses are both inductors L6 and L10 for whom electrical resistance increases very fast with the frequency. This approach gives indeed good results in case of moderate loaded Q (few units) but won't be accurate in case of narrow fractional bandwidth where higher loaded Q-factors are required. For these very specific applications classical micro strip filters deposited on low loss substrates such as ceramic should be considered. TSVs can be used to build compact filtering function up to several GHz.

V. CONCLUSION

This paper reports a novel approach based on TSVs to integrate and miniaturize band pass filter for L and S-band applications. This kind of approach is very interesting for moderate loaded quality filter devices. It can be used within hybrid systems where passive functions are combined with improved interconnections in order to obtain high performance devices. A simulation methodology based on a step by step calibration of the FEM tool and measurements on single 3D structures is described. It allows at the end simulating the filter in its packaging environment. From the simulation results, we have demonstrated the feasibility of TSV based BPF with insertion loss of about 2.6 dB at 4 GHz.

VI. REFERENCES

[1] P. Benkart, "3D Chip Stack Technology Using Through-Chip Interconnects", IEEE J. Design and Testf of Computers, vol. 22, n°6, pp. 512-518

[2] S.W. Yoon, D.W. Yang, J.H. Koo, M. Padmanathan and F. Carson, "3D TSV Processes and its Assembly/Packaging", Proc of IEEE International Conf. on 3D System Integration 2009, 3DIC 09, pp. 1-5.

[3] F. Murray, F. Le Cornec, S. Bardy, C. Bunel, Jan F.C. Verhoeven, F.C.M. van den Heuvel, J.H. Klootwijk and F. Roozeboom, "Silicon Based SiP: a new technology platform supported by very high quality passives and system level design tools", Proc. of 7th Silicon Monolithic Integrated Circuits in RF 2007, SiRF 07, pp. 149-153.

[4] Thomas H. Lee, "Planar Microwave Engineering", Cambridge University Press, 2004.

[5] C. Boucey, "Conception et Réalisation de Filtes Intégrés sur Silicium pour la TV on Mobile, Proc of Journées Nationales Micro-Ondes 2007, JNM 07, pp. 1-4

[6] V. Sridharan, "Design and Fabrication of Bnadpass Filters in Glass Interposer with Trhough-Package-Vias (TPV)", Proc. of IEEE ECTC, June 2010, pp. 530-535.

[7] Z. El Abidine and M. Okoniewski, "High-Quality Factor Micromachined Toroid and Solenoid Inductors", Proc of European Microwave Integrated Circuit Conference 2007, EuMIC 07, pp. 354-354.

[8] F. Hettstedt, H. Greve, U. Schurmann, A. gerber, V. Zaporojtchenko, R. Knockel, F. Paupel and E. Quandt, "Toroid Microinductors with Magnetic Nano Composite Cores", Proc of European Micowave Conference 2007, EMC 07, pp. 270-273.

[9] M. Duplessis, O. Tesson, J.R. Tenailleau, F. Neuilly, P. Descamps, " Physical Implementation of 3D Integrated Solenoids within Silicon Substrate for Hybrid IC Applications ", Proc. of European Microwave Conference 2009, EMC 09, pp. 1006-1009.

[10] O. Tesson, "High Density Inductor, Having High Quality Factor", Patent WO 2009/128047, 2009.

[11] I. Kelander, A.N. Arslan, L. Hyvonen, S. Kangasmaa, "Modeling of 3D Packages using EM Simulators", Proc of 8th IEEE Workshop on Signal Propagation on Interconnects, 2004, SPI 04, pp. 186-186.

[12] R. Jackson, "A Circuit Topology for Microwave Modeling of Plastic Surface Mount Packages", IEEE Trans. Microwave Theory Tech., vol. 44, pp. 1140-1146, July 1996.

[13] F. Alimenti, P. Mezzanotte, L. Roselli and R. Sorrentino, "Modeling and Characterization of the Bonding-Wire Interconnection", IEEE Trans. Microwave Theory Tech., vol. 49, n°1, pp. 142-150, January 2001.

[14] A.I. Zverev, "Handbook of Filter Synthesis", Wiley Inter-Science, 1967.

[15] A.E. Ruehli, "Inductance calculations in a complex integrated circuit environment", IBM J. RES. Develop., pp 470-481, september 1972.

[16] G. Zhong and C. Koh-Koh, "Exact closed form formula for partial mutual inductances of on-chip interconnects" Proc. of the 2002 IEEE International Conference on Computer Design, ICCD02, pp. 1349-1353.

[17] O. Tesson, S. Jacqueline, M. Duplessis and P. Collander, " Hybrid Integration of a Decoupling System up to 6 GHz – 3D Silicon Based IPD Combined with Local Interconnect Modeling ", Proc. of International Microelectronics and Packaging Society, IMAPS Nordic 2009, pp. 45-50.

[18] D. Brady, "The Design, Fabrication and Measurement of Microstrip Filter and Coupler Circuits", High Frequency Electronics, pp. 22-30, july 2002.

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Comparison of Three Impedance Analysers Implemented on FPGA Circuits

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***Abstract*— In this paper, we present three different methods we have developed for the design of an electrical impedance analyser implemented on an FPGA board. We describe in the first part the general principle of the methods : Ratiometric Measurement, Feedback Voltage Control and Adaptive Parametric Modelisation. In order to test and to compare the performances of each approach, the Hardware In the Loop strategy has been used. We present the steps from the mixed simulation using Matlab DSP Builder, which leads to the FPGA implementation. We investigate the limits and advantages for each method. The impedance analysis results of a model of an audio piezo transducer (7 kHz) are presented. The amplitude accuracy is less than 3 % and the analysis duration from 5 kHz to 10 kHz is about 54.5 ms for the first two methods.**

Keywords - electrical impedance spectroscopy; piezoelectric transducer; FPGA; DDS; Hardware In the Loop.

I. INTRODUCTION

The electrical impedance spectroscopy (EIS) applied to piezoelectric sensors and systems is very often used. It is commonly applied in non-destructive testing (NDT) [1][2]; to perform physical measurements [3]; biological measurements [4] or for the diagnosis of transducers [5]. In practice, the EIS requires heavy, bulky and expensive analyzer, (i.e., Hioki model IM 3570 : 5 MHz, 6 kg, 10 k$, Agilent model 4294A : 110 MHz, 25 kg, 40 k$) . To avoid these disadvantages, several research teams have investigated from 2004 on the design of implementable EIS on a light and low cost embedded system.

Various methods have been proposed. Petersen [6] designed a digital low power EIS device with an accuracy of 0.001%. The system includes an electrical bridge with two arms and a digital synchronous demodulator. One of the arms corresponds to the unknown impedance. The bridge is balanced by a least mean squares (LMS) algorithm. This method is not suitable when the impedance changes fastly and it is not implementable in a portable device.

Lewis et al. [7] have developed a cheap system for impedance spectroscopy with a frequency band between 700 kHz and 20 MHz. The excitation of the piezoelectric transducer is carried out with a pulse generator. The electrical impedance is then determined by a fast Fourier transform performed offline using the Matlab program.

Yang et al. [8] have designed a portable device whose principle is inspired by the traditional ratiometric method. For good accuracy, the device requires three successive algorithms of calibration.

Finally, Hamed et al. [9] have proposed and implemented on an FPGA target an impedance measurement method that does not require current measuring in the tested dipole. This method is based on feedback control of the excitation voltage.

In this paper, we present the implementation of three different EIS methods on an FPGA board. These methods are then applied to the analysis of the complex impedance Z of the same dipole.

In the first part, we present the principle and the equations of each method.

The second part is devoted to the digital architectures. The diagrams are described by the Altera-DSPBuilder tool. This allows the design and the implementation directly on the FPGA target from Matlab-Simulink.

In the last part, the impedance measurements of a Butterworth van Dycke dipole which simulate an audio piezo transducer, are analyzed and compared.

II. THE EIS TESTED METHODS

A. *Ratiometric measurement (RM)*

The principle of this methode is shown in Fig. 1

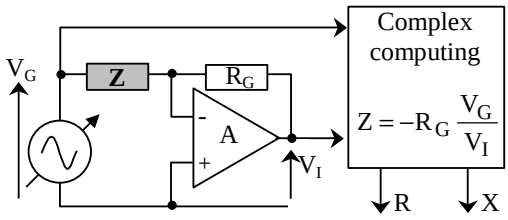

Figure 1. Ratiometric measurement of impedance

In this scheme, Z = R + jX is the unknown impedance, R_G is the reference resistor connected in series with Z.

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The output voltage of the operational amplifier is

$$V_I = -\frac{R_G}{Z} V_G \quad (1)$$

This determines the impedance Z by

$$Z = -R_G \frac{V_G}{V_I} = -R_G \left|\frac{V_G}{V_I}\right| e^{j\varphi} \quad (2)$$

where φ corresponds to the phase shift between the signals V_G and V_I

The computing block has two complex amplitude and phase detectors performed by quadrature demodulation

B. Feedback Voltage Control (FVC) method

In this system (Figure 2), a sinusoidal voltage generator V_G with an output resistance R_G is used to excite the tested dipole. The generator sweeps the desired frequency band. The voltage V_D applied to the dipole is regulated at a constant amplitude whatever the frequency is. For this reason, the variable resistor R_G is controlled in real time by a proportional-integral controller. The value of R_G and the phase φ between V_G and V_D are used to determine the complex value of Z.

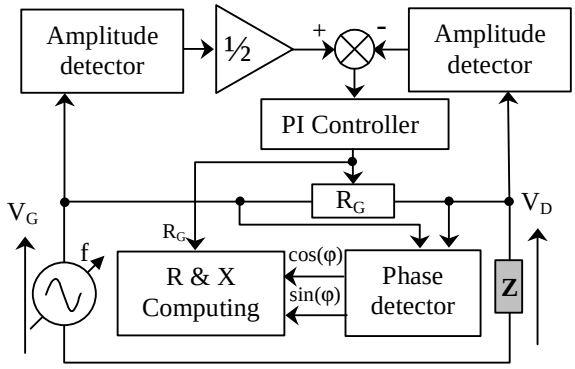

Figure 2. FVC method developed by Hamed and al.

The phase φ between V_D and V_G is determined by synchronous detection.

Real and imaginary parts of Z are determinated from φ and R_G at each frequency by

$$R = \frac{0.5\cos(\varphi) - 0.25}{1.25 - \cos(\varphi)} R_G$$
$$X = \frac{0.5\sin(\varphi)}{1.25 - \cos(\varphi)} R_G \quad (3)$$

C. Adaptive Parametric Modelisation (APM)

1) Principle

This model based method is represented in Figure 3. The dipole is considered as a system whose input is the voltage V and output is the current I. The transfer function of the dipole is then the admittance Y = 1/Z. An adaptive filter models in real time the dipole excited by a white noise. The spectral range is determined by the correlation time T_c of the white noise.

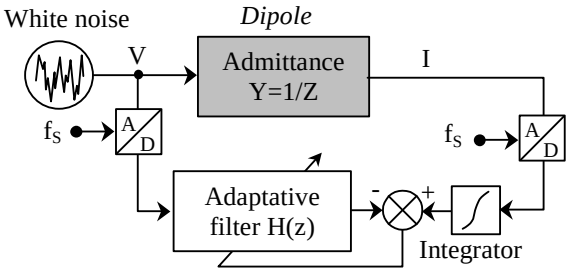

Figure 3. Adapatative parametric modelisation

The filter coefficients are identified with a classical LMS gradient algorithm.

This approach requires the "a priori" knowledge of the function Y(s) where s is the Laplace variable.

In this work, we are interested in the resonant dipole represented by a Butterworth van Dycke (BVD) structure (Figure 4). This structure corresponds to many transducers. It has a resonance frequency for which Z is minimal and a antiresonance frequency for which Z is maximal. So it is well suited to measure the accuracy of n impedanceanalyser.

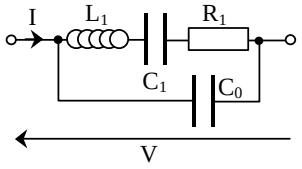

Figure 4. Butterworth van Dyck model

The admittance of this structure is

$$Y(s) = \frac{L_1C_0C_1s^3 + R_1C_0C_1s^2 + (C_0 + C_1)s}{L_1C_1s^2 + R_1C_1s + 1} \quad (4)$$

This admittance has a global capacitive behaviour. To reduce the risk of divergence of the gradient algorithm, Mayer et al. [10] suggest to carry out an integration of Y(s). This way standardizes the admittance modulus outside the resonance zone and reduces the system order.

2) Adaptive filter

It is possible to exploit a model of adaptive finite impulse response filter (FIR). In this case good resonance tracking requires the use of a high order transverse structure. That is why we use a recursive adaptive structure. His general transfer function H(z) is

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$$H(z) = \frac{b_N z^{-N} + \cdots + b_1 z^{-1} + b_0}{a_N z^{-N} + \cdots + a_1 z^{-1} + 1} \qquad (5)$$

where z is the variable of the Z-transform, N is the order and b_j, a_i are the coefficients of the filter.

III. FPGA IN THE LOOP IMPLEMENTATION

The design and implementation of digital architectures on FPGA target requires specific development tools.

Initially, the complete system is modelled under Matlab/Simulink. Indeed, the Mathworks and Altera companies have developed jointly software tools for fast FPGA prototyping.

- The analogue part is described with the SimPower System toolbox (Simulink).
- The digital part is described with DSPBuilder toolbox (Altera).

In a second step, the tool "Signal Compiler" of DSPBuilder generates the VHDL code of the digital architecture, which is implemented on the FPGA circuit.

Finally, with the hardware in the loop (HIL) simulation, the FPGA architecture is tested in a virtual environment in, which the analogue components are modelled [11].

In Figure 5, we illustrate the design steps of the FPGA in the loop prototyping approach.

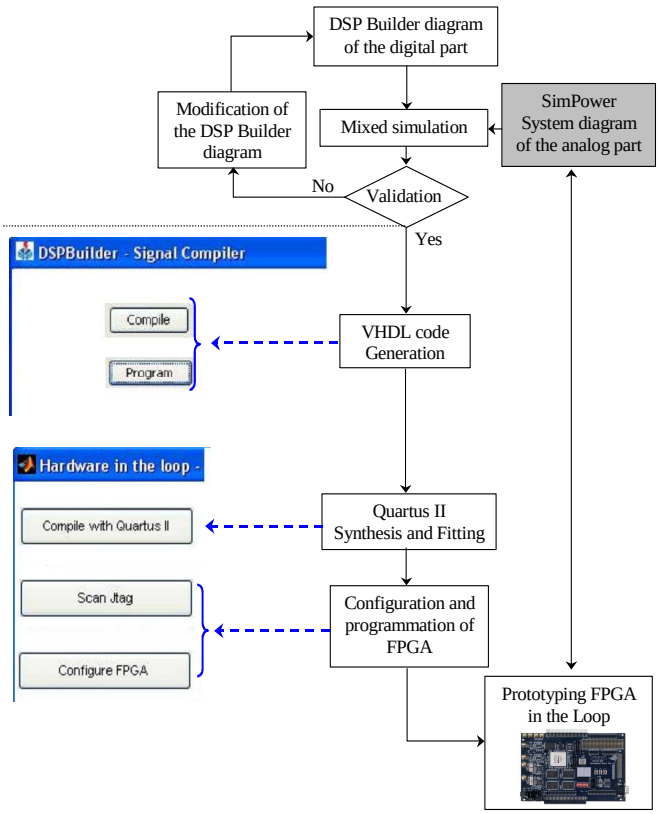

Figure 5. The steps of prototyping an FPGA in the loop

A. FPGA in the loop prototyping for the RM method

For this method of EIS measurement, we have used voltage and current measurement blocks and RLC blocks from the SimPower System library in order to simulate the dipole. These components constitute the analogue part of the system (Figure 6). The digital part contains two rectifiers, two low-pass filters, one divider and one direct digital synthesizer (DDS) to generate the sinusoidal signal with frequency sweeping.

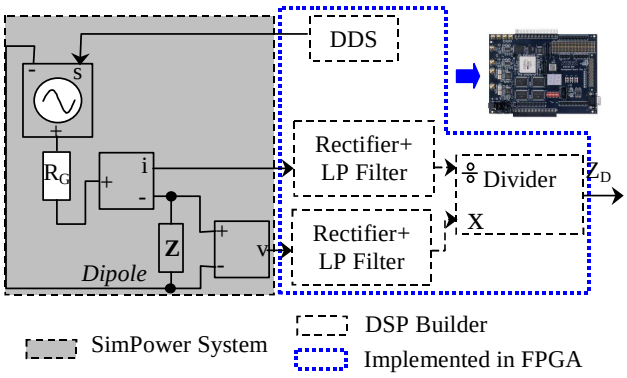

Figure 6. HIL scheme of the radiometric method

B. FPGA in the loop prototyping for the FVC method

Here, we don't need a current measurement, we only use the voltage V_D of the dipole in order to regulate it at $V_G/2$ by feedback control (Figure 7). This choice allows to have the best sensibility $\frac{dV_D}{d|Z|}$.

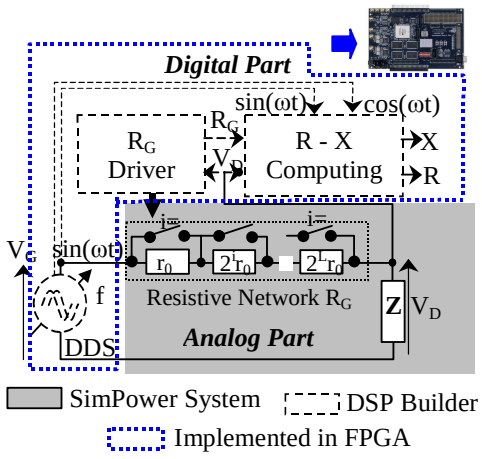

Figure 7. HIL scheme of the FVC method

C. *FPGA in the loop prototyping for the APM method.*

In this method, we must measure the voltage and the current of the tested dipole. The excitation signal is a white noise whose correlation time is T_c (Figure 8).

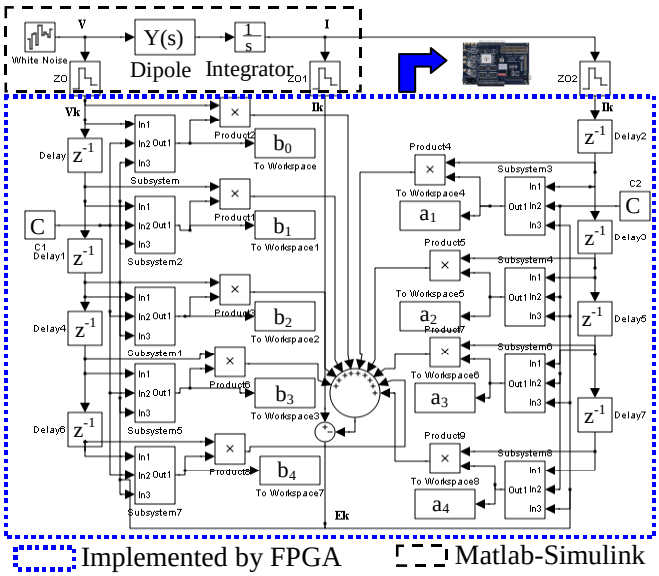

Figure 8. HIL scheme of the adaptive parametric modelisation

The coefficients a_i and b_j are updated using the gradient algorithm

$$b_j(k) = b_j(k-1) + C_1 V_{k-j} E_k \quad \text{for } 0 \le j \le 4 \qquad (6)$$

$$a_i(k) = a_i(k-1) + C_2 I_{k-i} E_k \quad \text{for } 1 \le i \le 4 \qquad (7)$$

where C_1 and C_2 are the adaptation constants
Figure 9 shows the subsystem diagram for the computation of the coefficients.

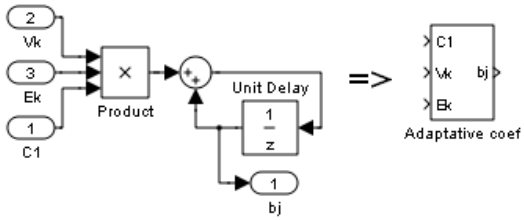

Figure 9. Adaptive coefficient subsystem

IV. RESULTS

A. *Range of frequency analysis*

The Stratix II allows to use a sampling frequency up to 100 MHz. The DDS synthesiser defines the frequency range of analysis. The structure we have adopted, can generate a sine excitation from DC to 5 MHz.

B. *Test of the three methods - Comparison*

The three methods RM, FVC and APM are used to analyse the impedance Z of a BVD structure corresponding to the dipole. The components values are given in Table I.

TABLE I. VALUES OF THE BVD COMPONENTS

L_1 (mH)	C_1 (nF)	R_1 (kΩ)	C_0 (nF)
486.4	1.1	2	4.64

These values correspond to an audio buzzer (7 kHz piezoelectric diaphragm of Murata Company).
The impedance is analysed in the range [5 kHz - 10 kHz], where the electric resonance area of the dipole is located. The RM and FVC methods use a sweeping rate of 91.7 kHz/s. Figures 10 and 11 represent the estimation curves of the real and imaginary parts (R and X) of Z obtained by each method. The curves are compared with the theoretical values R_{TH} and X_{TH} of the BVD impedance.

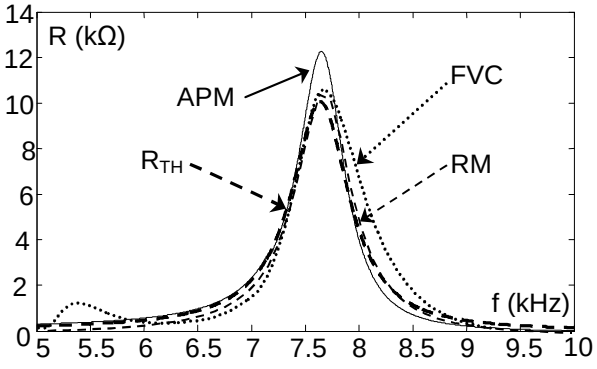

Figure 10. Real part of Z estimated by the three methods

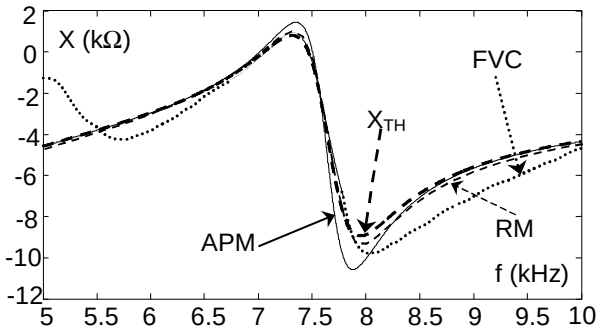

Figure 11. Imaginary part of Z estimated by the three methods

Table II summarizes the main characteristics of these measures. The accuracy is determined by comparison with the theoretical values.

TABLE II. ACCURACY AND DURATION OF THE MEASUREMENT OF Z

	Accuracy (at resonance peak)	Aanlysis duration
RM	99 %	54.5 ms
FVC	97 %	54.5 ms
APM	82 %	200 ms

C. Discussion

In this test, the RM method presents the best results. However, this method has important practical limitations.
A change in the calibre of R_S is necessary if we want to maintain a sufficient signal/noise ratio over a large dynamic range of Z. The dipole should not be grounded, this is not always possible in many situations. The FVC method allows to solve the previous limitations. In addition, the modulus of Z can be estimated from R_G. The feedback control must be stable and the analogue interface (digital resistive network) is more complicated.

The APM method is difficult to be implemented, because a setup phase must be performed. It requires to know " a priori" the dipole model in order to choose correctly the order N of the adaptive filter, the spectral density (1/Tc) of the white noise and the sampling frequency f_S

The convergence of the algorithm is achieved in practice by researching a compromise between these parameters. In our test, the best results are obtained with N = 4, $T_C = 10^{-5}$ s and $f_S = 3.10^5$ Hz.

The analysis time is directly related to the time constant of adaptation, in our case the analysis time is about 0.2 s. The impedance measurement errors are generally low but still significant near the resonance peak. When all adjustments are made, this method becomes very interesting because it provides a reference model for instantly monitoring the changes in characteristics of the tested dipole.

V. CONCLUSION

Three methods for impedance analysis that are implementable on an FPGA target were presented. The traditional ratiometric method is the simplest but requires in practice a change of range for the current measuring shunt and does not allow a grounded transducer. The 2^{th} method is an approach by automatic control of the series resistance to match the one of the transducer. This method allows the connection of the transducer to the ground without using an instrumentation amplifier. The last method is based on the parametric estimation of a model. The order of magnitude of the response time is 0.2. This method allows the determination of the impedance for any real-valued frequency thanks to the analytic model. In addition, the estimated adaptive filter model can be compared to a reference model in order to detect any drift in the transducer. However, this approach requires an "a priori" knowledge of the impedance type and a source of white noise. The presented methods were all implemented in an FPGA and some measurement results are given. A modified parametric estimation method based on the use of a pseudorandom binary sequences is under investigation.

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REFERENCES

[1] D. M. Peairs, P. A. Tarazaga, and D. J. Inman, "Frequency range selection for impedance-based structural health monitoring,". Journal of Vibration and Acoustics, vol. 129, no. 6, 2007 pp. 701–709.

[2] Bhalla. S and Soh C. K. "Progress in Structural Health Monitoring and Non- Destructive Evaluation Using Piezo-Impedance Transducers,". Smart Materials and Structures: New Research, Nova Science Publishers, Inc. , New York, 2007, pp. 177-228.

[3] Giurgiutiu. V. and Zagrai. A. N, "Embedded Self-Sensing Piezoelectric Active Sensors for Online Structural Identification," 2002.

[4] Giurgiutiu. V.and Zagrai. A."Damage Detection in Simulated Aging-Aircraft Panels Using the Electro-Mechanical Impedance Technique,". Adaptive Structures and Materials Systems Symposium, ASME Winter Annual Meeting, November 5-10, 2000, Orlando, FL

[5] D. M. Peairs, P. A. Tarazaga, and D. J. Inman, "Frequency range selection for impedance-based structural health monitoring,". Journal of Vibration and Acoustics, vol. 129, no. 6, 2007, pp. 701–709.

[6] C.L. Petersen "Low power portable device for high precision electrical impedance detection,''. *Sensa Wave technology Inc ,BC* Canada

[7] Lewis G. K., Lewis G. K, and Olbricht W., "Cost-effective broad-band electrical impedance spectroscopy measurement circuit and signal analysis for piezo-materials and ultrasound transducers,''. *Meas. Sci. Technol*., 2008, doi:10.1088/0957-0233/19/10/105102. 19, 105102

[8] Yang. Y, Wang. J, Yu. G, Niu. F, and He. P, "Design and preliminary evaluation of a portable device for the measurement of bioimpedance spectroscopy,". *Physiological Measurement* 27, 2006, pp. 1293–1310.

[9] Hamed. A., Tisserand. E., Berviller. Y., and Schweitzer. P, "Fast FPGA Implementation of an Original Impedance Analyser,". Sensors & Transducers journal, 2011, vol. 10, pp.191-205, ISSN 1726-5479, February

[10] Mayer. D,. Atzrodt. H, Herold. S, and. Thomaier. M, "An approach for the model based monitoring of piezoelectric actuators," *Computers and Structures*, vol. 86, no. 3–5, pp. 314–321, 2008.

[11] Vera. A, Meyer-Baese. U, and. Pattichis. M, "An FPGA based rapid prototyping platform for wavelet coprocessors,". *International Conference on Independent component analyses, wavelets, unsupervised smart sensors, and neural networks*, Orlando April 2007, pp. 1-10.

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Design of Reconfigurable Quad-band CMOS Class AB Power Amplifier employing MEMS Variable Capacitors in 0.18µm Technology

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***Abstract*— A reconfigurable quad-band CMOS power amplifier suitable for multi-band radiofrequency transceivers is presented. The multi-band power amplifier is a reconfigurable monolithic microwave integrated circuit designed to operate in 1.7, 1.8, 1.9 and 2.1 GHz frequency bands. The structure is a single ended one stage class AB power amplifier with tunable impedance matching network based on high Q micromachined inductors and MEMS tunable capacitors. The reconfigurable power amplifier is fully integrated in 0.18µm CMOS technology and achieves maximum output power with good efficiency over different operating frequencies. The device has a simulated maximum output power of 20 dBm and can achieve a variable gain over than 16 dB in the four operating bands with a power-added efficiency (PAE) better than 50%.**

Keywords- reconfigurable power amplifier; tunable impedance matching; RF microelectromechanical system (MEMS); CMOS-MEMS; variable capacitors

I. INTRODUCTION

As the wireless market continues to grow with the proliferation of wireless communications standards such as GSM, WCDMA, and Wimax, there is increasing demand for reconfigurable multi-band RF front-ends that meet the specifications of various standards.

Considering multi-band operation, designing reconfigurable power amplifier (PA) is required for multi-standard RF transceivers. From the cost point of view, CMOS technology is a breakthrough in competitive RF monolithic integrated circuits, allowing development of cost effective reconfigurable PA.

There are different configurations to achieve multi-band operation and many reconfigurable PAs using different approaches have been reported. The conventional multi-mode implementation consists of a combination of different PA units, designed optimally for each frequency band [1]. Although the PA module presents high performance, it needs complex structure resulting in larger circuit. The second method is a wideband approach with input and output impedance matching in wide range of frequencies [2]. However it is difficult to achieve high efficiency in all bands of interest. Compared to the two first methods, the tunable approach would avoid the use of redundant blocks of single PA and is based on adaptive matching network [3].

The introduction of radio-frequency micro-electro-mechanical systems (RF-MEMS) components have opened new perspectives to implement this ideal solution with enhanced tuning range, low loss and high quality factor Q of passive devices. The reported reconfigurable PAs based on tunable impedance matching network with MEMS switches and/or stubs have demonstrated a high output capability with good efficiency over several bands of operation [4]-[5]. However these devices require the hybrid integration of the MEMS matching network. Thanks to significant advances in CMOS-MEMS integration, reconfigurable PA fully integrated in CMOS process can be achieved.

In this work, the design of a reconfigurable quad-band class AB CMOS power amplifier with the help of MEMS variable capacitors and micromachined inductors is presented. The designed PA is fully integrated in 0.18 CMOS technology and operates in 1.7, 1.8, 1.9 and 2 GHz.

The paper is organized as follow. In next Section, the design of the class AB power amplifier is described. Section 3 presents the tunable approach with MEMS variable capacitors and Section 4 presents the simulation results. Conclusion and future work are summarized in Section 5.

II. CLASS AB POWER AMPLIFIER DESIGN

Power amplifiers have balancing parameters which, often are in conflict; thus a good linearity comes usually at the cost of efficiency. The aim is to achieve 20dBm of output power with good efficiency. A reduced conduction angle configuration is adopted and Figure 1 shows the schematic of the single ended one stage class AB power amplifier.

A. Transistor characterization & circuit design

The first step of the design consists to provide a suitable biasing point for the power amplifier to operate ideally in class AB region. The power amplifier's figure of merit such as maximum output power, gain, efficiency and linearity are related to the bias conditions. Using 0.18µm 1P6M RF-CMOS process available from TSMC, the voltage supply is fixed at 1.8 V for a maximum output voltage swing. The relative low oxide breakdown voltage in bulk CMOS technology limits the maximum drain voltage, hence the

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maximum output power. In order to increase the output power, a large transistor size required. The transistor width is chosen according to the maximum driven current capability required for 20 dBm output power. The maximum drain current is derived from [6] with a conduction angle α equals to 3π/2. The corresponding current value is 200mA which in turn leads to a transistor width of 400µm in TSMC 0.18µm RF-CMOS process. To operate in class AB, the gate is biased at 1.05 V corresponding to a DC bias current of 90 mA.

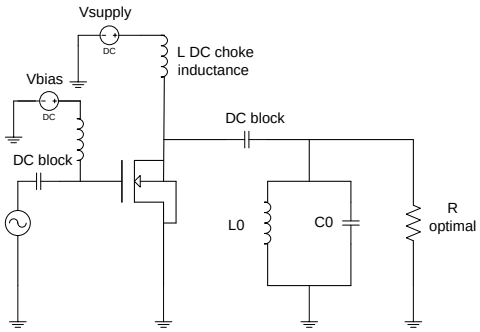

Figure 1. Schematic representation of the power amplifier

The inductor *L* is used as a DC biasing choke to set the DC level of the transistor to the supply voltage. It must have a high reactance at the operating frequency and with the assumption that its value is ten times greater than the load impedance, an inductance of 12 nH will suffice for all frequencies from 1.7 GHz to 2.1 GHz. An integrated capacitor of 10 pF is used as DC blocking capacitor.

The LC tank at the output termination is designed to resonate at $\omega_0^2 = 1/L_0C_0$ and removes higher harmonics.

B. Load pull analysis

For the given transistor size and bias conditions, the load impedance is swept in order to find the optimal load which, enables a maximum output power. To perform the load pull simulation, the input of the power amplifier is conjugately matched to the source for a maximum power transfer. Figure 2 shows the load pull simulation results for 2.1GHz frequency band.

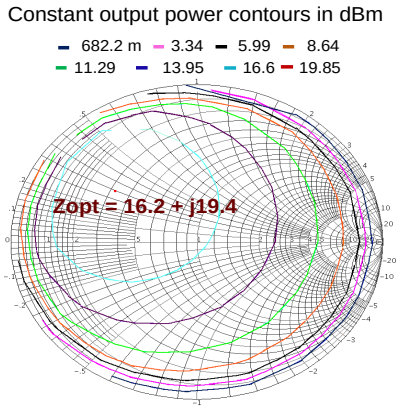

Figure 2. Load pull simulation results for 2.1 GHz.

An optimum power matching point is found after load pull analysis over the different operating bands. The maximum output power is delivered to the load with optimal impedance $Z_{opt} = 16.2 + j19.4\ \Omega$ at all frequencies of interest.

C. Input & Output matching networks

The output matching network is designed to transform the 50 Ω load antenna into optimal load impedance Z_{opt}. The matching network is also implemented in L-sections configuration as shown in Figure 3.

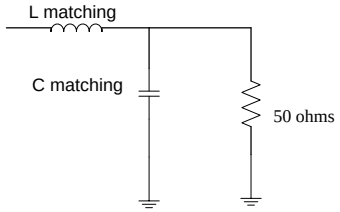

Figure 3. Fixed matching network

The required values for the impedance matching network are listed in Table I.

TABLE I. REQUIRED COMPONENT FOR OUTPUT MATCHING

Frequency	1.7 GHz	1.8 GHz	1.9 GHz	2.1GHz
C matching	2.7 pF	2.6 pF	2.4 pF	2.2 pF
L matching	3.56 nH	3.36 nH	3.25 nH	2.88 nH

The input matching network is designed to match the large signal input impedance of the transistor with the 50 Ω source impedance. The large signal input impedance is extracted at the operating frequency for a given output power such as 1 dB compression point. Table 2 summarizes the input impedance for each frequency and the required reactive components for source matching.

TABLE II. INPUT IMPEDANCE & REQUIRED COMPONENTS FOR INPUT MATCHING

Frequency	1.7 GHz	1.8 GHz	1.9 GHz	2.1GHz
Input Impedance (Ω)	221.5 + j 57.05	229 + j30	203 – j6.5	180 – j 29.8
C matching	869 fF	779 fF	763.3 fF	608 fF
L matching	9 nH	8.4 nH	7.3 nH	6.1 nH

III. TUNABLE AMPLIFIER WITH MEMS VARIABLE CAPACITORS

The reconfigurable amplifier is integrated with micromachined inductors and tunable matching sections based on variable CMOS-MEMS capacitors. The schematic of the designed circuit is presented in Figure 4.

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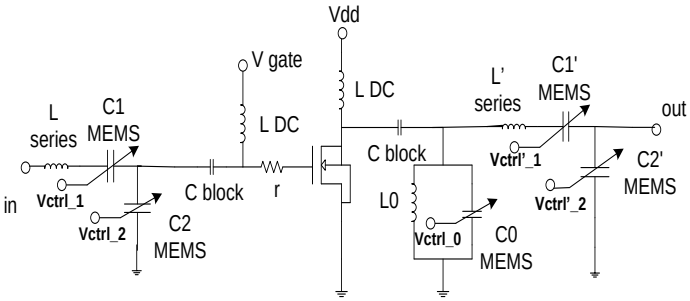

Figure 4. Schematic of the quad band reconfigurable power amplifier

A. *Tunable matching network*

The matching network is based on L-networks configuration for different operating frequencies and variable values for the inductance and capacitance. The concept of the matching network used in this design consists of implementation of the network with a combination of fixed inductors and MEMS variable capacitors as shown in the schematic diagram of the PA circuit in Fig. 4.

To achieve the required impedance both for source and load matching, series inductance of 15 nH and 12 nH are coupled to the source and load respectively with two MEMS variable capacitors actuated by DC voltage between electrodes to insure tunability over the four operating frequencies. In addition, the resonant frequency of the LC tank can be tuned by varying L_0 and C_0. In this case, a MEMS variable capacitor is employed with fixed inductance of 4.5 nH.

The required states of MEMS capacitance for impedance matching and tunable resonance frequency are reported in Table III.

TABLE III. VARIABLE CAPACITANCE FOR SOURCE/LOAD MATCHING & RESONATOR

Frequency	Source matching	Load matching	Resonator
1.7 GHz	C_1= 1.5 pF C_2= 0.9 pF	C_1'= 1 pF C_2'= 2.7 pF	C_0 = 1.95 pF
1.8 GHz	C_1= 1.2 pF C_2= 0.8 pF	C_1'= 0.9 pF C_2'= 2.6 pF	C_0 = 1.7 pF
1.9 GHz	C_1= 0.9 pF C_2= 0.7 pF	C_1'= 0.8 pF C_2'= 2.4 pF	C_0 = 1.56 pF
2.1 GHz	C_1= 0.65 pF C_2= 0.60pF	C_1'= 0.63 pF C_2'= 2.2 pF	C_0 = 1.28 pF

B. *CMOS-MEMS Variable capacitor*

The MEMS variable capacitors proposed in [7] represent a practical configuration for the tunable matching network. The MEMS variable capacitor will be fabricated by the CMOS-MEMS post-processing technique described in Figure 5. The MEMS capacitor is implemented with M3 and M5 metal layers as the bottom and top plates, respectively. An air-gap is created in between by removing interconnect metal layer M4. This CMOS-MEMS post-processing technique is developed at Centre for Integrated RF Engineering (CIRFE) [8].

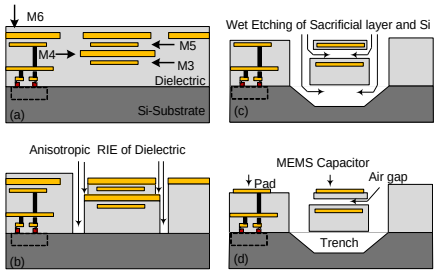

Figure 5. Post-CMOS processing steps required to integrate the MEMS parallel plate capacitors in the 0.18-µm CMOS process. (a) CMOS die after standard processing, (b) 1st RIE of CMOS dielectric layer, (c) wet etching of silicon substrate and the M4 sacrificial layer, (d) critical point drying and 2nd RIE of the CMOS dielectric layer capacitor's top plate and pads [7].

IV. SIMULATIONS RESULTS

The designed circuit was simulated using cadence Spectre. Simulations include components available from 0.18µm TSMC RF-CMOS process and device models for MEMS inductors and variable capacitor. The electrical models for micromachined inductors and MEMS variable capacitor were described in [9] and [10] respectively.

The gain for the tunable PA is over 16 dB in 1.7 GHz, 1.8 GHz, 1.9 GHz, and 2.1 GHz modes, respectively as shown in Figure 6. Figure 7 shows the frequency response of the PA from small signal simulation for the quad band of frequency.

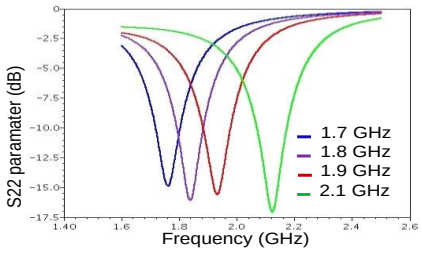

Figure 6. Simulated small signal S21 of the reconfigurable PA

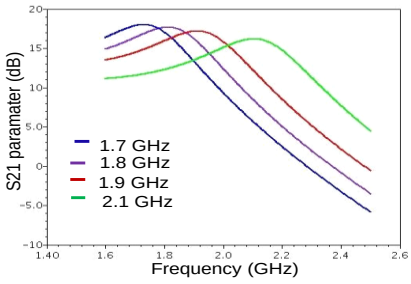

Figure 7. Simulated small signal S22 of the reconfigurable PA

The output matching network was designed to present the optimal load for maximum output power and the output return loss S_{22} of the amplifier is smaller than -10 dB for all frequencies.

Figure 8 shows the output power and PAE at various input power. As presented on plots, the linear output power is over 19 dBm in the four operating bands. The simulated PAE is 41.2%, 42%, and 41.6% in 1.7 GHz, 1.8 GHz, 1.9 GHz, and 2.1 GHz band respectively.

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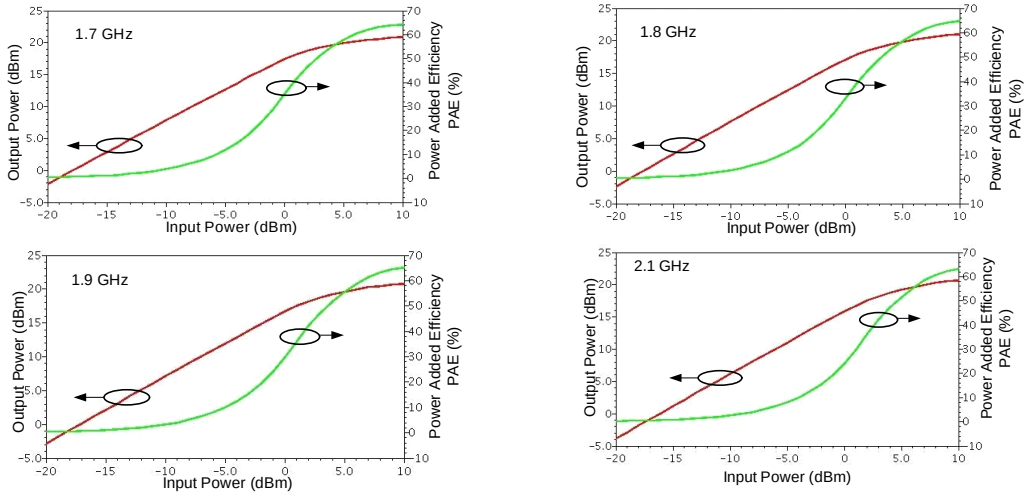

Figure 8. Simulated output power and efficiency PAE of the reconfigurable PA over the four operating band.

The designed tunable PA has been submitted for fabrication and the layout of the circuit is shown in Fig. 9.

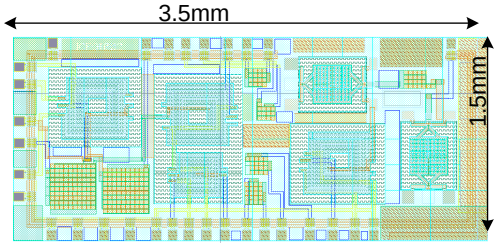

Figure 9. Layout of the proposed reconfigurable quad-band PA

V. CONCLUSION AND FUTURE WORK

In this paper, the design of a reconfigurable quad-band CMOS power amplifier (PA) operating in 1.7, 1.8, 1.9 and 2.1 GHz frequency bands is presented. The PA is fully integrated in 0.18µm CMOS technology and can be used in multi-band environment. Compared to traditional PAs, the designed device has a small circuit and works more effectively. The simulations results show that the PA can achieve a variable gain over than 16 dB with saturated output power of 20 dBm in the four operating bands and a PAE better than 50%. The proposed circuit is based on micromachined inductors and a tunable impedance matching network integrated with CMOS MEMS variable capacitors. The use of the CMOS-MEMS post processing technique allows the development of fully integrated reconfigurable RF circuits for multi-standard applications.

The designed reconfigurable power amplifier is regarded as our first prototype; hence future works will focus on the optimization of the design and the integration of next generation's PA with higher output power and suitable for multi-mode as well as multi-band application. The aim will be to develop a CMOS-MEMS reconfigurable PA according to the specifications for mobile phone standards.

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REFERENCES

[1] S. Zhang, P. Bretchko, J. Mokoro, and R. McMorrow, "On A novel power amplifier module for quad-band wireless handset applications," IEEE Trans. Microwave Theory & Tech., vol. 51, no. 11, pp. 2203-2210, November 2003.

[2] S.K. Wong, S. Maisurah, M.N. Osman, F. Kung and J.H. See, "High efficiency CMOS power amplifier for 3 to 5 GHz ultra-wideband (UWB) application," IEEE Trans. Consumer Electronics., vol. 55, no. 3, pp. 1546-1550, August 2009.

[3] W.C.E Neo, Y. Lin, X. Liu , L.C.N. de Vreede, L.E. Larson, M. Spirito, "Adaptive Multi-Band Multi-Mode Power Amplifier Using Integrated Varactor-Based Tunable Matching Networks," IEEE J. of Solid-States Circuits, vol. 41, no. 9, August 2006, pp. 2166-2176, doi: 10.1109/JSSC.2006.880586.

[4] A. Fukuda, H. Okazaki and S. Narahashi, "A Novel Compact Reconfigurable Quad-band Power Amplifier Employing RF-MEMS Switches," in 36th European Microwave Conference, January 2007, pp. 344-347, doi: 10.1109/EUMC.2006.281327.

[5] L. Larcher, R. Brama, M. Ganzerli, J. Iannacci, B. Margesin, M. Bedani, and A. Gnudi, "A MEMS Reconfigurable Quad-Band Class-E Power Amplifier for GSM Standard," 2009 IEEE 22nd International Conference on Micro. Electro. Mechanical Systems, March 2009, pp. 864-867, doi: 10.1109/MEMSYS.2009.4805520.

[6] S. C. Cripps, RF Power Amplifiers for Wireless Communication, 2nd edition, Norwood, MA 02062,Artech House, 2006.

[7] S. Fouladi and R. R. Mansour, "Reconfigurable amplifier with tunable impedance matching networks based on CMOS-MEMS capacitors in 0.18-µm CMOS technology," 2nd Microsystems and Nanoelectronics research Conference, pp. 33-36, November 2009.

[8] CIRFE, University of Waterloo, http://www.cirfe.uwaterloo.ca/.

[9] G. M. Rebeiz, RF MEMS Theory, Design, and Technology, New York, Wiley, 2003.

[10] J. Reinke, G. K. Fedder and T. Mukherjee "CMOS-MEMS Variable Capacitors Using Electrothermal Actuation," J. of Microelectromechanical Systems, vol. 19, no. 5, septembre 2010, pp. 1105 - 1115, doi: 10.1109/JMEMS.2010.206719.

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The Impact of High Dielectric Permittivity of 2-D Numerical Modeling Nanoscale SOI Double-Gate Mosfet Using Nextnano Simulator

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***Abstract*—Performance of high-k Double-Gate SOI MOSFETs is studied and compared to silicon dioxide based devices. This is achieved by computing variation of threshold voltage, swing subthreshold, leakage current and drain-induced barrier lowering (DIBL) with respect to different gate bias (V_G) when gate length (L_G) decreases. This comparison is pinpointed taking SiO_2 and HfO_2 as gate oxides. Furthermore, quantum effects on the performance of DG MOSFETs are discussed. It is observed that less EOT with high permittivity reduces the tunnel current and serves to maintain high drive current, when compared with device using SiO_2 dielectric. Our results show that the characteristics of SOI Double Gate MOSFET with HfO_2 are superior to that of a device with SiO_2 dielectric**

Keywords-high-k; **DG-MOSFET; quantum effects; nextnano3d; modeling.**

I. INTRODUCTION

Over the past years, silicon-based electronic technology has been improved through downscaling MOSFETs, resulting in higher device performance and density. However, it has been expected that this downscaling will reach its limits about the gate of 5 nm around the year 2020 or so. The 2006 edition of the ITRS (International Technology Roadmap for Semiconductors) forecasts a minimum feature size of 18 nm-node, a physical gate length of 7 nm for the year 2018 [1]. According to ITRS, a very thin gate insulator with EOT (Equivalent Oxide Thickness) less than 1 nm is required for both high performance and low power consumption CMOS devices. The thinner oxide lets more current leak between the gate and the substrate, driving up power consumption and better on- and off-state control [2]. In order to obtain a very thin EOT, we need to use high-k gate insulator such as HfO_2 which is the most promising candidate, since it possesses high dielectric constant and good thermal stability in contact with silicon [2, 3].

Another way to overcome short channel effects (SCE) is the use of multiple-gate structures on undoped SOI (Silicon On Insulator). One of these architectures is the Double Gate MOSFET (SOI DG-MOSFET) intended to control the channel very efficiently by applying a gate contact to both sides of the channel [4]. The intrinsic channel Double Gate MOSFET needs to rely solely on gate work function to achieve multiple threshold voltages on a chip due to the absence of body doping, which is efficient tool to adjust the threshold voltage in Double Gate MOSFET with doped channel [5, 6].

From the very beginning of semiconductor technology, it was thought that numerical, physics-based analysis of devices could help a great deal in their understanding. Nowadays, simulation and modeling of semiconductor devices have become one of the most important development methodologies in industry and research alike [7]. In this work we use the nextnano code to simulate a DG-MOSFET with high-k gate dielectric. This simulation tool is based on the self-consistent solution of the Schrödinger, Poisson and current equations [8, 9]. The coupled Poisson-Schrödinger system is solved by an approximate quantum charge density, which is employed inside of Poisson's equation in order to estimate the dependence of the density on the potential through Schrödinger's equation. Using this estimator the coupling between both equations is much decreased and rapid convergence is achieved. The electronic structure is calculated within a single-band or multiband k .p envelope function approximation. The included model for the carrier transport is a Wentzel–Kramer–Brillouin (WKB)-type approach also known as quantum-drift-diffusion (QDD) method, where the carriers are locally in equilibrium, charactized by a local Fermi level [10, 11].

The outline of the paper is as follows. Section II describes device structure. Section III presents some theoretical aspects. Section IV shows the simulation results using Quantum-drift-diffusion method. Using different gate oxide, the DIBL, subthreshold slope, and I_{on} current versus I_{off} current under different EOT are presented and compared, also the gate direct tunneling current as function of the gate voltage are presented. Section V concludes the paper.

II. DEVICE STRUCTURE

An even higher I_{on} current and decreased subthreshold slope can be obtained by the careful choice of a gate dielectric. Moreover a Physical gate length of 7nm is kept constant for easy comparison. At this channel length limits, the susceptibility of the transistor to short channel effects

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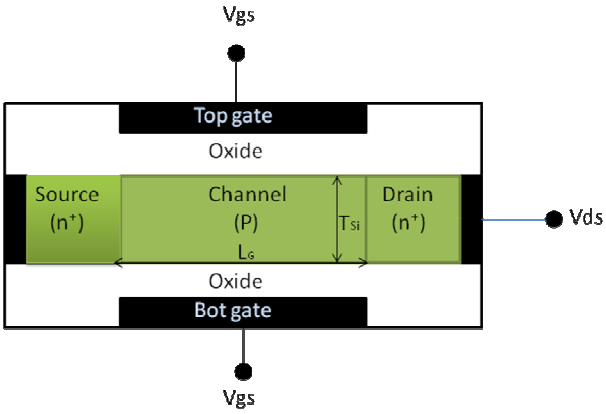

Fig. 1 Symmetrical DG-MOSFET considered in this work.

(SCE) is monitored in several ways such as threshold voltage (V_{TH}), leakage current (I_{off}) and drain induced barrier lowering (DIBL).

The structure of the proposed device is shown in Fig. 1. This symmetric structure is characterized by p-type doped Si channel of width 5nm. This channel is embedded between two heavily n-doped source and drain regions of length 10 nm that are connected to source and drain contacts. The junctions are assumed to be abrupt. The doping concentration of channel and source/drain are 10^{16} cm^{-3}, 10^{20} cm^{-3} respectively. The polysilicon gates with work function 4.1eV are separated from the Si channel by an oxide layer and the power supply voltage V_{DD} is 0.7V.

The 7nm length is chosen to study the performances of device, taking different Oxide thickness (5nm, 1.5nm, 1nm and 0.8nm) with the two Si channel width (5nm and 3nm) for both SiO_2 and HfO_2.

III. THEORETICAL ASPECTS

The model of carrier transport used in this paper is the quantum-drift-diffusion model as implemented in nextnano. This model uses the first moment of the Boltzmann equation to determine the current and the quantum mechanics to calculate the carrier density. The charge density $n_c(x)$ for carriers of type c is calculated by assuming the carriers to be in a local equilibrium characterized by local quasi-Fermi levels $E_{FC}(x)$

$$n_c(x) = \sum_i \left|\psi_{ic}(x)\right|^2 f\left(\frac{E_{Fc}(x) - E_{ic}}{k_B T}\right) \qquad (1)$$

ψ_{ic} and E_{ic} are respectively wave function and energy of eigenstate i that have been obtained from solving the multiband Schrodinger-Poisson equation [8].

The local quasi-Fermi levels $E_{F,c}(x)$ are determined by global current conservation $\nabla \cdot j_C = 0$, where the current J_c is assumed to be given by the semi-classical relation:

$$j(x) = \mu(x) n(x) \nabla E_{F,n}(x) \quad . \qquad (2)$$

The EOT (Equivalent Oxide Thickness) used in this work is that obtained by classical Electrostatic theory in planar devices where [12]:

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} T_{high-k} \quad . \qquad (3)$$

The SiO_2 and HfO_2 permittivities (k_{SiO2}, $k_{high\text{-}k}$) are 3.9 and 21.2 respectively, $T_{high\text{-}k}$: high-k material thickness.

IV. RESULTS

Using the proposed model, the DIBL is calculated for V_{DS} = 50 mV and plotted as a function of the oxide thickness (EOT) in Fig. 2. The evolution of the barrier for T_{Si} varying between 5nm and 3nm illustrates clearly the dependence of the drain-induced barrier lowering (DIBL) on permittivity and Si channel width. The range of variation of the DIBL for SiO_2 based device is from 0.02 eV for T_{Si} = 5nm to 0.063eV for T_{Si}=3nm. The DIBL is decreased for HfO_2 based device and varies from 0.015eV for T_{Si}=5nm and 0.023eV for T_{Si}=3nm. From this figure it can be concluded that HfO_2 has a great impact on the reduction of DIBL.

Fig. 3 illustrates the effect of high permittivity on subthreshold slope. It is well known that a small subthreshold slope is highly desired since it improves the ratio between the on- and off-currents. It is clear from figure 3 that for SiO_2 the subthreshold slope is degraded by almost 400 % when the oxide thickness is reduced from 0.8 nm to 5 nm for a channel width of 5 nm. While for HfO_2 the subthreshold slope is less degraded (only 148 %) for the same channel width. The figure also show that reducing the channel width (T_{Si}) to 3nm the same trends as already are observed for both SiO_2 and HfO_2. The subthreshold slope takes a minmum value 90 mV/dec at EOT=1.5nm. We can conclude that subthreshold characteristics of SOI DGMOSFET based HfO_2 are clearly better than SiO_2 based device, but remains far from ITRS recommendation as the subthreshold slope S should not be higher than 80mV/dec.

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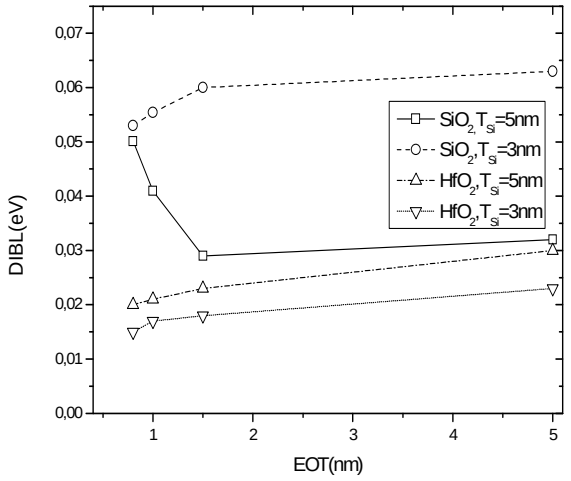

Fig. 2 DIBL as a function of the oxide thikness EOT (nm)

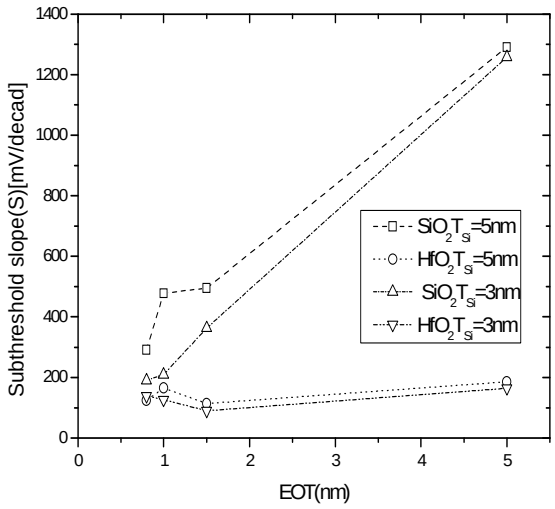

Fig. 3 Subthreshold slope as a function of EOT

Fig. 4 and Fig. 5 show gate direct tunneling current as function of the gate voltage. The gate direct tunneling current becomes an increasingly important such when reducing T_{Si} at 0.8nm physical thickness, and becomes much higher when replacing SiO_2 with HfO_2 thus the gate current at $V_{DS}=V_{DD}=0.7V$, is varied from $9.15\cdot10^{-19}$ A/m at EOT=5nm to 0,135A/m at EOT=0.8nm for SiO_2 and from $1.09\cdot10^{-7}$ at EOT=5nm to 2,03A/m at EOT=0.8nm.

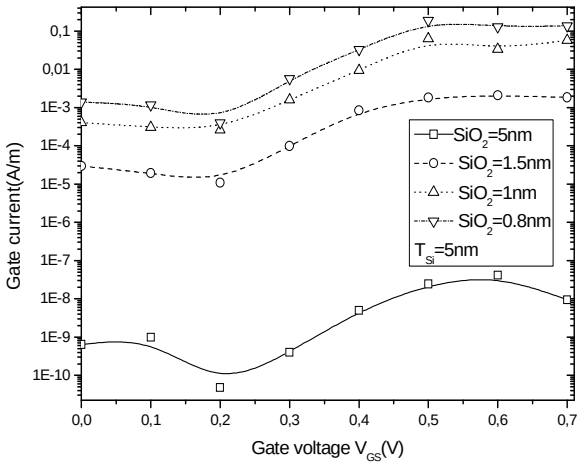

Fig. 4 Gate current as function of gate voltage for SiO_2.

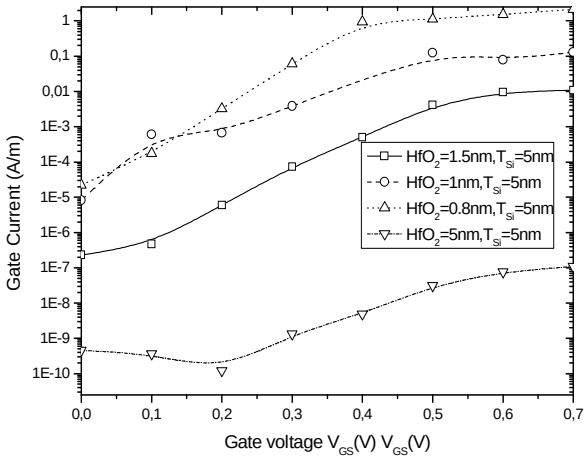

Fig. 5 Gate current as function of gate voltage for HfO_2

The I_{on} current versus I_{off} currrent for different EOT and for two channel width is represented in Fig. 6. The high permittivity increases I_{on} and decreases I_{off} for various EOT, for HfO_2 at EOT=0.8nm, I_{on} current value tends towards 1002.02 A/m with I_{off} currrent value equal to 0.15A/m, besides the SiO_2 I_{on} current value which is equal to 717A/m with I_{off} currrent value equal to 35.208A/m but when reducing the Si width channel to 3nm, we obtained a little values for I_{on} current and I_{off} currrent than 5nm width channel, in this case I_{on} current is much weak, which is cannot meet the ITRS predicted value.

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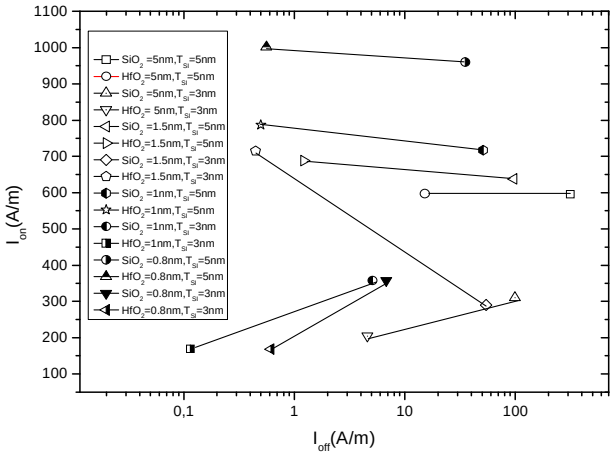

Fig. 6 I_{on} as As a function of I_{off}

V. CONCLUSION

In order to improve subthreshold slope and to suppress drain-induced barrier lowering in SOI MOFET, double gate architecture and high-k dielectric are introduced in this paper. The simulations were conducted using the nextnano code which uses a quantum-drift-diffusion model for carrier transport taking into account quantum confinement effects. It s concluded that hafnium oxide is one of the best candidate to replace SiO_2, due to its extremely high subthreshold slope. Also HfO_2 is effective at reducing I_{off} current and maximizing the ratio of I_{on}/ I_{off}.

REFERENCES

[1] ITRS Roadmap, Semiconductor Industry Association. CA: San Jose, 2006.

[2] Jg. Fossum, “Physical insights on double-gate MOSFETs, ” in proc. COMAC(Government Microcircuit Application Conf.), pp. 322-325, Mar. 2001.

[3] T. Ernst, C. Tinella, C. Raynaud, S. Cristoloveanu “Fringing fields in sub-0.1µm fully depleted SOI MOSFETs: optimization of the device architecture”, Solid-State Electronics, vol. 46, issue 3, pp. 373-378, Mar. 2002.

[4] R.H. Yan, A. Ournard, and K.F. Lee, “Scaling the Si MOSFET: from bulk to SOI to bulk, “IEEE Trans.Electron Devices, vol. 39, pp. 1704-1710, July 1992.

[5] G. Roy, A.R. Brown, F. Adamu-lema, S. Roy, and Asenov, “Simulation study of individual and combined sources of intrinsic parameter fluctuations in conventional nano-Mosfet’s, ”IEEE Trans Electron Devices, Vol. 53, No. 12, pp. 3063-3070, 2006.

[6] M. Leong, H.S.P. Wong, E. Nowak, J. Nowak, J. Kedzierski, and E.C. Jones, “High performance double-gate device technology challenges and opportunities,” in Procedings of International symposium on Quality Electronique Design, pp. 492-495, 2002.

[7] A. Scholze, A. shenk, and w. Fichtner, “Single-Electron Device Simulation” IEEE Trans. Electron Devices, vol. 47, NO. 10, October 2000.

[8] S. Birner, T. Zibold, T. Andlauer, T. Kubis, M. Sabathil, A. Trellakis, and P. Vogl. “Nextnano: General Purpose 3-D Simulations,” IEEE Transactions on Electron Devices, vol. 54, no. 9, September 2007.

[9] A. Trellakis, T. Zibold, T. Andlauer, S. Birner, R.K. Smith, R. Morchl, and P. Vogl, “The 3Dnanometer device project nextnano: concepts, methods, results, ” J. Comput, Electron, vol. 5, no. 4, pp. 285-289, 2006.

[10] M. Sabatil, S. Hackenbuchner, J.A. Majewski, G. Zandler, and P. Vogl, “ Towards fully quantum mechanical 3D device simulations, ” J.Comput.Electron, vol. 1, no 1/2. pp. 81-85, 2002.

[11] S. Hackenbuchner, “Electronnishe struktur von Halbleiter-Nanobauelementen im thermodynamischen Nichtgleichgewicht, ” in Selected Topics of Semiconductor Physics and Technology, vol. 48, G. Abstreiter, M.-C. Amann, M. Stutzmann, and P. Vogl, Eds. Walter Schottkky Inst, TU Munich, 2002.

[12] J. P. Perdew, Y. Wang, Phys. Rev. B 45, 13244, 1992.

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