Software Defined Radio as a DS-CDMA Receiver

Ryszard J. Katulski
Gdansk University of Technology
Department of Radiocommunications Systems and Networks
Gdansk, Poland
rjkat@eti.pg.gda.pl

Wojciech Siwicki
Gdansk University of Technology
Department of Radiocommunications Systems and Networks
Gdansk, Poland
wojciech.siwicki@eti.pg.gda.pl

Jacek Stefański
Gdansk University of Technology
Department of Radiocommunications Systems and Networks
Gdansk, Poland
jstef @eti.pg.gda.pl

***Abstract* — Programmable radio is one of the latest trends in the construction of multi-standard receivers. The technology, called Software Defined Radio (SDR), is also an ideal test platform that allows trying out different algorithms of signal receiving. This particular feature led to choose this platform to implement a DS-CDMA receiver (Direct Sequence Code Division Multiple Access). This receiver is a part of the radiolocation system called AEGIR. The main task of the receiver is to calculate geographical position on basis of received signals from ground stations. That is why Software Radio has been chosen. It allows a gradual upgrade of data processing algorithms. The main goal was to create a wireless receiver that allows calculating the correct position on the basis of the received signals and the processing time will be minimized as much as possible. This paper mainly focuses on algorithms in terms of correctness of the received signal and, what is equally important, its processing time.**

Keywords – Programmable radio; Software Defined Radio; SDR; phase correction; AEGIR

I. INTRODUCTION

The variety of standards for radio systems makes it necessary to construct a mobile terminal that has the technical possibilities of cooperation with different radio standards. This simple concept created an idea of a programmable radio called Software Defined Radio (SDR), based on a universal hardware layer, with only a layer of software determining its functionality [4-8].

One of the Software Defined Radio features is great flexibility; that is why this platform has been chosen to implement a localization receiver for AEGIR system [1-3]. The use of SDR technology in this approach allowed a flexible shaping of functionality of the receiver. This technique is also an ideal testing platform, because it allows implementing and testing different algorithms.

It consists of a wideband receiver and a personal computer (PC) equipped with an acquisition card. PC with appropriate software is used to control both the receiver and the acquisition card; also it serves for signal processing.

In this article, a basic concept of SDR will be presented. Next, the physical implementation of DS-CDMA signal receiver and its structure will be shown. Selected parameters of received signal and encountered problems with data processing (e.g., initial phase correction, processing time) will be presented as well.

II. SOFTWARE DEFINED RADIO

The concept behind Software Defined Radio is to implement – to the greatest possible extent – signal processing blocks of a radio transceiver in software rather than in dedicated hardware. The differences between the classic "analogue" version of a receiver and the programmable one are illustrated, respectively, in Figures 1 and 2 [4], [5].

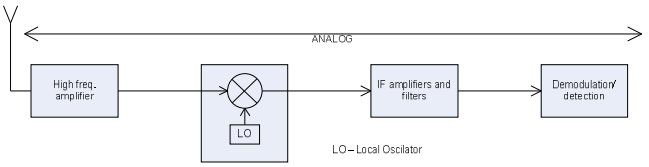

Figure 1. Block diagram of analogue receiver

Receiver shown in Figure 2 can be divided into two different parts of a system:

• hardware (analogue radio) in the form of a set of classic radio components,

• software (digital), whose main element is fast signal processor DSP (Digital Signal Processor).

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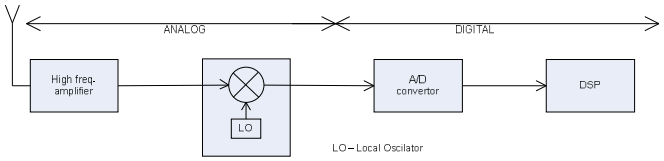

Figure 2. Block diagram of Software Defined Radio

Conceptually speaking, a SDR should have the following properties [7]:

- reconfigurable RX/TX architecture, controlled by software,
- most part of the radio functionality performed by software,
- system specification (bandwidth, bit rate, demodulation) can be updated whenever needed to do so.

The task of the analogue radio part is to strengthen appropriately and convert the received radio signal from the high-band radio frequency to intermediate frequency band. Then, in this band with a fast A/D converter (Analogue to Digital Converter) a received analogue signal is converted into its digital form. Processing is performed in a properly programmed digital signal processor.

III. STATE OF ART

One of the first steps was to check the literature of already implemented receivers in SDR technology. Most of the articles concerned implementations as computer simulations [9-10]. There were also articles on the hardware implementation based on FPGA (Field Programmable Gate Array) platform [11-12]. The concept of building a receiver on a FPGA platform has been rejected for the reasons explained later in this article.

Due to the fact that the whole radiolocation system was designed from scratch, the receiver has been created from scratch as well. The aim was to develop a simple and fast algorithm that would allow receiving signals from several sources.

IV. HARDWARE IMPLEMENTATION

Figure 3 shows the diagram of the receiver made in software defined radio technology.

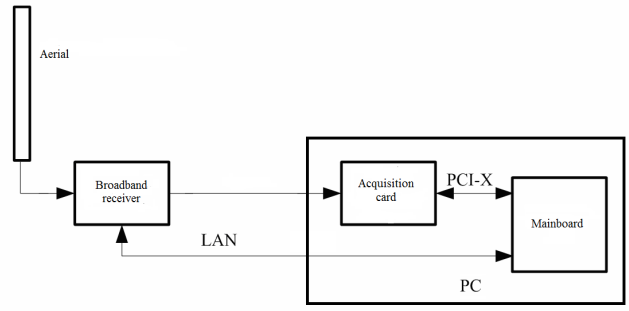

Figure 3. Block diagram of programmable receiver

It consists of a broadband receiver and a PC fitted with a data acquisition card (Figure 4), whereby the analogue radio signal is converted into a sequence of discrete data samples. Computer task is to control the operation of the receiver and to process data received from data acquisition card.

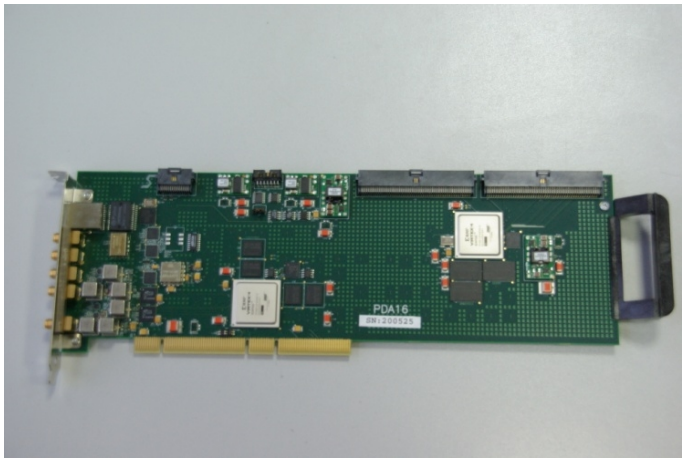

Figure 4. Acquisition card

Parameters of a PC are:

- Processor: i7 980EE (6 cores/12 threads)
- RAM: 6GB
- HDD: 1TB
- Mainboard with PCI-X slot for acquisition card.

Frame structure of receiving data is presented on Figure 5.

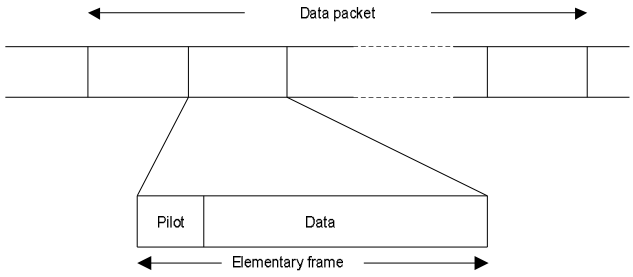

Figure 5. Frame structure

It consists of known sequence of pilot bits and sequence of transmitted data. Sequence of pilot bits are used to improve time of demodulation and are used for initial phase correction. Both mentioned algorithms will be presented later in this article.

Actual received signal parameters are as follows:

- The signal carrier frequency: 450MHz,
- Data rate: 1kHz,
- Bandwidth after spreading: 1MHz,
- Modulation: QPSK,

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- In-phase and quadrature-phase components carry independent data.

As already mentioned, this receiver is part of the radiolocation system AEGIR. For this reason it was decided to build a programmable radio, based on a PC computer (instead of FPGA), which allows to record data obtained from an acquisition card to hard disk and perform test with upgraded algorithms in a post processing.

V. ALGORITHMS

A. Main algorithm

The main algorithm is shown on Figure 6. The program can be divided into two segments. First: configuration and data acquisition, second – digital signal processing.

Program begins with launching and configuring the data acquisition card and setting the parameters of the receiver. Then, the process of acquisition (writing to a binary file data samples) begins. After a certain time, acquisition is completed and acquisition card goes into standby mode. The next step is to process the collected samples. They are multiplied by carrier (both the cosine and sine) and by the spreading sequences.

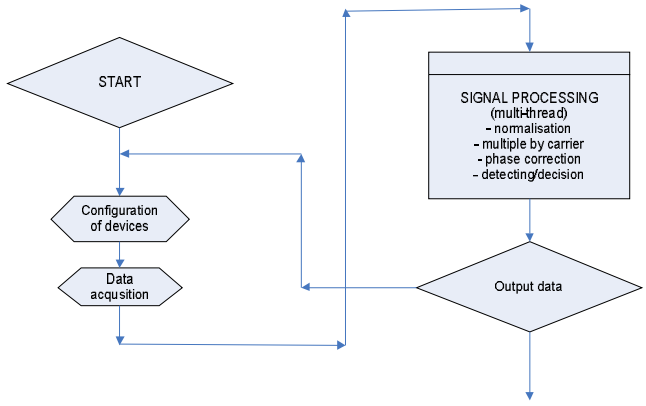

Figure 6. Main algorithm

B. Phase correction algorithm

During the processing of data, we should consider errors resulting from inaccuracies in the internal clocks of the receiver and data acquisition card. Correction is being determined after receiving a few bits; next, it is added in the following stage of detection. This frequency drift and phase error can be illustrated as a constellation of the received signal. Due to the independent component in in-phase and quadrature-phase, received signal can be detected as two BPSK modulation. In this case when *Re value* (read from real axis) is greater then 0 it means that we received logical '1' if is lower then 0 – logical '0'.

Bearing in mind the above, received signal constellation may take the form shown on Figure 7. Bellow the following sequence of bits has been given for illustration:

no	1	2	3	4	5	6	7	8	…	16	17	18	19
bit	1	1	1	1	1	0	0	1	…	0	1	1	0

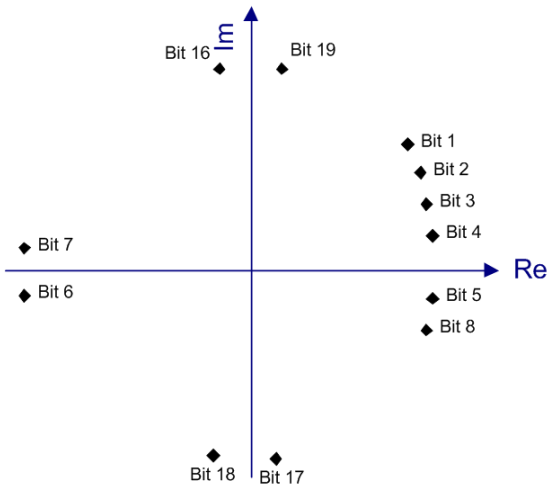

Figure 7. BPSK constellation of a received signal

Analysing the presented sequence with constellation shown in Figure 7 it can be seen that bits 18 and 19 without phase correction have opposite values. Phase correction is based on known sequence of pilot bits. Because sequence is known, correction can be calculated (in order to 'twist' received point on a constellation) and applied on next received bit.

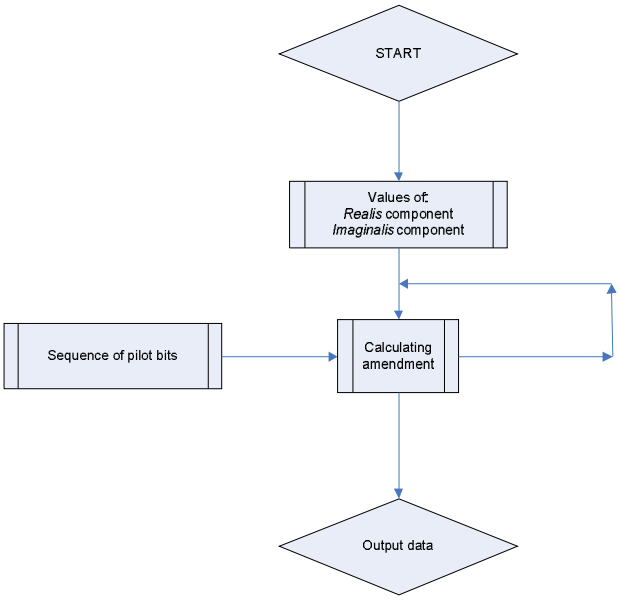

Figure 8. Algorithm of phase correction

After applying the correction phase algorithm (Figure 8), both points are on the side of their actual representation (Figure 9).

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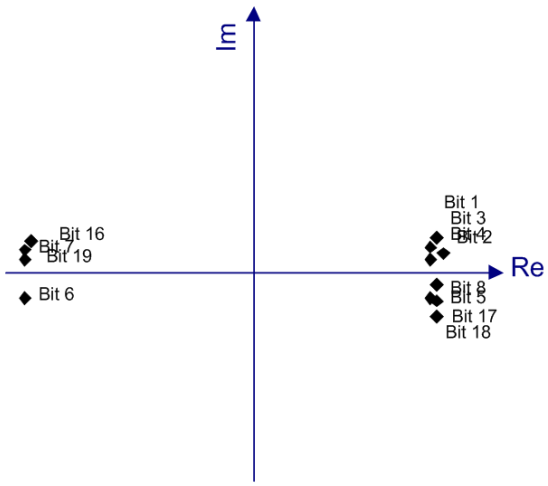

Figure 9. BPSK constellation after phase correction

C. *Processing time*

Time of signal processing is one of the most important parameters of a programmable radio. It is recommended to obtain the strongest possible CPU for a PC. If possible, convert each calculating subprogram to the application, using several processor cores. Only the development of multithreaded applications can effectively cope with the complexity of computing with which we meet in implementing a programmable radio. The hardware layer affects the processing speed; however, it is equally important to optimize the code. Also an algorithm of decoding/detection is very important as well.

Figure 10 shows first algorithm of data decoding. It is based on a classic correlation technic. Received data are correct, but time of computing is very long.

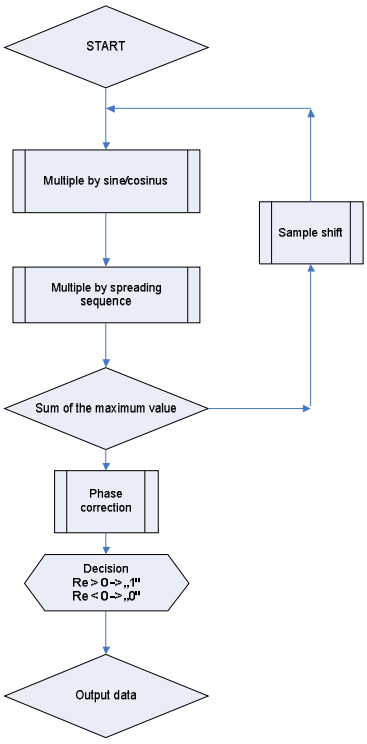

Figure 10. Algorithm od decoding

Because of long time of computing another algorithm was developed. Figure 11 presents this algorithm. It uses Fast Fourier Transformation (FFT) to calculate where the pilot bits start. Based on these results, data are multiplied by spreading sequence already at those locations and get *Re* and *Im* components.

Using the first algorithm, attempts to receive transmitted signal took over an hour of processing time (for 40 seconds of acquisition). Second algorithm reduced this time to approximately 40-60 seconds. The software was rewritten to work in a multithread environment. This procedure allows receiving signal and decoding information from many sources without significant time consumption.

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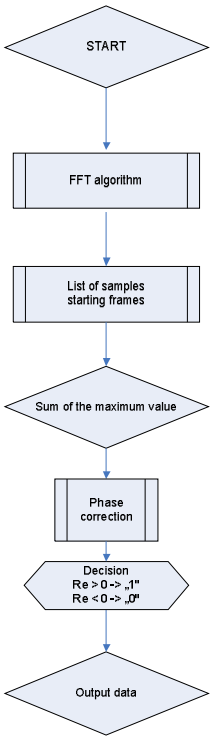

Figure 11. Algorithm od decoding

Given the fact that it is a locational receiver, it was necessary to make such changes in the algorithm that calculated position was generated every few seconds. To this end, the algorithm has undergone another change. Two types of length of acquisition were chosen. Long one with a minimum sampling frequency is used to store long sequences respectively, which allows reading of data contained in the radio signal and a short one at the higher sampling rate, which serves only to determine the differences of time needed to calculate the correct geographical position. Short acquisition time was reduced to about 2 seconds. Increased sampling frequency resulted in much more data to process. That is why FFT algorithm was internally divided to work in a few threads. Through this approach, a short acquisition (two seconds) gave expected time of computation (i.e., generating geographic position) of 4-5 seconds.

VI. CONCLUSION AND FUTURE WORK

Application of the DS-CDMA signal receiver in programmable radio technology allows a flexible approach to updating and verification of the implemented software receiver. It also allows implementing several methods of reception in order to compare their efficiency, correctness and processing time. Studies conducted in the lab and in real conditions confirm the versatility of the platform.

Mentioned AEGIR system was tested twice in real conditions at the Bay of Gdansk. Last test were carried out in October 2010. System is still being updated. Next test will be performed in June 2011 and another bandwidth of spreaded signal will be tested (respectively 2MHz and 4MHz).

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