Design and Implementation of Edge Detection and Contrast Enhancement Algorithms Using Pulse-Domain Techniques

Fatemeh Taherian† Davud Asemani‡ Elham Kermani‡

† Dep. Of Electronic Eng., Islamic Azad University, Tehran Central Branch, Tehran, Iran, F.taherian@iauctb.ac.ir

‡ Electrical Eng. Faculty, K.N. Toosi Univ. of Technology, Tehran, Iran
Asemani@eetd.kntu.ac.ir, Kermani@ee.kntu.ac.ir

***Abstract*—Image pulse sensors provide pixels information with a series of pulse train considering Pulse Frequency Modulation (PFM). PFM sensors are often used in vision chips considering related advantages. In this paper, edge detection and contrast enhancement algorithms are analyzed and simulated using pulse domain techniques of suppression and promotion. Comparing with classical methods, pulse-domain-based algorithms show a better performance as well as simpler implementation in circuit level. Designing and implementing the pulse-domain algorithms on FPGA, a simple and fast realization of image processing methods for edge detection and contrast enhancement is presented. The integration of proposed design in cameras is discussed and evaluated in terms of circuit complexity as well as computational load.**

Keywords- pulse frequency modulation (PFM); suppression; promotion; digital image processing.

I. INTRODUCTION

The demand of solid-state image sensors has grown up largely due to the increasing requests for digital still and video cameras. Charge-Coupled Devices (CCD) were earlier dominant in the image sensor market. However, recent progresses in the design of CMOS technologies have led to appearing CMOS sensors in most imaging products [1]. Acquired pictures of image sensors often encounter quality limitations because of noise, low contrast and blurring effects. Accordingly, image processors are generally used to improve the related image quality after the image sensors. In traditional systems, two chips were allocated for separately receiving and processing the images [2]. This method includes drawbacks such as large chip area, higher costs, higher consumption power and more complexity. In vision chips, this idea has been realized in an integrated way so that necessary processors are implemented along with photosensors to achieve better performance as well as more compact system. The idea of integrating preprocessing and sensor circuits at pixel level before transmitting image pixels has resulted in smart vision sensors and being advantageous over traditional image sensors [2]. A substantial reduction in noise and interferences is obtained as well as one of two chips is realized in the sensor level [3].

With the progress in VLSI technology, digital processing techniques have substituted analog one at the sensor level to improve performance though more transistors are utilized. One of best candidates for image processing at pixel level is pulse domain techniques where the photodiode's output signal is converted to a pulse train considering modulation techniques such as Pulse Frequency Modulation (PFM) [4].

In this paper, the focus is concentrated on basic image processing namely preprocessing techniques in pulse domain considering PFM. PFM photosensor represents the pixel value by the frequency of a series of digital pulses. Pulse modulation exhibit advantages in the image processing applications because of lower power consumption, higher speed and ability to integrate image pre-processing functions at sensor level. Besides, it may be automatically designed and implemented using Electronic Design Automation (EDA) tools. In this paper, image processing techniques including edge detection and contrast enhancement algorithms are designed and simulated in pulse domain as well as implemented on FPGA level. The organization of the paper is as following. Section II provides a review on the classic algorithms of image processing. Section III describes the principles of processing methods in pulse domain. In Section IV, image processing techniques are simulated in pulse domain and compared to classic ones. The results of circuit simulation and implementation are presented in Section V. Finally, Section VI includes the conclusion.

II. CONVENTIONAL APPROACHES

Edge detection and contrast enhancement represent the fundamental operations for improving image quality. In this section, a brief review of main conventional algorithms is described in this regard.

A. Edge detection

Edge enhancement and Edge detection are important methods in image processing. Also, these are basic operations at higher-level visual processing such as image segmentation, recognition and image compression [5]. Changes in some physical properties, such as intensity of illumination, color and reflectance appear as edges in the scene. Various algorithms have been so far proposed for edge enhancement such as Gradient operators (Robert [6], Sobel [7]) using maximum and minimum of first derivative. Gradient methods are more appropriate when the variation of luminance intensity is large in presence of a low noise [8]. Laplacian operator is another approach for edge detection. However, it exhibits a large sensitivity to noise and is unable to detect the orientation of edges. LOG operator is used as another candidate particularly when image is blurring or image noise is large. It is a combination of Gaussian low-

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pass filter and Laplacian operator. As another possibility, Canny [9] employs Gaussian smoothing to decrease noise and the Gaussian first derivative to detect edges. It nevertheless takes longer computation time and is naturally more complicated. However, the characteristics of human vision system have not been considered in these approaches. Marr and Hildreth [10] proposed another way based on the visual human performance using mathematical models. An improvement of this manner was developed by Peli [11] in which some filtering channels are used for edge enhancement stage and the threshold is the contrast sensitivity of human eye, and then, outputs of various frequency bands (spatial scales) are combined for producing the final edge detection. Another method for edge detection is the Logical/Linear operators [12] which combines linear operator's theory and Boolean algebra. Also, new algorithms such as fuzzy theory [13], natural network [14], mathematic morphologic theory [15], wavelet transformation [16] and rough sets [17] have been utilized for edge detection. They are often much more complex.

B. Contrast enhancement

One of the main parameters for measuring the quality of image is contrast. The contrast of image stands for a dynamic range representing the ratio of the brightest to the darkest pixel intensities [18] as follows:

$$Contrast = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \quad (1)$$

That I_{max} and I_{min} represent the highest and lowest intensity of illumination in image respectively. Contrast enhancement procedures leads to an improvement in visual quality for low contrast images. Contrast level is often studied using histograms. The histogram of a digital image with gray levels shows the distribution of pixel intensities [18]. For example, histogram of an image with the pixel intensities in the range $[0, L-1]$ is a discrete function $h(r_k) = n_k$ that r_k is kth gray level and n_k represents the number of image pixels having a gray level of r_k. A normalized histogram is defined as:

$$A(r_k) = \frac{n_k}{n} \qquad k = 0,1,2,\dots,L-1 \quad (2)$$

Contrast enhancement methods include histogram processing methods such as histogram equalization and contrast stretching algorithms such as Negative Transform, Log Transform, gamma correction and gray slicing [5]. The Histogram Equalization (HE) distributes uniformly the pixels over global range of gray levels with a predefined transformation function $s = T(r_k)$. HE method nevertheless suffers from contrast over-enhancement in bright sections.

III. PULSE DOMAIN IMAGE PROCESSING

In pulse-domain, the output signal of photodiode is converted to a pulse train using a pulse frequency modulation (PFM) scheme. In this case, the luminance of pixels is represented by the frequency of related output pulse stream. PFM sensor includes a self-reset feedback loop that consists of a photodiode (PD), a reset transistor and an A/D converter's circuit to obtain the pulse train (Figure 1) [19].

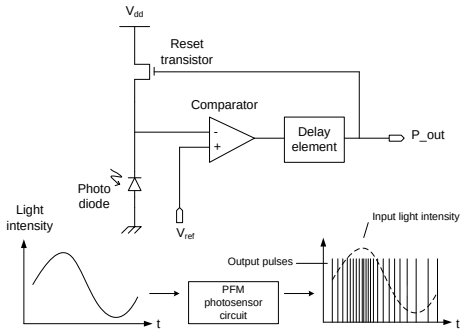

Figure 1. Architecture of PFM photosensor

Various techniques of image processing such as edge enhancement, edge detection and contrast enhancement may be simply realized in pulse domain using only two preliminary operations of suppression and promotion. These basic operations deal with the desired pixel as well as neighboring pixels. In suppression mode, a pulse in the pixel of interest is omitted if it occurs simultaneously with a pulse of neighboring pixel (Figure 2(a)). This cancellation procedure results in a decrease in the intensity of pixel of interest. In second mode, a pulse is inserted in the pulse stream of desired pixel considering promotion method (Figure 2(b)). Promotion algorithm leads to a larger brightness of image since the average number of output pulses increases. To formulate suppression and promotion algorithms, output pulse train IP_OUT may be obtained as follows if assuming that the pixel of interest and neighboring ones are associated with the pulse trains being in phase [19]:

$$IP\_OUT = \begin{cases} P\_OUT.\overline{P\_NBR} & (suppression) \\ P\_OUT + P\_NBR & (promotion) \end{cases} \quad (3)$$

Where P_OUT, P_NBR and IP_OUT stand for pixel of interest, neighboring pixel and the output pulses of pixel of

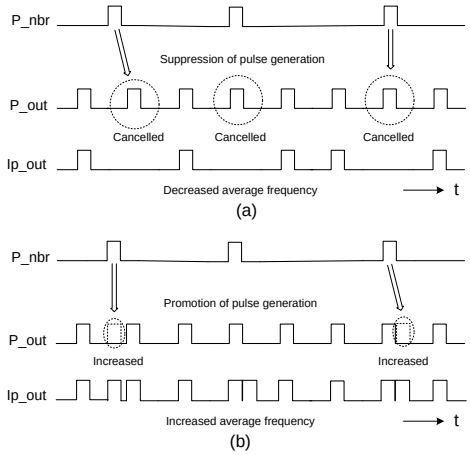

Figure 2. Processing operations in pulse domain: (a) suppression and, (b) promotion algorithms.

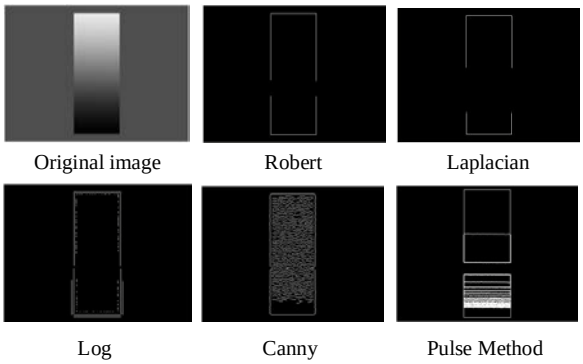

Figure 3. Results of edge detection methods compared to the result of pulse domain technique (right-bottom one).

interest respectively. According to (3), it may be easily shown that suppression operation leads to an edge enhancement and detection (compare with gradient), and pulse promotion operation is associated with a contrast enhancement algorithm.

IV. Simulation and Comparison

In this section, image processing algorithms using suppression and promotion operations are simulated with Matlab and the results are compared with the ones due to conventional algorithms. For this purpose, each image pixel has been represented by a train of 256 pulses as the output of PFM photosensor. Then, the basic pulse operators (suppression and promotion) are applied considering four neighboring pixels. Two codes have been designed as well to simulate PFM modulation and demodulations having applied

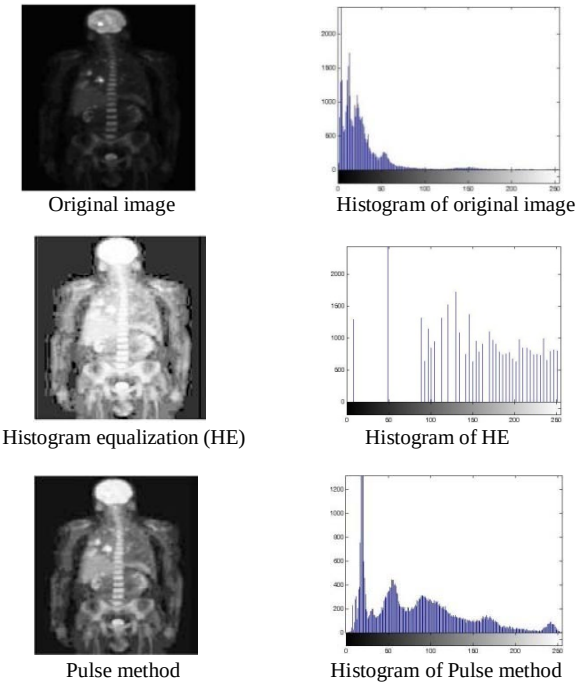

Figure 4. Contrast enhancement: original image (top) vs. the result of HE algorithm (middle) and result of pulse domain technique (promotion).

TABLE I. Comparison of Pulse Method with Conventional Algorithms

Parameter	Conventional Methods	Pulse Method
Data Processing Format	Byte	Bit
Hardware	Adder & multiplier	Bit logic circuits
Complexity	High	Low
Consumption Power	High	Low
Computation Manner	Batch	Real- time
Circuit Cost	High	Low
Speed	Low	High

before and after pulse processing techniques respectively. Then, both input and output of simulations are imagined as image data files. In the suppression algorithm, the pulse of the pixel of interest disappears when any of neighboring pixels send at the same time a pulse. In the promotion algorithm, both pulses of the pixel of interest and the neighboring one are considered in the output separately. Simulations show that pulse domain techniques lead to a better quality of edge detection and contrast enhancement than conventional methods. For example, one can find some edge layers at the output of pulse domain technique that have not been detected through conventional algorithms. Figure 3 shows the results for edge detection algorithms of Robert, Laplacian, Log and Canny compared to the pulse domain result. Besides, it is possible to control the accuracy, orientation and intensity of detected images in pulse domain technique using different neighbor pixel groups. Comparing computation loads, pulse domain technique exhibits faster performance since Laplacian and gradient algorithms are associated with larger computations. For example, a sample simulation time for canny and pulse domain edge detection methods are 0.25s and 0.013s respectively. In Figure 4, the results of contrast enhancement operation using HE algorithm and pulse domain method (promotion) have been shown. The results may be compared using histograms presented in Figure 4 as well. From computational point of view, pulse domain technique shows again a substantial improvement. HE method of contrast enhancement employs a transfer function applying to image that is associated with a large load of computations. Conventional methods such as HE algorithm use a nonlinear function which increases complexity in contrast to pulse domain technique realized by simple logic operations. Accordingly, pulse domain technique provides an algorithm being faster and simpler for contrast enhancement. The comparison of performances has been summarized in Table 1 for pulse domain and conventional methods.

V. Simulation and Implementation on FPGA level

Image processing techniques may be realized at the sensor level by considering two methodologies: inter-pixel [4] and intra-pixel [20] methods. Intra-pixel methods are generally used for improving sensor performance. On the other hand, Inter-pixel implementation leads to realization of programmable pixel sensors. For example, an inter-pixel realization of pulse domain techniques at sensor level has

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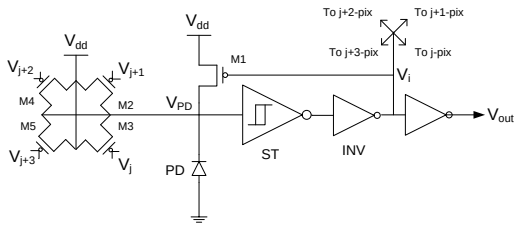

Figure 5. Inter-pixel realization of promotion method at analog sensor level

been shown in Figure 5. It is associated with pulse promotion operation with four neighboring pixels [4]. According to Figure 5, it has been implemented at analog circuit level (sensors). In this paper, image processing algorithms are implemented using an inter-pixel scheme using only digital circuits (not analog sensor level). PFM sensors have been employed for this purpose. A block of 7×7 pixels has been selected as basic block for implementation on FPGA. ISE software from Xilinx has been used along with XST and ISM as integrated synthesis and simulation tools. Considering PFM scheme, a digital basic circuit has been implemented per each pixel. Figure 6 shows the block diagram of related circuit designed for each pixel. In this general configuration, P_nbr represents the output of digital processing on four (up, down, left and, right) neighboring pixel pulses. This architecture realizes both suppression and promotion algorithms depending on control signal of SC. The pixel of interest is represented by p_out and Ip_out signals before and after processing respectively. P2nbr signal is used for next pixels processing as the neighboring pixel. In processing circuits, p_out and p_nbr signals are then utilized. At final stage, a digital circuit has been designed to provide the output in bit format. The output pulses of image processor unit are converted to *n* bits. Considering *M* clock cycles applied in any *n*-bit pixel cycle, the maximum rate of input pulses is supposed being equal to the clock frequency f_{CLK}. In this paper, it has been supposed that $M = 2^n$. Signal rate at each signal wire of pulse train (*P_out*) and output pixel samples (*Q*) would be f_{CLK} and f_{CLK}/M. The output of pixel is read out as an *n*-bit parallel digital signal. The results of timing simulation for one pixel have been demonstrated in Figure 7. In this simulation, it is supposed that n=5 for better illustrating timing diagrams. S and P signals are the outputs of image processing block for suppression and promotion respectively. Meanwhile, the outputs of pulse-to-bit converter block are represented by Q1 and Q2 for suppression and promotion respectively. Figure 8 illustrates

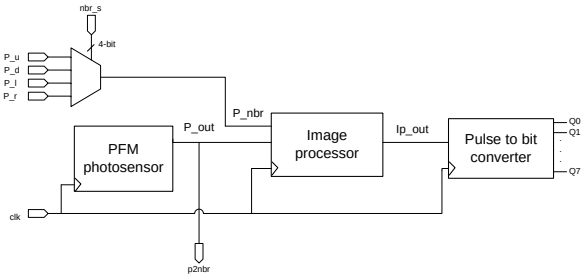

Figure 6. Block diagram of digital circuit per pixel.

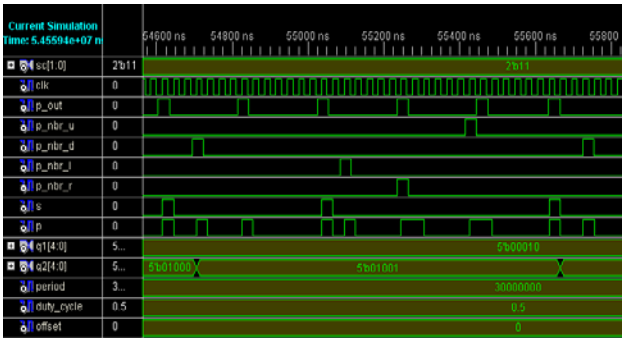

Figure 7.The results of timing simulation for one pixel

the schematic at Register Transfer Level (RTL) for the image processing part of this circuit with n=8. The design summary for image processing and pulse-to-bit converter blocks is demonstrated after implementation in Table 2 considering device counts per pixel. Total number of necessary devices per pixel has been summarized in Table 2 as well. Figure 9 shows the global architecture of an array (block of 7×7 pixels). The output values from any pixel are read out as XY address format.

VI. CONCLUSION

In this paper, parallel image processing algorithms have been discussed and simulated for contrast enhancement and edge detection at the pixel level using pulse domain basic techniques of promotion and suppression respectively. Simulation show that pulse domain techniques lead to a better quality as well as higher performance in comparison to conventional image processing methods. Besides, computational load of pulse domain techniques is limited to logical operations which appear much faster than multiplication operations utilized in conventional methods. On the other hand, pulse domain techniques appear as suitable candidate for implementation. In this paper, a sample implementation has been presented and analyzed at RTL and gate levels. Xilinx Spartan III family has been employed as programmable circuit for implementation of suppression and promotion techniques. Also, this algorithm gives good results for color images. Future work will be concentrated on realization of other image processing algorithms in pulse domain.

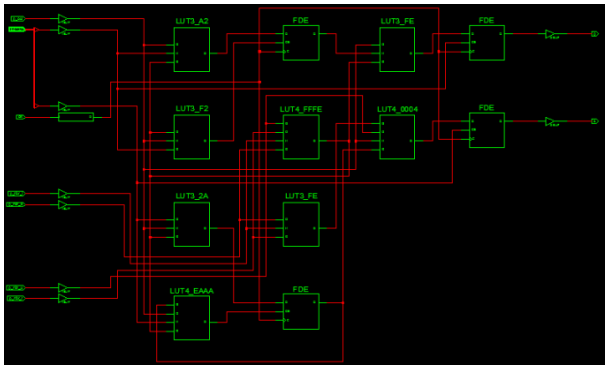

Figure 8. RTL schematic of suppression and promotion algorithms per pixel

TABLE II. Design Summary per Pixel (number of devices used)

Resource	Image Processing	Pulse to Bit Converter	Entire Pixel
No. of Flip Flops	4	38	42
No. of Slices	5	32	37
No. of LUTs	8	45	53
No. of IOBs	10	14	24
Simulation Time	1 sec	1 sec	2 secs

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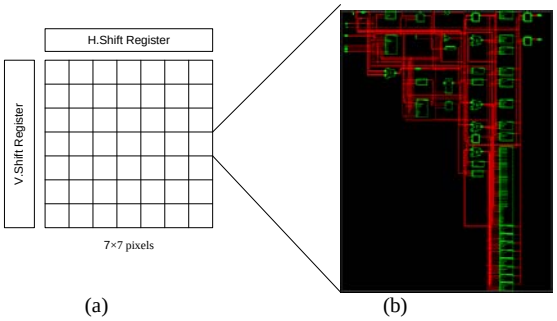

(a) (b)

Figure 9. (a) Schematic diagram of an array, (b) RTL schematic per pixel

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