# Differential Power Amplifiers in 130 nm Partially Depleted and 28 nm Full Depleted Silicon-On-Insulator Technologies for 5G Applications

[1]Marcos L. Carneiro, [2]Tristan Lecocq, [3]Eric Kerhervé, [4]Magali de Matos, [5]Thierry Taris, [6]Jean-Marie Pham
[1]Postgraduate Program in Industrial and Systems Engineering, Pontifícia Universidade Católica de Goiás, Goiânia, Brazil.
[1,2,3,4,5,6]University of Bordeaux, CNRS UMR 5218, Bordeaux INP, Talence, France.
e-mail: [1]mcarneiro@pucgoias.edu.br, [2]tristanlecocq@free.fr, [3]eric.kerherve@bordeaux-inp.fr, [4]magali.de-matos@u-bordeaux.fr, [5]thierry.taris@ims-bordeaux.fr, [6]jean-marie.pham@u-bordeaux.fr

*Abstract*— **This paper starts with a review of the 5G Narrow Band-Internet of Things (NB-IoT) and it provides an analysis of the 130 nm Partially Depleted (PD) Silicon-On-Insulator (SOI) and 28 nm Full Depleted (FD) SOI technologies. It proposes the design of two Power Amplifiers (PAs) for 5G NB-IoT applications and presents performance graphs for S-parameters, Power-Added Efficiency (PAE), gain, output power (*Pout*), frequency sweep, and different biasing setups for the back-gate voltage. Both PAs consist of a gain stage (driver) and a power stage, using pseudo-differential and cascode topologies. The 28 nm PA includes an additional stacked transistor in the power stage to accommodate a higher drain bias voltage. They were fabricated and measured, demonstrating the gain adjustment capability of FDSOI technology via back-gate voltage, which allowed for approximately 3.6 dB of gain adjustment. Both PAs met the required performance parameters in post-layout simulations, achieving maximum Power-Added Efficiency (*PAEmax*) of 49% and 38.5%, gain of 36 dB and 34 dB and saturated Power (*Psat*) of 32 dBm and 28.8 dBm, respectively for 130 nm and 28 nm, placing them at the state-of-the art.**

***Keywords- Power Amplifier; CMOS; 130 nm PDSOI; 28 nm FDSOI; 5G applications; Nb-IoT.***

## I. INTRODUCTION

This paper is an extended version of [1]. This version adds a review section about the Narrow Band-Internet of Things (NB-IoT), the integration technologies of 130 nm Partially Depleted (PD) Silicon-On-Insulator (SOI) and 28 nm Full Depleted (FD) SOI, and Power Amplifiers (PA). In the design methodology section, the resistivity of the thick metal layers as a function of the track width for 130 nm PDSOI and 28 nm FDSOI technologies was added, along with details about the designed interstage wideband transformer used in both technologies and the cascode active balun used in the 28 nm circuit. On results it was added the 28nm FDSOI PA Pout vs Pin measured performances for 3 levels of back-gate voltage and the Pout and PAE performances, related to the frequency between 1 GHz and 3 GHz, for circuits on both technologies.

The transition from 4G Long Term Evolution (LTE) to 5G has revolutionized the Internet of Things (IoT) with the advent of massive IoT, enabling the connection of numerous devices simultaneously. Narrow Band-Internet of Things (NB-IoT), a key 5G standard within Low-Power Wide-Area Networks (LPWAN), addresses the need for massive IoT by supporting battery-powered devices with extended lifespans and optimized installation costs. Operating on licensed 3GPP bands, NB-IoT offers higher data rates compared to unlicensed LPWAN technologies like Long Range (LoRa) and Sigfox. It achieves extensive coverage through transmission repetitions and increased signaling power, while its Single-Carrier Frequency Division Multiple Access (SC-FDMA) modulation reduces Peak-to-Average Power Ratio (PAPR), improving Power Amplifier (PA) efficiency and ensuring suitability for massive IoT applications [2].

Silicon-on-insulator (SOI) technology is pivotal for overcoming RF integration challenges in IoT circuits. Leveraging the high integration capabilities of Complementary Metal-Oxide-Semiconductor (CMOS), SOI reduces parasitic capacitances with a BOX layer, enhancing performance by over 20% [3]. While SOI improves reliability, energy efficiency, and reduces variability compared to bulk CMOS [4], NB-IoT's Single-Carrier Frequency-Division Multiple Access (SC-FDMA) modulation imposes strict PA design requirements, demanding linear operation and efficiency at low power. Advanced SOI technologies like Partially Depleted SOI (PDSOI) and Full Depleted SOI (FDSOI) provide tailored solutions, excelling in isolation and low-power scenarios, respectively [5].

This paper analyzes the 130 nm PDSOI and 28 nm FDSOI technologies, and it proposes the design of two PAs for the 5G NB-IoT applications (see Fig. 1). The gain and linearity adjustment capability via the back-gate voltage of FDSOI technology is demonstrated. Both circuits consist of PAs with a gain stage (driver) and a power stage, using pseudo-differential and cascode topologies.

Section II presents a review of the NB-IoT, the integration technologies of 130 nm PDSOI and 28 nm FDSOI, and PAs classes. Section III compares 130 nm PDSOI and 28 nm FDSOI technologies, highlighting their components and PA design methodology. Section IV presents post-layout simulation and measurement results, including performance analysis, gain tuning via back-gate voltage for the 28 nm PA, and a state-of-the-art comparison. Section V concludes with findings and future research directions.

## II. TECHNOLOGY AND CIRCUIT REVIEW

With the evolution from 4G to 5G and the growing demand for connected devices, developing new standards that allow an increase in the number of simultaneously connected

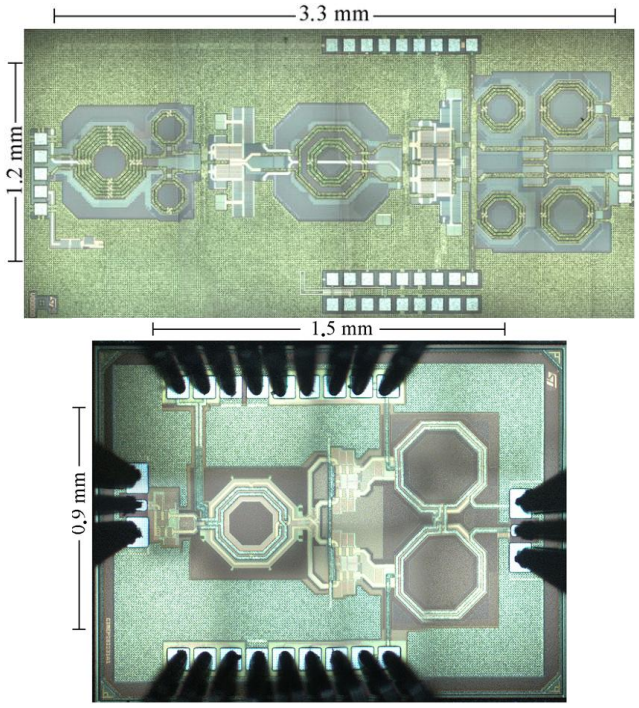


Figure 1. 130nm PDSOI PA (top) and 28nm FDSOI PA (bottom).

devices is essential. This section is dedicated to presenting the NB-IoT standard, the benefits of using silicon technologies for IoT circuits, and topics on the characterization and design of power amplifiers (PAs), as well as the key parameters that affect design.

*A. NB-IoT Standard*

The IoT refers to a network of electronic devices that gather, process, and communicate environmental information, such as temperature and pressure. Devices, or IoT nodes, transmit data to a base station, which centralizes information for analysis. Data can then be stored and processed in the Cloud or locally, depending on whether the base station's computing capacity is sufficient [6]. IoT networks can be organized as local area networks (LANs) for limited geographical areas, connecting to the internet via wireless protocols such as Wi-Fi or physical cables for improved efficiency and speed. For broader coverage, wide area networks (WANs) with low-power wireless standards (LPWANs) are employed. LPWANs enable battery-powered IoT devices to operate for extended periods, thereby optimizing installation costs by reducing the number of required base stations. Standards such as LoRa and Sigfox utilize free ISM bands, enabling cost-free operation with limited data rates. In contrast, NB-IoT and Cat-M operate in licensed 3GPP bands, which support higher data rates but incur higher costs due to licensing [2].

The 5G network, as the fifth generation of cellular communication standards, builds upon advancements in speed, bandwidth, and functionality that have evolved since the inception of mobile networks in the 1980s with 1G. Initially limited to analog voice transmission, each generation has expanded capabilities to meet growing demands, with 4G in 2016 facilitating support for IoT. The deployment of 5G not only continues these improvements but also targets modernization in industrial sectors and the development of smart cities [7]. This evolution, along with the rapid growth in the industrial IoT market [8], calls for revisiting existing IoT standards. Massive IoT, a concept introduced with 5G, is designed to support a high density of connected devices through enhanced LPWAN technologies and the capabilities of 5G. Its defining features include high connection density, irregular non-critical data transfers, small data packet sizes, and stringent energy efficiency requirements, aiming for over 10 years of battery life [9].

To meet the stringent requirements of massive IoT, 5G introduces two dedicated standards, Cat-M and NB-IoT. This paper focuses on NB-IoT, due to its extensive research applications. NB-IoT, an LPWAN standard, reuses 4G LTE frequency bands and protocols to streamline deployment. This standard emphasizes extended network coverage and ultra-low device complexity [10]. Coverage improvements are achieved through transmission repetitions and increased signaling power, with three repetition modes allowing varying degrees of coverage enhancement. However, increased repetition and power can impact energy consumption, requiring a trade-off between low power use and extensive coverage. To reduce device complexity, NB-IoT optimizes the physical layer, lowering the computing demands for signal processing. It also employs SC-FDMA modulation for the uplink, which reduces PAPR and improves the power amplifier's efficiency [11]. NB-IoT encompasses multiple emission classes (e.g., classes 3, 5, and 6) to adjust power usage according to quality of service (QoS) requirements, thereby optimizing energy consumption [12]. Additionally, energy-saving techniques such as eDRX and PSM are employed. eDRX allows for the periodic shutdown of the receiver, while PSM enables deep sleep mode by turning off the radio module for negotiated periods, further extending battery life [13].

SC-FDMA modulation is crucial in minimizing energy consumption for NB-IoT devices, as it enables single-carrier characteristics through a digital Fourier transform (DFT) while maintaining subcarrier allocation, thereby supporting multiple connections [14], [15]. Unlike OFDMA, where each QPSK symbol occupies one subcarrier for the entire symbol duration, SC-FDMA encodes each QPSK symbol across all N subcarriers for 1/N of the symbol duration, achieving lower PAPR. This flexibility enables simultaneous multi-user access on the same LTE channel and dynamically allocates resource blocks (RBs) according to user demand, with two modes of allocation—localized and interleaved. For example, in a 10 MHz LTE channel, there are 50 RBs, each with 12

subcarriers, resulting in 600 addressable subcarriers for allocation [14], [15]. SC-FDMA is well-suited for massive IoT applications by balancing energy efficiency and user capacity within LTE constraints [14].

*B. SOI Technology for RF function integration in Silicon*

CMOS SOI technology involves manufacturing a wafer with an inserted insulating layer, resulting in a silicon-insulator-silicon substrate stack. The thickness of the upper silicon layer can range from 5nm to several micrometers. Various insulators are used for these wafers (e.g., sapphire, silicon oxide), with silicon oxide being the most common for low-cost applications. The most widely used SOI wafer fabrication processes are Separation by IMplanted OXygen (SIMOX) and the Smart-Cut method, which together account for 90% of SOI wafer production [16].

The SIMOX process begins with implanting a large amount of oxygen into a standard wafer. A high-temperature annealing step then transforms the oxygen ions into a silicon oxide layer. The oxide layer's thickness and depth are controlled by annealing temperature, dose, and energy used during oxygen ion implantation [16].

While advanced silicon-on-insulator (SOI) technologies such as SIMOX improve silicon's electrical performance, silicon-based materials still face limitations in high-power applications. As a result, power amplifiers for commercial use—particularly in mobile telephony—often rely on III-V technologies, such as GaAs or GaN, which offer superior power performance compared to silicon technologies (see Fig. 2). Silicon has lower breakdown voltages, making it less competitive with these materials. Additionally, CMOS has a lower maximum operating frequency than its III-V counterparts, making it easier to design power amplifiers with III-V technologies. However, CMOS offers high integration capability and low cost, attracting industrial interest, especially in massive IoT applications.

CMOS SOI technology inherits many advantages from bulk silicon technology, particularly its integration capability and low manufacturing cost. SOI technology shares many aspects of the CMOS fabrication process, thereby keeping production costs low. Adding the steps to convert a CMOS wafer into a CMOS SOI wafer only increases costs by about

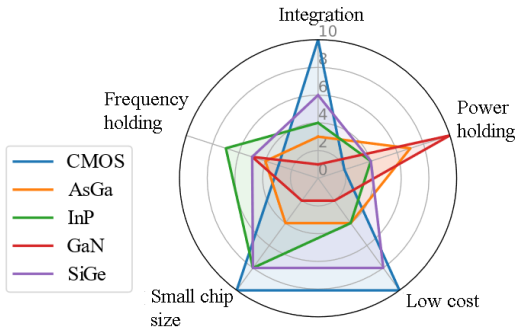



Figure 2. Comparing integrated technologies.

10% to 15%, making SOI competitive in terms of cost [4]. Additionally, the cost gap narrows as technology nodes shrink, providing a significant advantage for SOI.

SOI technology enhances performance by over 20% due to the reduction of parasitic capacitances in transistors [3]. This improvement primarily results from isolating the transistor's active area from the substrate with a BOX layer, thereby preventing the direct connection of PN junction capacitances to the transistor and reducing parasitic capacitances. SOI also offers improved reliability, reduced process complexity and variability, and lower energy consumption compared to CMOS technology [4].

Both CMOS and CMOS SOI technologies continue to evolve, particularly with decreasing minimum feature sizes, resulting in enhanced transistor frequency performance, improved integration, and lower circuit production costs. However, transistor miniaturization also increases their susceptibility to degradation due to the reduction in maximum supported voltages for each junction.

To enhance integration, technologies are adding more metal layers, which reduces the individual layer thickness and thus the maximum current density. Lower maximum voltages and current densities further limit the power handling of CMOS technologies, so several degradation mechanisms must be considered in PA design [17] as gate oxide breakdown, hot carrier injection, punch-through effect, floating body effect, and electromigration.

*C. Power Amplifiers*

The power amplifier is the circuit responsible for amplifying the input signal to a specified output power level, as defined by the NB-IoT standard, before transmitting it to the antenna. It is therefore subject to constraints related to power, linearity, efficiency, and thermal management.

Power amplifiers are categorized into two main operating classes: linear (or sinusoidal) and switching. Linear classes, including Class A, AB, B, and C, are defined by the transistor's conduction time, set by its biasing, where the transistor operates as a controlled current source [18]. This mode yields a linear relationship between the input and output power, making it suitable for signals that require linearity.

Switching classes, such as Class D, E, F, and G, are based on the harmonic treatment of the output network or the input signal processing. Here, the transistor functions as a switch, and these classes are generally suitable only for constant-envelope signals. However, since NB-IoT employs SC-FDMA modulation, which does not have a constant envelope, only linear operating classes are suitable for this application.

The choice of an operating class for a PA depends on efficiency, output power, gain, and linearity constraints. As the conduction angle decreases, power gain also decreases due to the increased excursion of the input signal required to reach the maximum current. Operating classes A, AB, and B

provide a balance between efficiency, gain, and linearity.

As modulation complexity and/or operating frequency increase, the amplifier must be more linear and have maximum gain, guiding the choice toward Class A.

For NB-IoT, with a frequency below 6 GHz, gain and linearity must still be optimized, making a deep Class AB—close to Class B—the preferred choice.

## III. Design Methodology

This design methodology section presents a study on technologies and the designed PAs. Details about the metal layers of the 130 nm FDSOI and 28 nm PDSOI technologies are presented, followed by a comparison of the inductors, capacitors, and transistors of both technologies. The parameters are presented in the order in which the designer should analyze them during the project. Based on this analysis, the following subsection provides details of the schematics of the two designed PAs, highlighting their similarities and differences.

### *A. Evaluation of Passives and Transistors of SOI Technology*

Fig. 3 presents the metal layers of the 130 nm PDSOI and 28 nm FDSOI. The first observation concerns the difference in the number of available metal layers and their thickness. Indeed, the smaller the technology node, the higher the integration density, which also requires an increase in interconnection density. Several solutions have been implemented to increase this density [19]. The rise in metal layers and the reduction of the minimum etching widths are the most common and easiest to apply. However, reducing the minimum etching width impacts the maximum thickness of metal layers that can be achieved due to manufacturing processes. This consequently explains the reduction in the thickness of the metal layers in the 28 nm FDSOI.

To determine the quality of the interconnections, the graphs presented in Figure 4 show the resistivity of the thick metal layers as a function of the track width. The metallization of the 130 nm PDSOI exhibits significantly improved performance due to the thicker layers of both aluminum (ALU, LB) and copper (M4U, Ix). The curves are plotted between the $W_{min}$ and $W_{max}$ of each level. Thus, in addition to having higher resistivity, the 28 nm FDSOI also has lower maximum widths in Ix layers. This must be considered in electromigration calculations to ensure that the conductor is sufficiently wide to carry the desired current. The densification of the metal layers also leads to a decrease in the maximum voltages between two metal levels due to the phenomenon of Time-Dependent Dielectric Breakdown (TDDB) [20]. Consequently, the maximum power supported by the passives is reduced.

Figures 5 and 6 illustrate the performance of inductors and capacitors from each technology, respectively. The

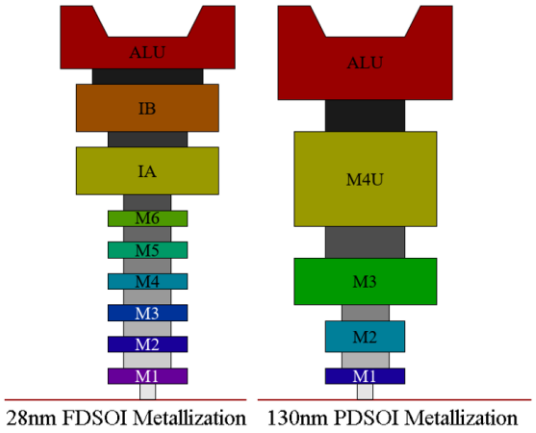



Figure 3. Metal layers of 28 nm FDSOI and 130 nm PDSOI technologies

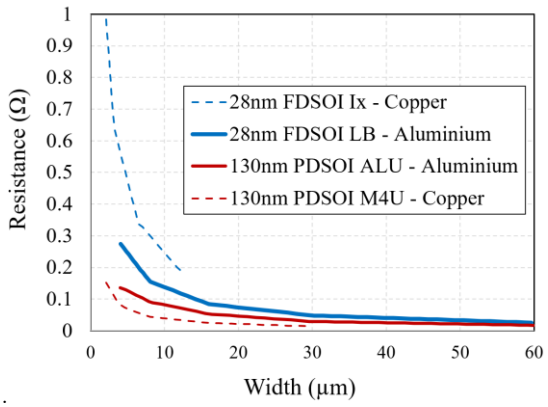



Figure 4. Resistivity of the thick metal layers as a function of the track width for 130 nm PDSOI and 28 nm FDSOI technologies.

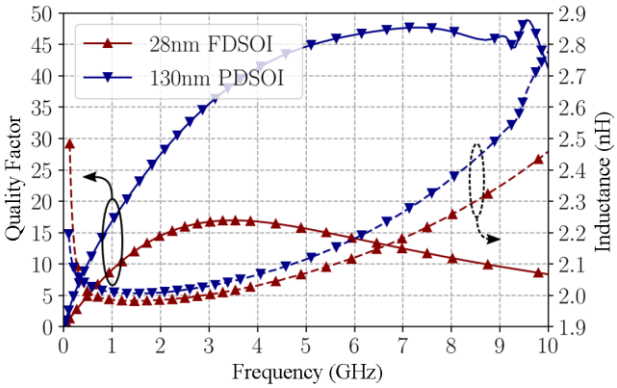



Figure 5. Comparison of inductances from 28 nm FDSOI and 130 nm PDSOI technologies.

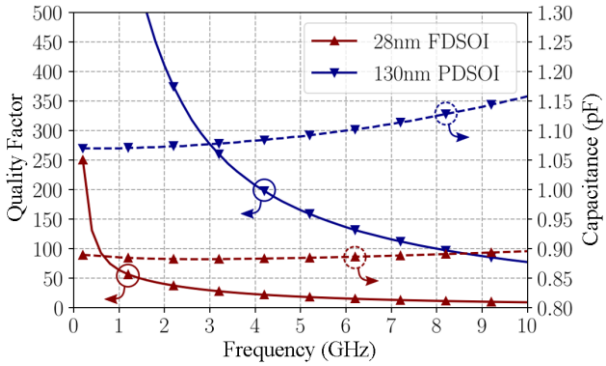



Figure 6. Comparison of capacitances in 28 nm FDSOI and 130 nm PDSOI technologies.

comparison was made with inductors using an octagonal topology [20]. In 28 nm FDSOI, the inductors are designed on the three thick levels, ALU-IB-IA (see Fig. 3), to reduce resistivity and increase the quality factor at low frequencies. In 130 nm PDSOI, two thick metal levels, ALU-M4U (see Fig. 3), are utilized. For the same topology, the inductor achieves a quality factor *Q* of 28 at 2 GHz in 130 nm PDSOI, compared to 15 in 28 nm FDSOI. However, high-value inductors exhibit better high-frequency behavior in 28 nm FDSOI due to a higher self-resonant frequency, indicating lower parasitic capacitances. For capacitors, the quality factor at 2 GHz in the 130 nm technology is approximately 300 for a capacitance of 1.1 pF (see Fig. 6). In contrast, the 28 nm technology yields a quality factor of 40 at 2 GHz for a capacitance of 0.88 pF. Indeed, the 28 nm technology has much thinner and more resistive metal layers than the 130 nm technology. On the other hand, the capacitors in 130 nm occupy larger silicon areas.

Figures 7 and 8 show the output transfer characteristics of NMOS transistors for RF applications in PA design. The transistors from 28 nm FDSOI have a higher current density, reaching 1.2 mA at the maximum *Vgs* voltage, compared to 0.58 mA for the thick oxide transistor in 130 nm PDSOI. Additionally, the 28 nm transistors have lower threshold voltages, around 250 mV, compared to approximately 350 mV for the 130 nm transistors, enabling operation at lower voltages.

The 130 nm PDSOI technology offers improved transistor quality in the saturation region. Indeed, the slopes *∂Id/∂Vds* in the saturation region are lower for the 130 nm PDSOI transistors than for the 28 nm FDSOI transistors. This also indicates that the *gds* in 130 nm is lower than in 28 nm. The consequence is achieving more linear transistors for large-signal applications.

In summary, the electrical characteristics of the 28 nm FDSOI transistors—higher current density, lower threshold voltage, and reduced operating voltage—make them more suitable for energy-efficient, compact, and long-range IoT RF transmitters, particularly in systems requiring LPWAN or massive-IoT operation. These advantages enable smaller chips, longer battery life, and more reliable communication in constrained environments.

### *B. Power Amplifier Design Methodology*

The two PA architectures were designed (see Figs. 9 and 10) based on preliminary transistor sizing and analysis of the presented passive components. Both architectures were designed to achieve comparable performance and NB-IoT restrictions in post-layout simulations. This allows for evaluating their fabricated circuit measurements to compare the two technologies and discuss their advantages and limitations in relation to the target application.

Each circuit includes a driver stage with a single-ended input and pseudo-differential cascode topology at the output. Additionally, both circuits feature a pseudo-differential cascode power stage. The 130 nm PDSOI PA, depicted in Fig. 9, incorporates a pseudo-differential cascode power stage alongside a pseudo-differential cascode driver setup. This configuration ensures a straightforward design and excellent

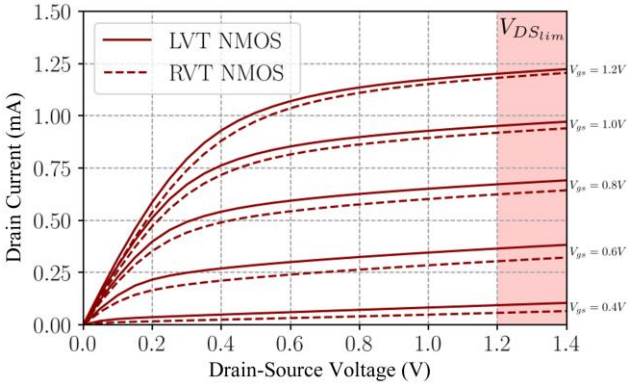



Figure 7. Output Transfer Characteristics Id(Vds) in 28 nm FDSOI.

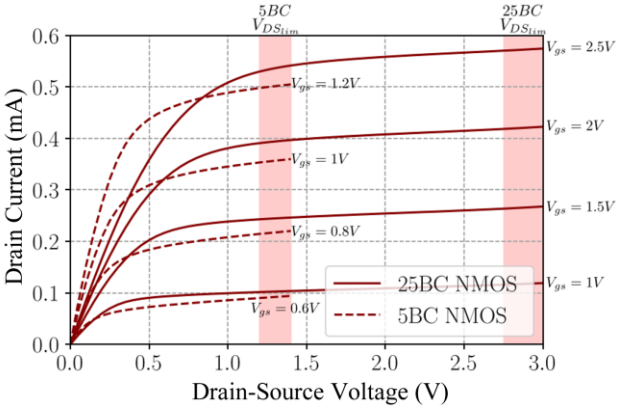



Figure 8. Output Transfer Characteristics Id(Vds) in 130 nm PDSOI.

performance tailored for NB-IoT applications. The design achieves higher output power by employing pseudo-differential architecture while minimizing constraints on the ground return path by suppressing even harmonics. Furthermore, the cascoded transistor arrangement enhances the amplifier's gain, allowing it to meet the 35 dB target specification. To ensure stability, given the high gain, neutralization capacitors ($C_{neutro}$) are incorporated. The matching networks are designed to enable broadband operation facilitated by a broadband matching transformer. In the 130 nm technology, the power stage transistors were dimensioned with $W_{total}$ = 1200 µm, and the driver stage transistors were dimensioned with $W_{total}$ = 300 µm. The circuit was biased with Vdd = 5 V.

The interstage wideband transformer in the 130nm PA (see Fig. 11a), located between the driver and the power cell, was designed to present a coupling coefficient (k) of 0.35 at the central frequency of 1.85 GHz. The simulated optimal conjugated output impedance of the driver is $R^*_{optDRV}$ = 50 − 50j Ω and the input impedance of the power cell is $R_{inPC}$ = 5 − 27.2j Ω. The wideband transformer presents inductances of 3.4 nH and 2.8 nH in the primary and secondary, respectively. The quality factors are 2.8 and 5.1 for the primary and secondary, respectively.

The transformer exhibits an average insertion loss of 2.1 dB, with a minimum of 1.9 dB at 1.54 GHz. The significant losses are mainly due to the reduced coupling coefficient of the transformer and the quality factors of the

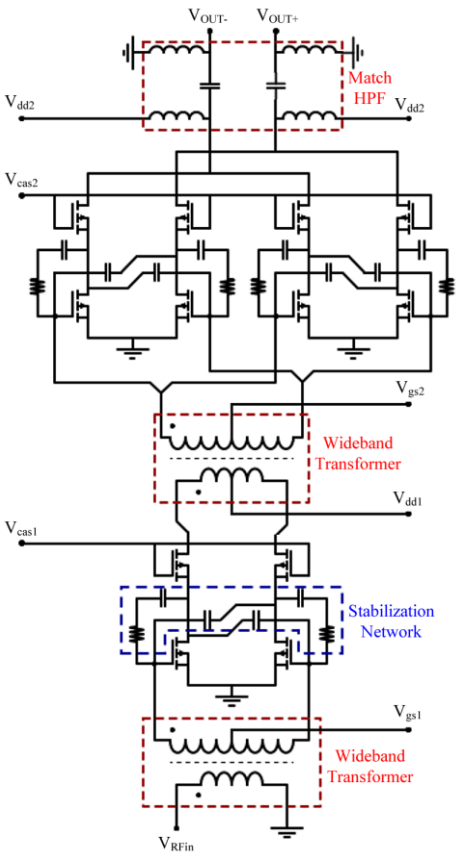



Figure 9. PA in 130 nm PDSOI technology schematic.

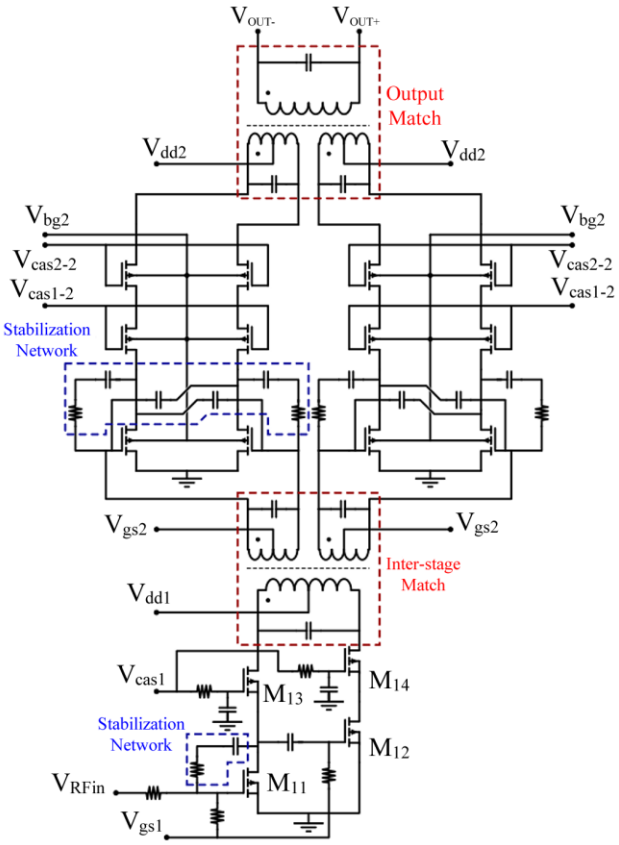


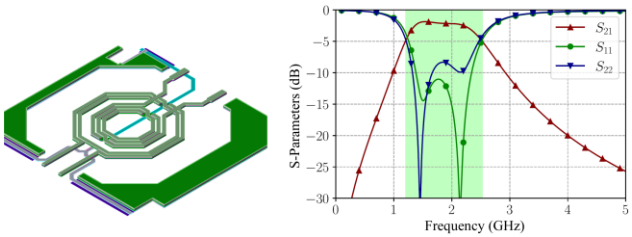

Figure 10. Schematic PA in 28 nm FDSOI technology schematic.

inductors in 130 nm PDSOI technology. The 3 dB bandwidth of the circuit is 1.3 GHz, with a lower cutoff frequency at 1.2 GHz, allowing coverage of the entire targeted NB-IoT band. Figure 11b presents the transformer's small signal performance.

Figure 10 shows the complete schematic of the PA in 28 nm FDSOI technology. This design utilizes two power cells with differential triple-stack cascode topology in its power stage to enable a supply voltage (Vdd) closer to the 130 nm technology, facilitating a more accurate comparison. The power cells are combined to compensate for the technology's power limitations, enabling a total output power of 28 dBm.

The output matching network uses a distributed active transformer (DAT) to optimize the load impedance at the output through series recombination. The inter-stage matching is designed around a 2-to-4 transformer (Figure 12), which performs impedance matching while distributing power across each power cell. Finally, the driver employs a cascode active balun topology [21], eliminating the need for a passive input balun. In the 28 nm technology, the power stage used transistors with $W_{total}$=900 µm, and for the driver stage, $W_{total}$=225 µm, and the circuit was biased with $Vdd$=3V.

The cascode active balun in the input of the 28 nm PA functions as an amplifier that transforms a single-ended input into a differential output, while also supplying sufficient gain for the subsequent power stage [5]. This approach helps minimize chip area by eliminating the need for a passive balun




(a) Transformer layout (b) S-Parameters performance

Figure 11. (a) Transformer layout in the 130 nm PA and (b) small signal performance.

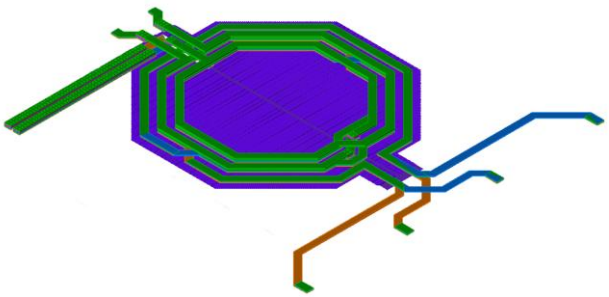


Figure 12. Inter-stage matching 2-to-4 transformer layout in the 28nm PA.

typically placed before the driver stage. The active balun design (shown in Fig. 9) employs a common-source transistor (M11) to provide the initial 180° phase shift. The resulting signal is then directed through a second common-source transistor (M12), introducing an additional 180° shift, effectively producing a signal in phase with the original input. Both differential signals are further amplified using common-gate transistors (M13 and M14), which serve as cascode stages to enhance gain, output isolation, and power capability. A series capacitor connected to the gate of M12 serves a dual purpose: it decouples the transistor's DC bias and allows fine-tuning of the signal level reaching M12, ensuring a balanced output power across both branches.

This circuit explores the potential for improving output power by utilizing a stacked architecture and back-gate biasing, aiming to meet the power requirements of NB-IoT applications. The back-gate voltage allows for fine-tuning of the gain and linearity performance, as demonstrated in the results section.

In the case of inductors and transformers, the coplanar topology was preferred in 130 nm PDSOI due to the limited number of thick metal layers. In 28 nm FDSOI, stacked transformers are favored because of their better coupling factor. Both circuits were designed to achieve post-layout simulations (PLS) at a central frequency of 1.85 GHz, with a bandwidth exceeding 400 MHz, a gain of 35 dB, a maximum Power-Added Efficiency ($PAE_{max}$) above 30%, and a power back-off PAE ($PAE_{PBO}$) above 20%.

## IV. Results and Discussions

### A. Post-Layout Simulation and Measurement Performance

The S-parameter performance of the PA in 130 nm PDSOI and the PA in 28 nm FDSOI technologies post-layout simulation (PLS) and measurement from 1 GHz to 3 GHz are presented in Figs. 13 and 14, respectively. The 130 nm PA presents an almost constant *S21* performance (between 35 dB and 39 dB) from 1.55 GHz to 2.4 GHz, an *S22* near -3 dB, and an *S11* less than to -5 dB in this frequency range. The 28 nm PA presents flatter behavior, with a maximum *S21* performance of 33 dB between 1.5 GHz and 1.8 GHz, *S22* less than -5 dB, and *S11* less than -15 dB.

The gain and PAE performances for the 130 nm PA from post-layout simulation and measurements at a frequency of 1.85 GHz are presented in Fig. 15. The measured gain performance exhibits a class AB characteristic shape, with a gain of 34.5 dB at low power and a maximum of 36 dB. The maximum PAE reaches 48.5% at a $P_{sat}$ of 31 dB in PLS and 38% in measurements at a $P_{sat}$ of 28 dBm.

The gain and PAE performances for the 28 nm PA from post-layout simulation at a frequency of 1.85 GHz are presented in Fig. 16. The gain performance achieves 33.26 dB in low power and a maximum of 34.72 dB; the maximum PAE reaches 38.5% at a $P_{sat}$ of 28.5 dB. The transistors were optimized until the edge of stability was reached, predicting that losses in further components would ensure stability. However, the implemented circuit presented stability issues at high output power.

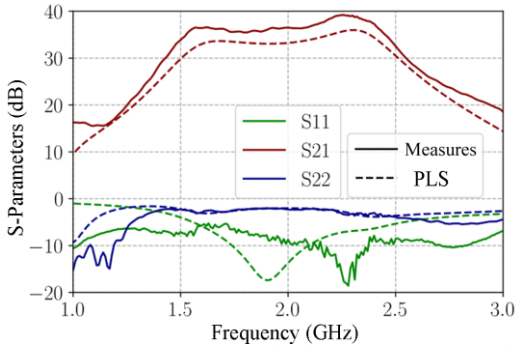



Figure 13. PA in 130nm PDSOI technology S-parameters post-layout simulation (PLS) and measurement performance.

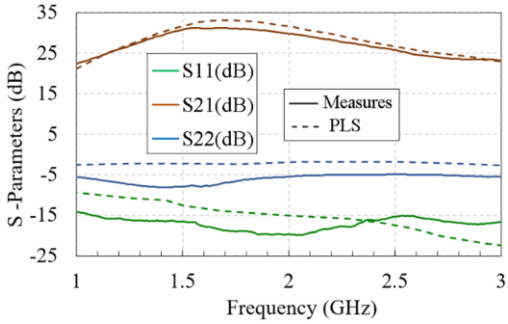



Figure 14. PA in 28nm FDSOI technology S-parameters post-layout simulation (PLS) and measurement performance.

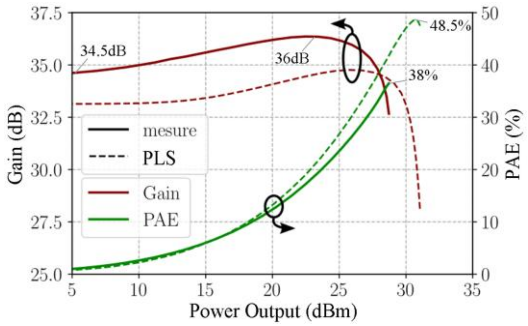



Figure 15. 130nm PA gain, PAE post-layout simulation, and measured performances in 1.85 GHz.

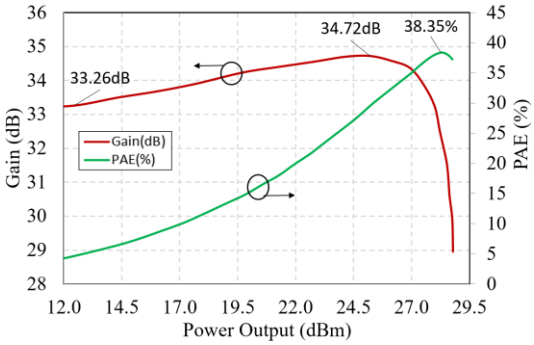



Figure 16. 28nm PA gain and PAE post-layout simulation performance in 1.85 GHz.

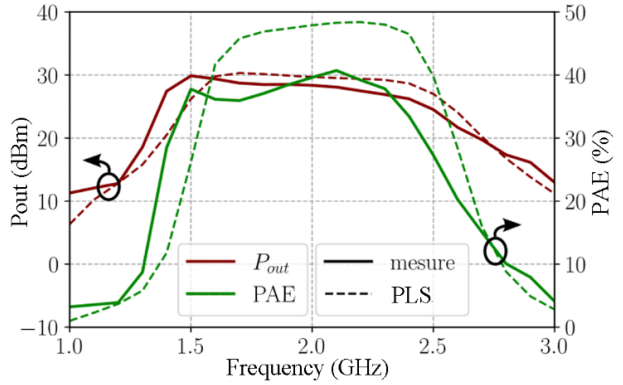



Figure 17. 130 nm PA Pout and PAE performances between 1 GHz and 3 GHz.

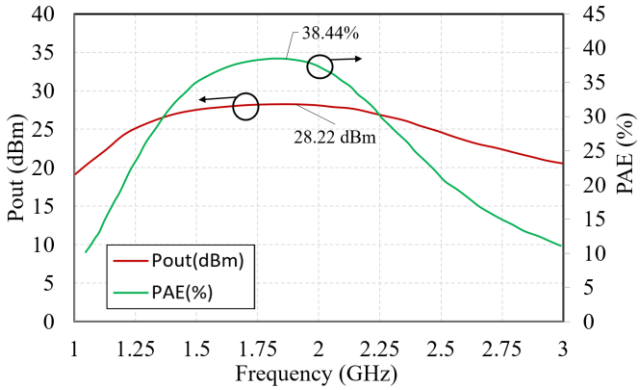



Figure 18. 28 nm PA Pout and PAE performances (PLS) between 1 GHz and 3 GHz.

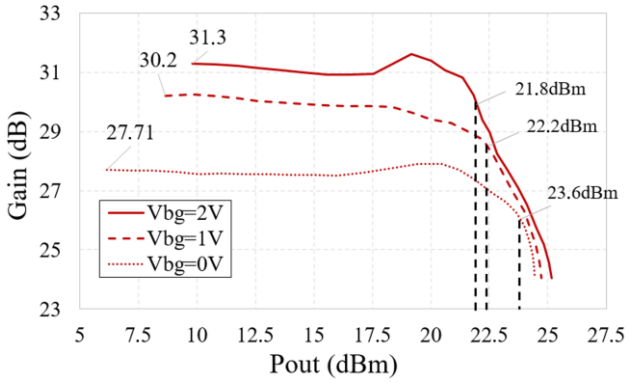



Figure 19. 28nm FDSOI PA gain versus $P_{out}$ measured performances for 3 levels of back-gate voltage.

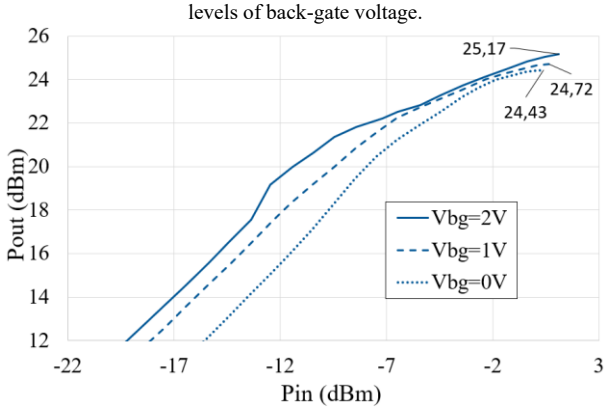



Figure 20. 28nm FDSOI PA Pout vs Pin measured performances for 3 levels of back-gate voltage.

The gain and PAE performances related to the frequency sweep from 1 GHz to 3 GHz for the 130 nm and 28 nm PA are presented in Figs. 17 and 18, respectively. The 130 nm PA exhibits a maximum Pout between 25 dBm and 30 dBm in the frequency range from 1.4 GHz to 2.5 GHz, with measurement results closely matching those of PLS. A maximum PAE between 37% and 40% is observed from 1.5 GHz to 2.4 GHz. The 28 nm PA presents a maximum Pout of 28.22 dBm and a maximum PAE of 38.44% at 1.85 GHz.

### *B. Fine Tuning Gain with Back Gate Transistor Bias in 28nm FDSOI Technology*

In CMOS SOI technology, access to the transistor's back-gate provides additional control over the device's characteristics that can be leveraged to modify key performance parameters of a PA, such as output power, gain, and PAE. Changing the back-gate bias (*Vbg*) effectively modulates the transistor's threshold voltage *Vth*. A lower threshold voltage can increase the transistor's current driving capability, potentially enhancing the power output and, depending on the biasing conditions, the gain. However, this can also lead to higher power consumption and decreased efficiency.

The measured performance of gain versus $P_{out}$ and $P_{out}$ versus $P_{in}$ for the PA in 28 nm with three different levels of *Vbg* voltage are presented in Figs. 19 and 20. For *Vbg=2V,* the transistors are more biased for maximum conduction, resulting in the highest initial gain of 31.3 dB and a curve with the typical shape of a class AB PA, reaching 21.8 dBm of linear output power. A *Vbg=1V* offers a more balanced operation, with a lower initial gain (30.2 dB) but greater linearity up to higher output power levels (*OCP1*=22.2 dBm). Meanwhile, *Vbg=0V* shows the lowest gain (27.7 dB) due to reduced transistor conduction, but the highest linear output power (*OCP1*=23.6 dBm). Despite the difference in maximum linear power output among the three bias setups, the maximum saturated power outputs are between 24.43 dBm and 25.17 dBm.

These results demonstrate how the back-gate voltage in 28nm FDSOI technology can be leveraged to optimize amplifier performance according to specific requirements for gain and linearity.

### *C. 130nm and 28nm Power Amplifier Comparative Analysis*

This subsection presents a comparative analysis of the two PAs in terms of size and performance. As seen earlier at the start of the results section, the PA implemented in 28 nm technology occupies an area corresponding to 34% of the area occupied by the PA in 130 nm technology.

By integrating the balun functionality directly into the cascode input stage, the design removes the need for an external passive balun. This element typically occupies a significant portion of the RF front-end layout. Passive baluns rely on inductors and transformers with relatively large

TABLE I. COMPARING WITH THE STATE-OF-ART

| Ref. | Freq. (GHz) | Psat (dBm) | P1dB (dBm) | PAE max (%) | PAE 6dB (%) | Gain (dB) | Topology | Technology | Supply (V) |
|---|---|---|---|---|---|---|---|---|---|
| [28] | 2.3 | 32.8 | 32 | 59 | 40 | 27.5 | LDMOS Doherty | 130nm SOI** | 3.4 |
| [29] | 2.4 | 35.1 | 34 | 53 | | 29.5 | Doherty | 130nm SOI | 5 |
| [23] | 1.95 | 30.5 | 29.7 | 53 | 40 | 26.5 | Doherty | 180nm SOI | 4 |
| [24] | 1.85 | 31.9 | N/A | 56.2 | | 14.2 | ET PA | 180nm bulk | 4 |
| [27] | 2.6 | 33.1 | N/A | 43.5 | N/A | 28.1 | 4-stack E/Fodd | 45nm SOI | 3 |
| [25] | 2.4 | 30.3 | N/A | 36.5 | 29.1 | N/A | C-commuted | 40nm Bulk | 2.4 |
| [22] | 2.4 | 31.6 | N/A | 49.2 | | N/A | Digital Outphasing | 45nm bulk | 2.4 |
| [26] | 1.85 | 30.7 | 28.8 | 44.4 | 28 | 11 | Quasi-Doherty | 180nm SOI | 3 |
| **PA 130*** | **1.85** | **32** | **30** | **49** | **26.6** | **34** | **Cascode Classe-AB** | **130nm PDSOI** | **5** |
| **PA 28*** | **1.85** | **28.8** | **28.3** | **38.5** | **20.8** | **33** | **Triple stack Classe-AB** | **28nm FDSOI** | **3** |

*PLS | **SOI with LDMOS option

geometries, which scale poorly in deep-submicron CMOS. Replacing them with an active balun not only reduces the overall silicon footprint but also enables a more compact and area-efficient PA architecture, which is particularly advantageous for highly integrated IoT and multi-antenna systems.

A comparative analysis between Figs. 13 and 14 shows that the PA based on 130 nm PDSOI technology outperforms the 28 nm FDSOI in terms of S-parameter performance. The *S21* gain of the 130 nm PA remains around 35 dB in the central range (1.6 to 2.3 GHz), while the 28 nm PA reaches 30 dB only in the range between 1.5 and 1.9 GHz. However, the *S22* and *S11* of the 28 nm PA are more negative (below -5 dB and -15 dB, respectively), indicating better impedance matching at the input and output, with lower signal reflection.

A performance comparison between PAs gain (dB) and PAE (%) through Figs. 15 and 16, considering the post-layout simulation, shows that the 130 nm PA achieves higher maximum output power (~31 dBm) than the 28 nm PA (~28.5 dBm), making it more suitable for high-power applications. Considering the PLS performance, the 130 nm PA achieved a saturated output power of 31 dBm and the 28 nm PA achieved approximately 28.5 dBm, making the 130 nm technology more suitable for high-power applications, as expected. The 130 nm amplifier also provides slightly higher gain at lower output power levels. Furthermore, the 130 nm PA shows superior PAE performance in PLS, achieving a maximum of 48.5%, while the 28 nm PA achieves 38.35%. Comparing measurements, Fig. 15 shows that the 130 nm PA achieves a $P_{sat}$ of 28.82 dBm and a P1dB of 27.29 dBm, while the 28 nm PA, in Fig. 16, reaches a $P_{sat}$ of approximately 25.5 dBm and a $P_{1dB}$ of 23.6 dBm.

Although the performance values of the circuit made with 130 nm technology are higher, the circuit in 28 nm technology allows for adjustments in gain and linearity performance through back-gate voltage. This enables the choice to operate in either a high-gain mode or a high-linearity mode, depending on the communication requirements.

### D. State-of-the-Art Analysis

A comparison with the state of the art is conducted to conclude the performance assessment of the PAs presented in this section. Table I summarizes the state-of-the-art PAs and the performance metrics of the PAs developed in this research.

Considering 5G and NB-IoT applications that require modulations with high PAPR, the comparison was primarily made with promising topologies and techniques, such as Doherty and Envelope Tracking, as well as other high-efficiency classes.

It is observed that the two developed PAs outperform all PAs in Table I in terms of gain. Regarding *Psat*, the PA in 130 nm outperforms the works [22] [23] [24] [25] [26]. Regarding PAE, the PA in 130 nm outperforms the works [25] [26] [27], and the PA in 28 nm outperforms the work [25].

Regarding output power, the developed PAs are promising, as they are being compared with Doherty PAs, which consist of two or more PAs in parallel. If double the power were considered for the presented PAs, they would be comparable to Doherty's maximum power-level topologies.

The 130nm PDSOI pseudo-differential PA demonstrates an overall performance superior to the 28nm FDSOI design. PAs in [28] and [29] use off-chip passive components, which enhance performance due to significantly higher-quality factors than integrated passives. The PA architecture in [24] employs an envelope tracking technique, yielding a substantial improvement in PAE. Lastly, PA [25] is based on a switched amplifier architecture, enabling higher power density.

The PA designed in 28nm FDSOI is competitive in terms of state-of-the-art performance; however, the low quality factor of integrated passives tends to reduce the maximum achievable PAE.

## V. CONCLUSION

This paper compared two PAs implemented in 130 nm PDSOI and 28 nm FDSOI technologies and targeted at low-power RF applications. The results section presented a detailed analysis of their S-parameter responses, gain, PAE, output power, frequency behavior, and, for the 28 nm PA, the impact of back-gate biasing.

The paper compares passive elements of both technologies through the resistivity of metal layers, capacitances, and inductances. It also compares active components (transistors), showing that the 130 nm PDSOI technology has much thicker layers than the 28 nm FDSOI technology, making it more suitable for power emission. However, the 28nm technology also enables this functionality while occupying three times less space, albeit at a considerably higher cost and with lower

performance, given its primary orientation towards digital circuits.

Both PAs are composed of a gain stage (driver) and a power stage (power amplifier, PA), utilizing differential and cascode topologies. The PA implemented in 28 nm technology features a 3-stacked transistor in its power stage, allowing for a higher drain bias voltage. This adjustment was deemed fair within the functional comparison, as the technology features thinner layers, necessitating such adaptations. Details about the interstage matching wideband transformer of both circuits were presented, and the cascode active balun circuit on the 28 nm PA was detailed.

Performance graphs were presented for S-parameters, PAE, gain, Pout, frequency sweep, and different biasing setups for the back-gate voltage in the 28 nm technology. The results indicate that the performance of the circuit fabricated in 130 nm technology is superior to that of the 28 nm circuit.

The 28 nm FDSOI technology enables fine-tuning of the PA's gain through back-gate voltage, thus providing additional operational freedom. The two employed technologies, 130 nm and 28 nm, can produce PAs suited for the intended application.

The developed PAs exhibit superior gain performance compared to the state-of-the-art. They are promising in power when used in efficiency-boosting topologies that combine multiple PAs to increase PAE at backoff and maximize output power.

For future research, it is suggested that we explore the use of these PAs in efficiency-enhancing topologies and power-combining strategies, such as Doherty and Envelope Tracking, to facilitate comparisons with the state-of-the-art and contribute to the development of circuits for 5G and NB-IoT applications.

## ACKNOWLEDGMENT

This study was financed in part by the project Beyond5 and by the *Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil* (CAPES) - Finance Code 001.

## REFERENCES

[1] M. L. Carneiro, T. LeCocq, E. Kerherve, M. Matos, T. Taris and J. Pham, *Comparative Analysis of 130nm PDSOI and 28nm FDSOI Technologies for 5G Power Amplifier Applications,* The Twenty-First International Conference on Wireless and Mobile Communications (ICWMC 2025) - IARIA, v.21, pp. 10 - 15, Lisbon, 2025.

[2] K. Mekki, E. Bajic, F. Chaxel and F. Meyer, *Overview of Cellular LPWAN Technologies for IoT Deployment: Sigfox, LoRaWAN, and NB-IoT,* IEEE International Conference on Pervasive Computing and Communications Workshops (PerCom Workshops), pp. 197–202. doi: 10.1109/PERCOMW.2018.8480255, 2018.

[3] G. K. Celler and S. Cristoloveanu, *Frontiers of Silicon-on-Insulator,* Journal of Applied Physics, vol. 93, pp. 4955–4978, 2003.

[4] H. Mendez, *Silicon-on-Insulator, SOI Technology and Ecosystem, Emerging SOI Applications,* April, 2009.

[5] A. Chen, *Advances in Semiconductor Technologies: Selected Topics Beyond Conventional CMOS,* Wiley-IEEE Press, 2023.

[6] A. S. Gillis, *What is the Internet of Things (IoT)?,* Available: https://www.techtarget.com/iotagenda/definition/Internet-of-Things-IoT. [Accessed: Mar. 28, 2023], 2014.

[7] Telefonaktiebolaget LM Ericsson, *What is 5G? How will it transform our world?,* Available: https://www.ericsson.com/fr/5g. [Accessed: Mar. 30, 2023], 2021.

[8] P. Wegner, *Global IoT market size to grow 19% in 2023 - IoT shows resilience despite economic downturn,* Available: https://iot-analytics.com/iot-market-size. [Accessed: Mar. 28, 2023], 2023.

[9] Thales Group, *Massive IoT: Tech overview, business opportunities and examples,* Available: https://www.thalesgroup.com/en/markets/digital-identity-and-security/mobile/massive-iot. [Accessed: Mar. 30, 2023], 2022.

[10] GSMA Mobile IoT Industry Alignment group, *3GPP Low Power Wide Area Technologies,* Svetlana Grant (GSMA), September, 2016.

[11] A. T. Prittu and M. Mathurakani, *SC-FDMA -An Efficient Technique For PAPR Reduction In Uplink Communication Systems -A Survey,* IJRET: International Journal of Research in Engineering and Technology, Volume: 03 Special Issue: 01 | NC-WiCOMET-2014, 2014.

[12] ETSI, *LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing (3GPP TS 36.521-1 version 16.8.1 Release 16),* Available: https://www.etsi.org/deliver/etsi_ts/136500_136599/13652101/16.08.01_60/ts_13652101v160801p.pdf. [Accessed: Mar. 31, 2023], 2021.

[13] GSM Association, *NB-IoT Deployment Guide to Basic Feature set Requirements,* June, 2019.

[14] Ixia, *SC-FDMA, Single Carrier FDMA in LTE,* 915-2725-01 Rev A, November 2009.

[15] H. G. Myung, J. Lim and D. J. Goodman, *Peak-To-Average Power Ratio of Single Carrier FDMA Signals with Pulse Shaping,* IEEE 17th International Symposium on Personal, Indoor and Mobile Radio Communications, pp. 1–5. doi: 10.1109/PIMRC.2006.254407, 2006.

[16] N. Alfaraj, *SIMOX vs. Smart-Cut: A Brief Overview of the Silicon-on-Insulator Technology,* doi: 10.13140/RG.2.2.10340.27522, January, 2018.

[17] Renesas Electronics, *Semiconductor Reliability Handbook,* R51ZZ0001EJ0250 Rev. 2.50, January, 2017.

[18] A. D. Pham, *Biasing Techniques for Linear Power Amplifiers,* Ph.D. dissertation, Massachusetts Institute of Technology, Available: https://api.semanticscholar.org/CorpusID:112109794, May, 2002.

[19] IBM Corporation, *BEOL Process Challenges - Emerging CMOS Technology at 5 nm and Beyond,* IEDM 2015 Short Course, Albany Nano Tech Center, NY, USA, 2015.

[20] B. Leite, *Design and modeling of mm-wave integrated transformers in CMOS and BiCMOS technologies,* University of Bordeaux, 2011BOR14359, PhD Thesis, address: http://www.theses.fr/2011BOR14359/document, 2011.

[21] Y. Sim, J. Park, J. Yoo, C. Lee and C. Park, *A CMOS power amplifier using an active balun as a driver stage to enhance its gain,* Microelectronics Journal, vol. 63, 05, 2017.

[22] A. Banerjee, L. Ding and R. Hezar, *A High Efficiency Multi-Mode Outphasing RF Power Amplifier With 31.6 dBm Peak Output Power in 45nm CMOS,* IEEE Transactions on Circuits and Systems I : Regular Papers, vol. 67, no 3, pp. 815-828, doi: 10.1109/TCSI.2019.2954068, 2020.

[23] P. Draxler and J. Hur, *A Multi-Band CMOS Doherty PA with Tunable Matching Network,* IEEE MTT-S International Microwave Symposium (IMS), pp. 944–946. doi: 10.1109/MWSYM.2017.8058742, 2017.

[24] S. Jin, B. Park and K. Moon, *A Highly Efficient CMOS Envelope Tracking Power Amplifier Using All Bias Node Controls,* IEEE Microwave and Wireless Components Letters, vol. 25, no. 8, pp. 517–519, 2015.

[25] B. Yang, H. J. Qian and X. Luo, *26.5 A Watt-Level Quadrature Switched/Floated Capacitor Power Amplifier with Back-Off Efficiency Enhancement in Complex Domain Using Reconfigurable Self-Coupling Canceling Transformer,* IEEE International Solid-State Circuits Conference (ISSCC), pp. 362-364. doi :10.1109/ISSCC42613.2021.9366029, 2021.

[26] K. Kim, D.-H. Lee and S. Hong, *A Quasi-Doherty SOI CMOS Power Amplifier With Folded Combining Transformer,* IEEE Transactions on Microwave Theory and Techniques, vol. 64, no 8, pp. 2605-2614, doi : 10.1109/TMTT.2016.2577584, 2016.

[27] M. Khorshidian and H. Krishnaswamy, *A Fully-Integrated 2.6GHz Stacked Switching Power Amplifier in 45nm SOI CMOS with >2W Output Power and 43.5% Efficiency,* IEEE MTT-S International Microwave Symposium (IMS), pp. 323–326, 2019.

[28] A. Serhan, D. Parat and S. Gerardin, *A Reconfigurable SOI CMOS Doherty Power Amplifier Module for Broadband LTE High-Power User Equipment Applications,* IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 79–82. doi: 10.1109/RFIC49505.2020.9218305, 2020.

[29] P. Reynier, A. Serhan, D. Parat and S. Gerardin, *A High-Power SOI-CMOS PA Module with Fan-Out Wafer-Level Packaging for 2.4 GHz Wi-Fi 6 Applications,* IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 59–62, 2021.

[30] T. Shen, W. Zhang, K. B. Yeap, J. Tan and P. Justison, *An Investigation of Dielectric Thickness Scaling on BEOL TDDB,* IEEE International Reliability Physics Symposium, pp. 3A.2.1–3A.2.6. doi: 10.1109/IRPS.2015.7112698, 2015.

[31] Y. Eo and K. Lee, *High Efficiency 5GHz CMOS Power Amplifier with Adaptive Bias Control Circuit,* IEEE Radio Frequency Integrated Circuits (RFIC) Systems, Digest of Papers, pp. 575–578. doi: 10.1109/RFIC.2004.1320686, 2004.