Overview of Experimental Module CANDARMA

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Abstract— **The purpose of this study is to present a Real Time Operating System embedded ARM-7 microcontroller-based module, CANDARMA. CANDARMA is an experimental payload module settled in low earth orbit remote sensing satellite. The significance of CANDARMA comes from the various experimental applications performed on it. These studies include usage of an ARM-7 architecture based microcontroller, running a Real Time Operating System on the microcontroller, experiencing two different high speed analog to digital converters and various integrated circuits, which will bring in knowledge for future satellite designs. This paper describes CANDARMA's implementation key points and benchmarks in details which can be used in analog and imaging applications in satellite systems.**

Keywords-Satellite; Microcontroller; Real Time Operating System; Space Heritage

I. INTRODUCTION

Turkey has made investments on space activities by setting off some satellite projects in the last decades. RASAT [1], one of the satellite projects of Turkey, is an outcome of these investments and will be an imaging satellite for civil purposes. RASAT is the second remote sensing satellite of Turkey and a TUBITAK-UZAY product and is planned to be launched in February-2011. Basic specifications of RASAT are given in Table 1 [2].

With the advance of technology, capabilities of microcontrollers have increased coarsely; they got faster and faster, became more equipped with addition of new developed peripherals. Today, an enhanced microcontroller can run up to Ghz's levels (TI- AM3703-1000 – 1 Ghz, Intel-i7-960 - 3.20 GHz) [3][4] and be loaded with various peripherals (TI-AM1707 - EDMA3, Three Configurable 16550 type UART, Two Serial Peripheral Interfaces (SPI), Multimedia Card (MMC)/Secure Digital (SD), Card Interface with Secure Data I/O (SDIO), USB 2.0 OTG Port With Integrated PHY, Three Multichannel Audio Serial Ports, 10/100 Mb/s Ethernet MAC, Three Pulse Width Modulators, etc.) [5].

TABLE 1. TECHNICAL SPECIFICATIONS OF RASAT

Turkish EO Satellite	RASAT
Orbit	700 km circular, sun synchronous
Weight	93 kg
Spatial resolution	Panchromatic: 7.5 m Multispectral: 15 m
Expected life time	5 years
Swath width	30 km
Payloads	**Optical payload:** A pushbroom type imager **BiLG**E: Flight computer **GEZGiN-2:** Image process and compression module **X-Band:** High speed Transmitter Module **CANDARMA**: An Experimental ADC and Microcontroller Test Module

Development in microcontrollers' features lead to higher expectations from microcontrollers. Due to the fact that the internal ROM and RAM have been large enough, engineers quitted using external RAM and ROM in applications. Increase in the operating frequency results in handling more tasks, and providing the capability to run RTOS with high performance controllers.

Design engineers all around the world take the advantage of advances from the development of new architectures and increasing capabilities. Examples of new generation microcontrollers' usage can be seen in the new satellite projects. For instance, AT91SAM7A3 which is an ARM-7 architecture microcontroller has taken place in the ADCS part of AAUSAT3 [6].

AT91M55800A another ARM-7 family microcontroller was used in SwissCube satellite which was launched in 2009 [7]. Together with AT91M55800A, 16-bit TI-MSP430F1611 controller was also used in the CDMS (Control & Data Management System). While MSP430F1611 is being used for some communication work, AT91M55800A has been used for the most of the work because of its processing capability [8]. GP4020 another ARM7TDMI controller was also used in PROBA-2 Spacecraft in 2008 [9].

In imaging satellites, speed and accuracy are the most important criteria which directly affect resolution of the imaging unit. Engineers who want to design high resolution imaging satellites have to use new- generation analog to digital converter (ADC) integrated circuits (ICs), because usually newly designed ADC outclasses its formers by means of speed and accuracy.

The main handicap with using a new generation advanced IC is to find sufficient support for the product. Space Heritage is another critical issue in space applications. Using an IC that had never been experienced in space is always taking a risk. CANDARMA is designed to serve its benefit on that issue. After working successfully in space conditions, our new ICs will have space heritage

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and they will be trusted to use for further satellite electronics applications.

This paper will describe the structure of this module. In the next section functional and architectural overview of CANDARMA will be presented and following sections, the ADCs and microcontroller of the module, qualification tests will be explained in details. Finally, paper concludes with giving ideas about future work.

II. OVERVIEW OF CANDARMA

CANDARMA is designed simple while meeting all of our goals. The block diagram of CANDARMA is schematically explained in Figure 1.

It is connected to satellite system by power and CAN bus. Module itself is supplied with unregulated 28 V and produces necessary 5V and 3.3V in the inner stages.

Functionality of CANDARMA can be divided into two main steps; CAN communication and Analog to Digital Conversion. First of all, a number for the test purpose is sent over CAN-Bus. Microcontroller picks and processes sent-data, produces an appropriate analog voltage proportional to the sent-number with the help of internal DAC module. DAC output voltage is amplified by voltage amplifier LM6646. Amplified voltage is transferred to both ADCs as an input. After conversion, most significant 8-bits of the ADCs are read by the controller at a rate of 1 Mhz and compared with the number sent over CAN. Read value is then sent back over CAN-Bus allowing us to check conversion accuracy, when needed. In this operation, necessary clocking signals for the ADCs are generated by the controller. By this functionality loop, CAN connection, basic operation and DAC channels of the controller were checked besides ADC ICs and voltage amplifier LM6646.

III. ARM-7 BASED MICROCONTROLLER

8051 core architecture was developed in 1980 by Intel and gained popularity in industrial control applications after that time. With successful experiences in space missions, 8051 architecture dominated this field for years. Up to this date in space missions 8051 architecture based microcontrollers have been widely used all over the world. TUBITAK-UZAY also used to utilize Infineon C515 microcontroller for controller work in satellite electronics. C515 is an 8-bit 8051 architecture controller which has a strong space heritage. With developments in technology and increasing needs in applications, C515 is getting out of date day by day by means of running speed and application features.

LPC2378 microcontroller, which is thought to replace C515, is a product of NXP Company. CANDARMA is connected to Satellite Can-Bus with a baud rate of 388kbit/sec with the help of LPC2378 microcontroller. This 32bit microcontroller is not radiation hardened. LPC2378 has two Can-Bus channels providing us to connect CANDARMA to primary and secondary CAN buses of the satellite at the same time.

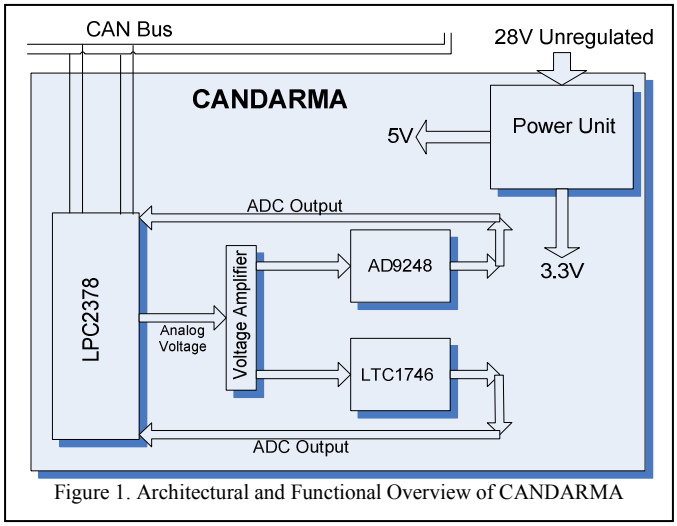

Figure 1. Architectural and Functional Overview of CANDARMA

Specifications, in which LPC2378 is better than C515 are not limited to only number of CAN Bus channels. Table 2 compares C515 and LPC2378 by means of technical specifications.

LPC2378 is faster than C515 by means of maximum oscillator frequency, but this is not the whole case. Our C515 microcontroller model has a MIPs rate of 1.66 while LPC2378 having a rate of 64 Dhrystone MIPs.

The difference between the sizes of on-chip ROMs is noticeable. Due to the limited internal ROM space of C515, an external ROM was used to store the software in our earlier applications. This solution brought in lots of burden. In order to drive the external ROM, some components as latch, inverter, capacitors and resistors were used. External components also makes memory mapping complicated, because the number of components increases, reliability of system decreases and test – manufacturing – maintenance gets harder. LPC2378 Internal ROM is exceedingly big enough for our firmware and data, which will ease our job in various ways and increase reliability.

High speed operating capability and large storage size enabled us to embed A Real Time Operating System. MicroC/OS II, is used as RTOS. All of the controller tasks, while running under MicroC/OS II, were subjected to various functionality tests, software crash never occurred.

Our satellite systems have two CAN-Buses and C515 has one CAN-Bus; therefore, a mechanical relay is included for switching between CAN-Buses. By use of dual CAN-Bus channel of LPC2378 there is no need for a mechanical switch and its peripheral components.

LPC2378 is able to boot load a new code sent by packets over CAN Bus. HY628100 is included in the design for RAM operations of RTOS and bootload. That bootloader is tested and verified while running under MicroC/OS II.

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TABLE 2. COMPARISON OF C515 & LPC2378

	C515	LPC2378
Architecture	8051	ARM7
Structure	8 bit	32 bit
Processor frequency	Up to 24 MHz	Up to 72 MHz
MIPS*	1.66 MIPs**	64 Dhrystone MIPs
Operating modes	Single 8 bit mode	16-bit Thumb mode 32-bit ARM mode
On-chip ROM	8 Kbyte	512 Kbyte
On-chip RAM	256 byte on-chip RAM	32 kB of SRAM on the ARM local bus-CPU access 16 kB SRAM for Ethernet interface*** 8 kB SRAM for USB***
ADC	8- bit ADC	10-bit ADC
I/O Pins	48 I/O pins	104 I/O pins
Peripherals	Three 16-bit timer/counters	Four 16-bit timer/counters
	Watchdog timer	Watchdog timer
	12 interrupt sources	32 vectored interrupts
	SPI controller.	SPI controller.
	1 UART Channel	4 UART Channels
	Single channel CAN controller	CAN controller with two channels
	-	USB 2.0 full-speed device with on-chip PHY and associated DMA controller
	-	Four UARTs
	-	Ethernet MAC with associated DMA controller
	-	Two SSP controllers
	-	Three I2C-bus interfaces
	-	I2S (Inter-IC Sound) interface
	-	SD/MMC memory card interface
	-	10-bit DAC.

* Million instructions per second
** For C515C-8R / -8E
*** Can also be used as general purpose SRAM.

IV. ANALOG DIGITAL CONVERSION ICs

CANDARMA also includes two types of high speed AD Converters; AD9248 and LTC1746. AD9248 is a dual input ADC and can operate up to 65 Msps without missing any conversion. LTC1746 is a low power ADC and can operate up to 25 Msps. Both ADCs can make conversions up to 14 bits of precision. Similar ADCs with the used ones in this module were subjected to radiation tests in [10]. According to the results 9-bits precision can be obtained after 20 krad(Si) total dose radiation. In CANDARMA by using the DAC channel of microcontroller analog signals are produced and supplied as an input to the ADCs. By comparing the input analog signal and output digital signal, CANDARMA provides data about errors and deviations from expected results.

V. QUALIFICATION TESTS PERFORMED

CANDARMA was subjected to thermal and thermal-vacuum tests while functionality test results being logged continuously.

Single- cycle thermal vacuum test and 7-cycles thermal tests are performed in TUBITAK-UZAY thermal chamber. Thermal chamber and thermal- vacuum chamber are both capable of meeting ECSS-E-10-3A testing standards.

A. Thermal – Vacuum Test

Thermal testing of CANDARMA consists of two phases: in the first phase CANDARMA is exposed to 10^{-6} mbar vacuum and temperatures of -40 ^{0}C up to +60 ^{0}C. Thermal vacuum temperature log graph is shown in Figure 2.

Temperature values are also measured with the help of temperature sensors as can be seen from Figure 3. fixed on different parts of the module. Maximum and values logged on CANDARMA are listed in Table 3.

B. Thermal Tests

This phase consists of 7 thermal cycles. In this phase no thermal sensors are placed on CANDARMA module. Thermal chamber temperature altered between -40 ^{0}C and +60 ^{0}C with time, as can be seen in Figure 4.

During the test, module is also subjected to functionality test. ADC reads and CAN communication is logged during the test. The voltage to be generated by DAC of microcontroller is sent from CAN-Bus, the generated analog voltage is converted by ADCs and read back by microcontroller. The read data is sent back over CAN-Bus and logged by PC.

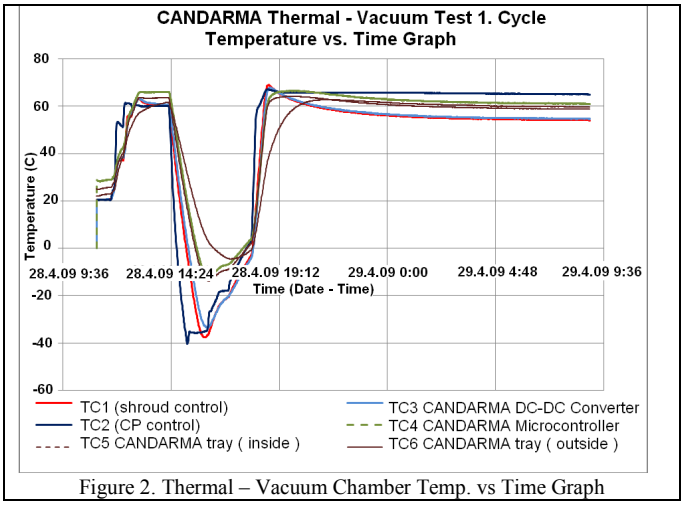

Figure 2. Thermal – Vacuum Chamber Temp. vs Time Graph

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Figure 3. Temperature sensors mounted on CANDARMA

No software crash was observed during the tests. No deviation was observed for the most significant 8-bit readings. CAN-Bus check is done 10 times per second. Can-Bus connection was never lost.

VI. CONCLUSION AND FUTURE WORK

In this paper, experimental module CANDARMA was presented. Functionality of the module and functionalities of included ICs are explained.

After having a successful experience of space experience, this microcontroller will gain reliability and other design engineers will be confident for using other features like Ethernet, I²S, I²C, USB etc. Real Time Operating System will be tested with LPC2378 and will also be verified to work in space conditions with this microcontroller.

This experimental work is expected to bring in significant experience and knowledge in various fields. With accomplishment of this work LPC2378 and ADCs will gain space heritage.

TABLE 3. MINIMUM AND MAXIMUM VALUES OBTAINED DURING THERMAL – VACUUM TEST

Thermal Sensor	Position	Maximum Temperature (C)	Minimum Temperature (C)
TC1	Shroud control	68.88	-37.64
TC2	Cold plate control	67.03	-40.31
TC3	CANDARMA DC-DC converter	67.73	-33.61
TC4	CANDARMA Microcontroller	66.46	-5.71
TC5	CANDARMA tray (inside)	64.21	-1.75
TC6	CANDARMA tray (outside)	62.01	-17.61

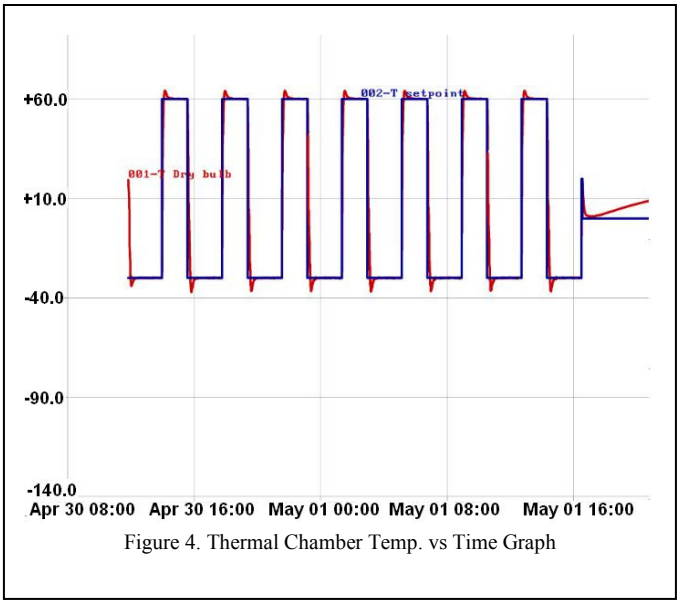

Figure 4. Thermal Chamber Temp. vs Time Graph

For future work, embedding the ARM controller in a radiation hardened FPGA for a satellite module is being planned.

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