Physical Layer Simulation of Large Distributed Automation Systems in SPICE

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***Abstract*—In this paper, we propose an analysis of the physical layer of large distributed automation systems based on simulation in SPICE. For large systems, changes of the physical topology or minor modifications of the physical layer hardware of a bus node result in much more increased influences to the signal integrity compared to smaller system architectures. The simulation provides references for further designs of the physical layer hardware of a bus node and an analysis of its behavior in different large topology configurations with up to 1000 bus nodes in a network with a total length of up to 1000 meters.**

Keywords- large distributed automation systems; physical layer simulation; signal integrity; fieldbus simulation

I. INTRODUCTION

Due to the increase in performance and the cost reduction of micro-processors, the decentralized approach of automation systems is used more and more in the last years. Furthermore, current developments of automation systems focus on distributed systems to handle modular extensibility and to avoid isolated applications. The decentralized approach suggests a connection of each sensor and actuator to a bus system via a bus coupler. As a result a large distributed automation system is generated, of which behavior is dependent on a high number of influence factors, based on the complex structure of the transmission channel system and the large number of bus participants.

Current research on physical layer simulations in works mainly in the field of automotive bus systems ([1]-[6]) or focused on lower scale case studies ([7], [8]). In this paper the focus lies on more complex bus system topologies, for example hardware architectures in decentralized building automation systems, which contain more than 1000 bus couplers which are networked in a transmission channel system of up to 1 km without a repeater. Changes of the physical topology or minor modifications of the physical layer hardware of a bus node, such as stub lines, mismatches or unsuitable dimensioning, could cause a negative influence to the signal integrity. A simulation based analysis is essential for this kind of large distributed automation systems.

Based on the fieldbus system SmallCAN ([9] and [10]), developed at the Institut for traffic safety and automation engineering, Technische Universität Braunschweig, the signal integrity for a large distributed automation system is validated by a physical layer simulation in SPICE.

Therefore, the main components models of the mentioned automation system and their connection to a large distributed system are described in section 2 of this paper.

In section 3 the main requirements for a sufficient signal integrity behavior in SmallCAN are introduced.

In section 4 the results are shown after simulation. Next to specific complex topology configurations with up to 1000 bus participants, the influence of modifications of the physical layer hardware of a bus node is also be analyzed.

II. Simulation model

To simulate the data transmission system for SmallCAN, three main components of the data transmission system are modeled in SPICE:

- energy supply unit.
- physical layer hardware of a bus coupler.
- transmission channel system.

The energy supply unit provides a recessive signal level of 24 V for the data line and a constant current source which impresses a current of 250 *mA* in case of a forced dominant signal level. The developed model *ENERGY_SUPPLY_UNIT* supports three ports for ground, input power supply and data line.

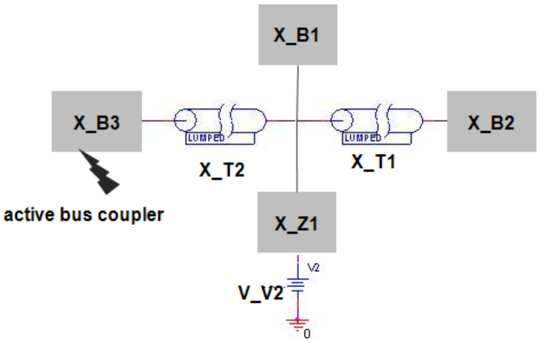
The dominant signal level is caused by short-circuiting the data line to the ground, executed by a MOSFET-Transistor of an active bus coupler. The developed model *BUS_COUPLER* represents a bus coupler with the logical input port for transmitting data, the data line of the bus, ground and the logical output port for the receiving data.

The transmission channel system of SmallCAN considers the electrical parameters for a typical phone cable:

- capacitance per unit $\mathrm{C}' = 55\ \frac{\mathrm{pF}}{\mathrm{m}}$.
- resistance per unit $\mathrm{R}' = 0{,}05\ \frac{\Omega}{m}$.
- inductance per unit $\mathrm{L}' = 0{,}075\ \frac{uH}{m}$.

For the transmission channel system the SPICE model TLUMP128 is used. The individual models of the components are connected to a whole system model of the specific hardware architecture, described by a SPICE net list. The physical topology can be chosen free, as long as the total cable length is lower than 1000 m.

Figure 1 shows a minimal topology with 3 bus couplers at a maximum distance of 3 *m* and the accordance net list. Two phone cables with 1 *m* and 2 *m* are connected between the energy supply unit X_Z1 and the bus couplers X_B2 and X_B3. A pulse, generated by the voltage source V_V3, controls the logical input port of bus coupler X_B3 to trigger the dominant signal level on the bus. The energy supply unit feeds in a current of 250 *mA* in the data line in the direction of the active bus coupler X_B3.



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V_V2  1        0                                    30Vdc
X_Z1  0        2    1                               ENERGY_SUPPLY_UNIT
X_B1  TX_1       2      0           RX_1            BUS_COUPLER
X_T1    3   2    GND_1  TLUMP128  PARAMS: R=0.05 L=0.075u C=55p  LEN=2
X_B2  TX_2      3      GND_1   RX_2                 BUS_COUPLER
X_T2    4   2    GND_2  TLUMP128  PARAMS: R=0.05 L=0.075u C=55p  LEN=1
X_B3  EVENT  4      GND_2   RX_3                    BUS_COUPLER
V_V3 EVENT  GND_2  PULSE 0V 5V 1000u 10n 10n 0.1m 0.198m
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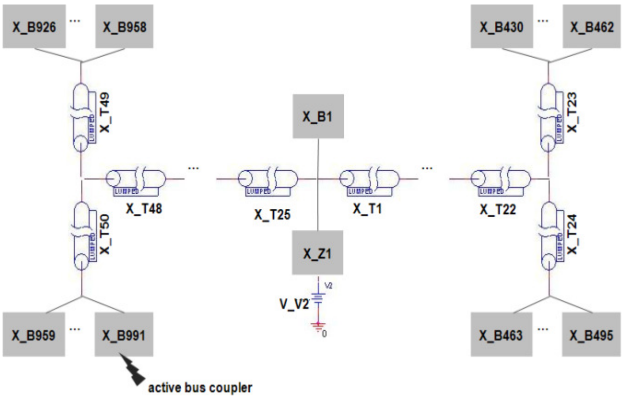
Fig. 1. Minimal scale hardware architecture and SPICE-net list.

In Figure 2 an example of a maximal periodically structured topology with 991 bus couplers of a total cable length of 1 *km* and a section of its net lists are depicted. The energy supply unit X_Z1 is placed in the middle of the system, from where two main lines were extended. Each following stub line has a length of 20 m. At each end of the stub line a network, composed of 33 bus couplers, is located.

III. Requirements

After short-circuiting, the following signal curve depends on signal integrity properties, such as reflection behavior and voltage changes. The following requirements have to be fulfilled for each topology configuration to guarantee a sufficient signal integrity behavior:

- The voltage drop between the data line and the ground has to be lower than 7 V / 500 m, which guarantees the recognition of the dominant signal by the receiver hardware.
- After the settling time and line delay time of 11,9 us the level signal on the data line has to be lower than the threshold voltage of 14 V during the falling edge and has to be overrun it during the rising edge, to ensure a stable signal trace before the signal sampling starts.



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V_V2  1        0                                    30Vdc
X_Z1  0        2     1                              ENERGY_SUPPLY_UNIT
X_B1  XX_1  2     0  20001                          BUS_COUPLER
X_T1    3   2      T1_0  TLUMP128   PARAMS: R=0.05 L=0.075u C=55p  LEN=20
…
X_T22   22  22  T23_0 TLUMP128   PARAMS: R=0.05  L=0.075u C=55p  LEN=20
X_T23   24  23  T24_0 TLUMP128   PARAMS: R=0.05  L=0.075u C=55p  LEN=20
    X_B430   XX_430    24  T24_0  20430             BUS_COUPLER
    …
    X_B462   XX_462    24   T24_0  20462            BUS_COUPLER
X_T25   25  23  T25_0 TLUMP128   PARAMS: R=0.05  L=0.075u C=55p  LEN=20
    X_B463   XX_463    25   T25_0  20463            BUS_COUPLER
    …
    X_B495   XX_495   25    T25_0  20495            BUS_COUPLER

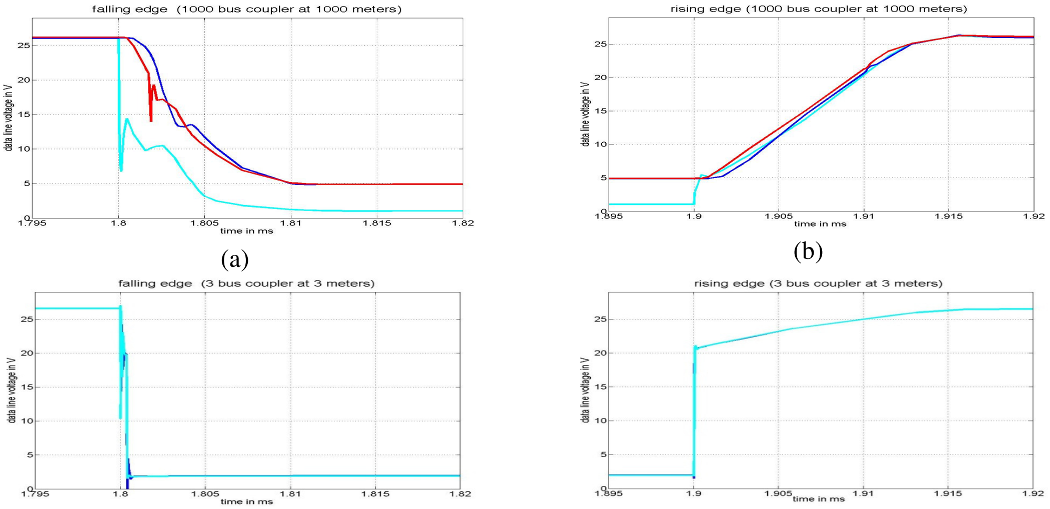
X_T25    26    2    T26_0   TLUMP128   PARAMS: R=0.05 L=0.075u C=55p  LEN=20
…
X_T48   50  48  T48_0 TLUMP128  PARAMS:  R=0.05  L=0.075u  C=55p LEN=20
X_T49   51  50  T49_0 TLUMP128  PARAMS:  R=0.05  L=0.075u  C=55p LEN=20
    X_B926 XX_926   51   T49_0    20926             BUS_COUPLER
    …
    X_B958 XX_958   51    T49_0  20958              BUS_COUPLER
X_T50    52  50  T50_0  TLUMP128  PARAMS:  R=0.05  L=0.075u  C=55p LEN=20
   X_B959  XX_959   52   T50_0    20959             BUS_COUPLER
   …
   X_B991     EVENT   52  T50_0    20991            BUS_COUPLER
V_V3 EVENT  T50_0 PULSE 0V 5V 1000u 10n 10n 0.1m 0.198m
```

Fig. 2. Large scale hardware architecture and section of the SPICE-net list.

IV. SIMULATION RESULTS

In Figure 3 (a),(b), the simulation results are depicted for the mentioned large distributed topology. For comparison an ideal trace for the minimal system with three bus couplers by a total cable length of 3 m is also depicted in Figure 3 (c),(d). The voltage between the data line and data ground is measured near the active bus coupler X_B991(cyan), near the energy supply unit at bus coupler X_B1 (red) and far from the active bus coupler at the bus coupler X_B495 (blue).

The simulation results show that the voltage drop between data line and ground is lower than the permitted value of 7 *V*. Due to the influence of the line capacity the signal trace results in a much flattened curve in contrast to the signal curve for the minimal system. It can be also seen that during the falling edge more signal levels are formed,



(a) (b)

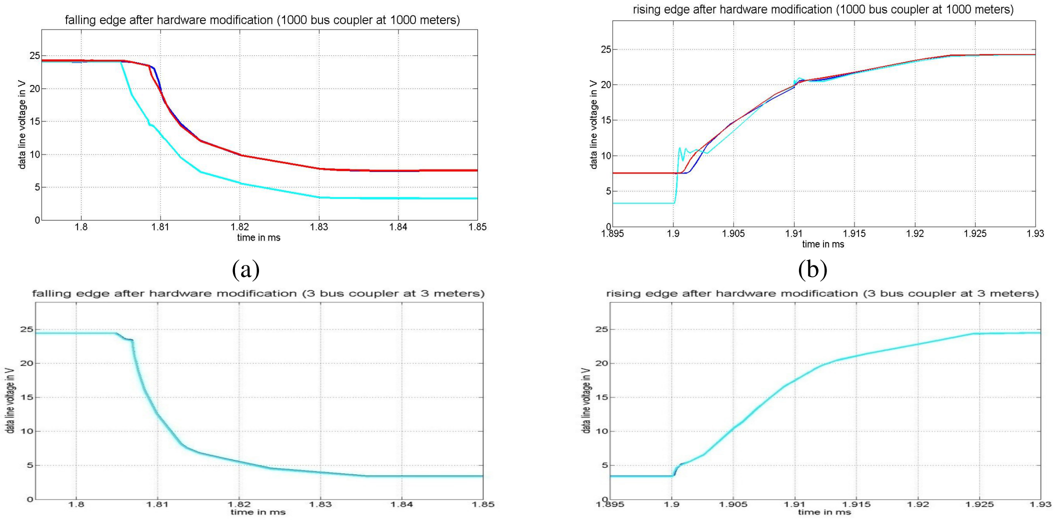
(c) (d)

Fig. 3. Simulation results for a large and minimal distributed topology.

due to the reflection behavior. After a line delay time of nearly 2,5 *us* and the settling time the signal is fall below the threshold voltage of 14 *V* within the permitted time of 11,8 *us*.

The trace of the steep edges, affiliated under minimal topology conditions, cannot be kept for extended topology configurations, due to the resulting flattened curve. Furthermore, for smaller system topologies the steep edges result in excessive emitted interferences. Therefore, some modifications of the physical hardware of the bus coupler are implemented to avoid the steep edges during signal level changes. By a delayed triggering of the output transistor, the current flow in the data line is impressed under controlled conditions to avoid the steep edges.

In Figure 4, the simulation results after the hardware modifications of the transmitter are depicted. Due to the controlled triggering of the output transistor, the signal behavior for the large distributed topology resembles more the signal behavior for the minimal system, compared to the simulation results of Figure 3. The mentioned signal integrity requirements are fulfilled and the reflection behavior is reduced. In summary it could be assumed, that for different topology configurations the signal trace on the data line is more predictable after the mentioned hardware modifications.



(a) (b)

(c) (d)

Fig. 4. Simulation results for a large and minimal distributed topology after hardware modification.

V. CONCLUSION AND OUTLOOK

The effort for a measurement based analysis of the physical layer of large distributed automation systems is extremely high and not practical. Therefore, a simulation based analysis for this kind of automation systems is proposed in this contribution. The main component models of an automation system and theirs variable connection by a topology net are described. The simulation results for different case studies show various signal behaviors, dependent on different bus topologies and modifications of the transceiver hardware. Variable parameters allow the analysis of signal integrity for different conditions. Generally, statements about the signal integrity for complex automation systems can be yielded by this simulation.

In further works, an optimized signal behavior for all conditions could be found by an automated modification of parameters, simulation execution and an analysis of the results. Monte Carlo simulations, offered by SPICE Tools, could be used for that.

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