Development of An Autonomous Time-synchronized Sensing System Capable of Measuring Acceleration and Images

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Abstract - **In Japan, the maintenance and management of aging bridges, highways, and other civil infrastructure and buildings is an important social issue. Proper maintenance and management require regular and highly accurate inspections, but these inspections rely on visual examinations by humans, which are expensive. Hence, to make this process more efficient, there is a need to automate inspections using sensing systems. Moreover, after a disaster, such as a major earthquake or a tsunami, it is necessary to expedite evacuation operations and rescue people, and for this purpose, the viability of or damage to each structure must be accurately evaluated using a sensing system. To meet these challenges, research and development is being carried out on an autonomous time-synchronized sensing system. The system adds high-precision time information to measurement data, acquires and analyzes digital sensor data that are time-synchronized, and uses it to automate inspections. As a first step in this research, a sensor device was developed that performs autonomous time-synchronized sensing using a digital high-precision accelerometer. As a second step, a heterogeneous digital sensing platform was developed that can be connected to a camera sensor in addition to a digital accelerometer. The data from the digital accelerometer and images from the camera sensor are given a unified time stamp synchronized with the absolute time at the moment of data acquisition, thereby enabling synchronized measurement of vibration and images. A mechanism was implemented to add time stamps to the outputs of the digital accelerometer and camera sensor using the timekeeping accuracy of a chip-scale atomic clock (CSAC) mounted on the sensor device. As a prototype, the heterogeneous digital sensing platform achieved the desired performance. In this paper, an autonomous time-synchronized sensing system, which was newly designed and built to be applied to actual bridges, highways and buildings to stably acquire data from a digital accelerometer with accurate time information, image data from a camera sensor and data from any type of analog sensor, based on knowledge obtained in previous development, is reported.**

Keywords-Time Synchronization; Chip Scale Atomic Clock; Earthquake Observation; Structural Health Monitoring; Micro Electro Mechanical Systems; Camera Sensor

I. INTRODUCTION

As civil infrastructure, such as bridges and highways as well as high-rise buildings, deteriorate over time, automation of inspections for their maintenance and management is an important social issue. In addition, Japan is prone to earthquakes and other disasters, so there is a need to detect damage to structures immediately after a disaster and to assess the damage status. Data collection by sensing systems is necessary to automate these inspections and damage detection, but time synchronization across sensors must be ensured in order to analyze the data measured by multiple sensors and evaluate structural viability. Without time-synchronized data, time-series analysis using phase information cannot be performed. Time synchronization methods have been realized using dedicated wiring, wired or wireless networks, etc. However, when wiring is required, it places significant restrictions on the locations where sensors can be installed, and when wireless communication is used, it can be applied only where wireless communication is possible between sensors. In either case, it is impossible to deploy sensors over a wide area. On the other hand, if sensors installed at arbitrary locations can autonomously maintain accurate time information, this problem can be overcome. The method of using Global Positioning System (GPS) signals is effective outdoors, but cannot be used inside buildings, underground, under bridges or in tunnels. Therefore, a sensor device was developed that autonomously maintains accurate time information using a chip-scale atomic clock (CSAC) [2][3][7], which is an ultra-high precision clock [4][8][9]. In order to apply the sensor device to earthquake observation, logic was implemented to detect the occurrence of earthquakes and store data of earthquake events, and its functionality was confirmed in a shaking table experiment. The developed sensor device was also installed in actual buildings and bridges, and applied to earthquake observation and structural viability assessment [4]. However, the sensor device had a MEMS accelerometer, which made it difficult to accurately measure minute vibrations, and there was still a risk of noise contamination in the analog signal. The accelerometer mounted in the sensor device is therefore now a digital type, eliminating the risk of noise [5]. A camera sensor can also be connected to the sensor device, and a heterogeneous digital sensor platform was developed as a prototype [6]. In this paper, details of the autonomous time-synchronized sensing system, newly designed and built based on knowledge obtained from previous research and development, and a mechanism for adding ultra-high-precision time information to sensor data by a CSAC are described.

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In this paper, Section II shows the existing time synchronization methods and describes their problems and achievement of the development of digital sensing platform proposed in this research. Section III describes the configuration of autonomous time-synchronized sensing system and the development of the actual sensor device. Further, Sections IV and V describe the performance verification experiments on the time synchronization and the time stamp of developed camera sensor device, respectively. It is confirmed that time synchronization among the developed digital sensor devices with camera is achieved.

II. STATE OF THE ART

Many studies have been done on time synchronization in sensing, including the use of Global Navigation Satellite System (GNSS) signals via satellites, and the Network Time Protocol (NTP) [10] for time synchronization on the Internet. There are also studies that have achieved time synchronization by taking advantage of the characteristics of wireless sensor networks, such as low propagation delay. For example, protocols, such as Reference Broadcast Synchronization, Timing-sync Protocol for Sensor Networks, Flooding Time Synchronization Protocol, etc., have been studied [11]-[15]. However, although time synchronization methods that use wireless technology are convenient, there is no guarantee that wireless communication will always be available. Particularly, if wireless communication is disrupted during a disaster, such as an earthquake, it will be impossible to perform time-synchronized sensing, and data analysis cannot be carried out. Another technology that achieves highly accurate time synchronization indoors is the IEEE 1588 Precision Time Protocol (PTP), which employs Ethernet cables used in general Local Area Networks (LANs) as the transmission path, and time packets to achieve a synchronization accuracy within 1 microsecond. However, it is difficult to ensure stable synchronization accuracy due to fluctuations in packet delay and packet loss due to congestion within the LAN. In addition, because the delay is compensated by packet switching, the number of PTP devices that can be connected to the master device is limited, and it is not possible to deploy them in a Wide Area Network environment, where the delay changes dramatically.

When GPS signals are not available, wireless transmission and reception are unstable, and wired network connections are unavailable, it is nevertheless desirable for sensors to autonomously maintain accurate absolute time information in order to acquire data that ensure long-term, stable time synchronization. If each sensor can provide accurate absolute time information (a time stamp) to the data it measures, sensor data with autonomous time synchronization can be obtained. It was therefore decided to develop a sensor device that autonomously maintains accurate absolute time information by applying a CSAC [2][3][7], which is a clock with high timekeeping accuracy, The CSAC is a clock that can achieve ultra-high accuracy time measurement of the order of tens of picoseconds (5×10-11 seconds), while being sufficiently ultra-compact to be mounted on a board. Development began in 2001 with support from Defense Advanced Research Projects Agency (DARPA), and a consumer version was released in 2011. The CSAC is expected to be further miniaturized and lower-priced as it becomes more widely used for applications, such as countermeasures against interference with GPS due to jamming signals, high-precision positioning in environments without access to GPS signals, installation in smartphones and advanced disaster monitoring. CSACs have a smaller error by 4 to 8 digits than that of timekeeping using a crystal oscillator, NTP or GPS signals, which are commonly used in sensor devices. If this CSAC is installed in each sensor device and a mechanism implemented to add a high-precision time stamp to the sampling of measured data, time-synchronized sensor data can be collected even when GPS signals are unavailable, wireless transmission/reception is unstable, and wired network connections are not available. In previous development, the sensor device had an analog MEMS accelerometer, and the system configuration was such that any analog sensor could be connected via an external input interface. However, since the accuracy of an analog MEMS accelerometer was not high and the risk of noise contamination of the analog signal remained, it was decided to develop a fully digital sensing platform. Specifically, a digital accelerometer was installed in the sensor device to enable highly sensitive acceleration measurement without the risk of noise contamination, while a camera sensor could also be connected, and a technology was developed to accurately time-stamp both digital outputs using the CSAC. The data acquired by the sensor device described in this paper, which ensure time synchronization, can be used for the purpose of civil infrastructure inspection and structural viability assessment of buildings.

III. AUTONOMOUS TIME-SYNCHRONIZED SENSING SYSTEM AND CIRCUIT CONFIGURATION

If an ordinary sensor device is provided with a CSAC to correct the time information of the CPU and perform measurement, the CSAC's timekeeping accuracy is too high, which results in a delay. Therefore, to add the time information of the CSAC directly to the sensor's measurement data by hardware, a mechanism was implemented using a Field-Programmable Gate Array (FPGA), which is a dedicated integrated circuit. In this way, measurement data with absolute time information added by the FPGA are stored in a storage device and collected over a network, without putting an excessive load on the CPU of the sensor device. Moreover, since the FPGA is programmable, it can not only handle CSAC time information but can also incorporate logic for detecting the occurrence of earthquakes and fires using the measurement data. In this paper, a mechanism whereby accurate CSAC time stamps are added to the outputs of a digital-type accelerometer, a camera sensor and an external analog input, is described.

A. System Configuration

As shown in Figure 1, the sensor device developed in this research consists of an oscillator and FPGA that synchronize GPS time (GPST) with a CSAC, provide a stable reference signal, and maintain absolute time information; a sensor section with a digital accelerometer and an external analog sensor input interface; a signal processing board with a CPU;

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and a camera for capturing images. The oscillator and FPGA supply a high-precision 10 MHz reference clock and 1 Pulse Per Second (PPS) signal, and the FPGA generates time stamps and trigger signals for acquiring data. The sensor section comprises a digital accelerometer and an external analog sensor input interface. Any analog sensor can be connected to the external analog sensor input interface. The digital accelerometer outputs data in response to a trigger signal via a Universal Asynchronous Receiver/Transmitter (UART). Data from the sensor connected to the external analog sensor input interface are converted by A/D converters in response to trigger signals, and output as 16-bit serial values. The camera sensor can release the shutter in response to a trigger signal, and output RGB values. The acquired data are stored in a connected Solid-State Drive (SSD). Camera data and sensor data are stored on separate SSDs in consideration of access speed. This data can be viewed, retrieved or deleted via the network by taking out each SSD, or by using the system's file server function. Operations, such as measurement setup, time setting and operation mode change are performed via the network. As for the network, the system has an internal wired LAN and Wi-Fi, so users can choose either one.

B. Oscillator and FPGA

Figures 2 and 3 show the configuration and appearance of the oscillator and FPGA sections. The oscillator and FPGA sections have the function of synchronizing the CSAC with 1 PPS output from the GPS module or 1 PPS input from outside, and generate triggers to be input to the sensors and camera in the FPGA from the 10 MHz clock of the CSAC. The trigger signals thus generated are synchronized with the 1 PPS of the CSAC, which is synchronized with the GPS.

When performing time synchronization across multiple sensor devices, all sensor devices can be set as "master", or one sensor device can be set as "master" and the other sensor devices can be set as "slaves." When a sensor device is a "master," it receives the GPS signal, and inputs the 1 PPS from the GPS module to the CSAC to synchronize the GPS with the CSAC. If the sensor device is a "slave," the master and slave are synchronized by inputting the 1 PPS output from the "master." In addition, commands to set the CSAC synchronization period or reset the CSAC 1 PPS phase value, and a command to select either the GPS or an external input, are executed from the signal processing board on the CSAC and FPGA via a connector. The 10 MHz and 1 PPS output from this board is the clock source for this system. Due to a combination of the frequency stability of the GPS and CSAC, the synchronization period is set to 1000 seconds so that the time can be maintained for a long period even if the GPS is interrupted.

C. Sensor board

Figures 4 and 5 show the configuration and appearance of the sensor section. The sensor section comprises a digital accelerometer and an external analog sensor input interface. The data from the digital accelerometer can be sampled at 1 kHz at the time of the trigger. The external analog sensor input interface has three channels for connecting an analog accelerometer for comparison with the digital accelerometer. Depending on the purpose of measurement, any analog sensor can be connected in addition to the analog acceleration sensor.

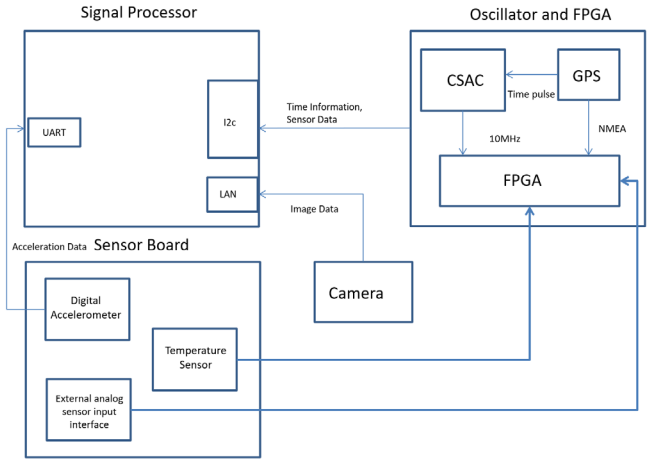

Figure 1. System configuration.

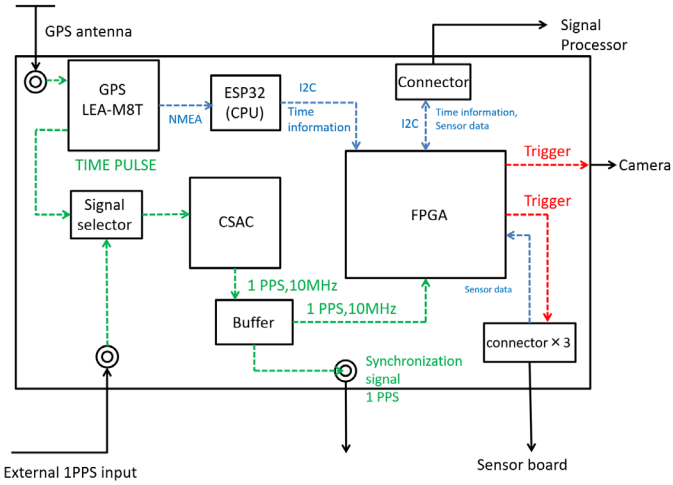

Figure 2. Oscillator and FPGA.

Figure 3. External appearance of oscillator and FPGA.

The signal input from the external analog sensor interface is converted by an A/D converter and output as a 16-bit serial value, but by splitting the signal into two channels and amplifying one of them 64 times, an A/D converter with 16-bit resolution can obtain a resolution equivalent to 22-bits. Data from the digital accelerometer are output to the FPGA via the UART, and data from the sensor connected to the external analog sensor input interface are output via a Serial Peripheral Interface (SPI).

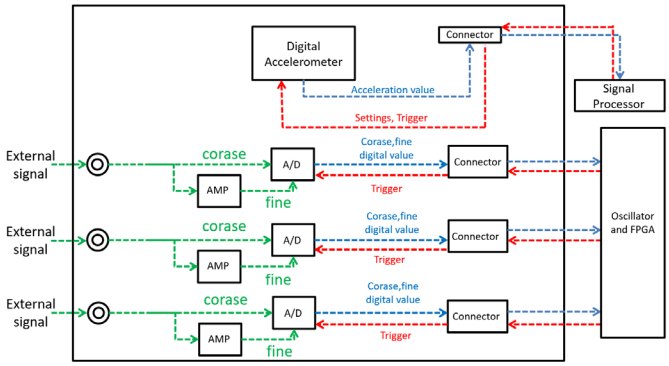

Figure 4. Sensor board.

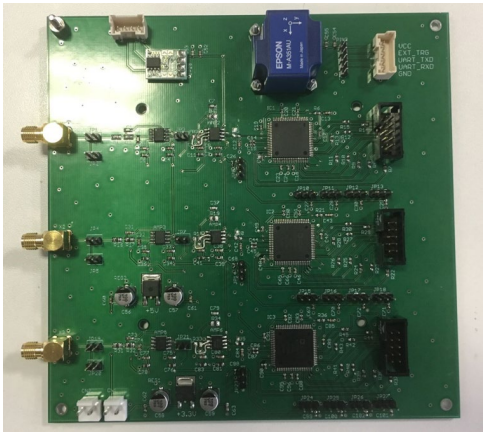

Figure 5. External appearance of Sensor board.

D. Signal processor

Figures 6 and 7 show the configuration and appearance of the signal processor. For the signal processor, the Raspberry Pi 4 shown in Table 1 is used. As shown in Table 1, Ubuntu is installed as the CPU OS, an SSD can be used via USB 3.0, camera communication is possible via Gigabit Ethernet, and an internal Wi-Fi antenna can be connected. Internal data can be retrieved and viewed via the LAN (Wi-Fi) using Samba functions, and Secure Shell (SSH) can be used to configure settings and start measurements. In addition to the above functions, the CPU mainly performs time setting, sorting of acquired data, format conversion, filing, and processing of image data from the camera.

E. Digital accelerometer

Figure 8 and Table 2 respectively show the appearance and specifications of the digital accelerometer mounted on the sensor board. The digital MEMS accelerometer mounted on the sensor board has a 3-axis crystal acceleration sensor with high accuracy and excellent stability, which is micro-fabricated from a highly accurate and stable crystal material. As shown in Table 2, it has low noise and low power consumption and is capable of high-resolution vibration measurement.

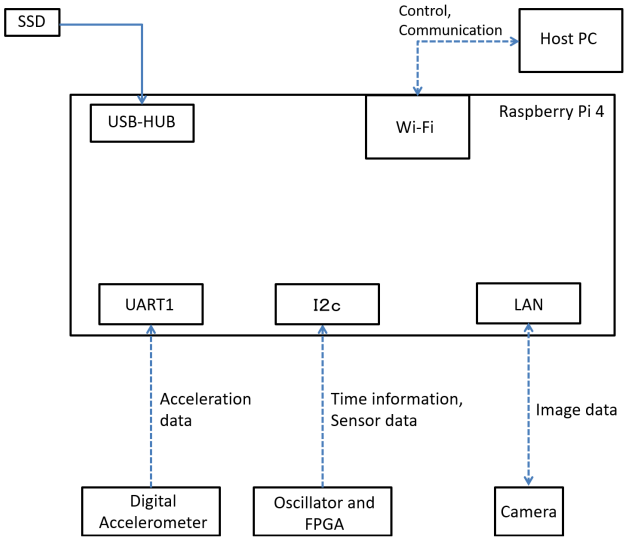

Figure 6. Signal processor.

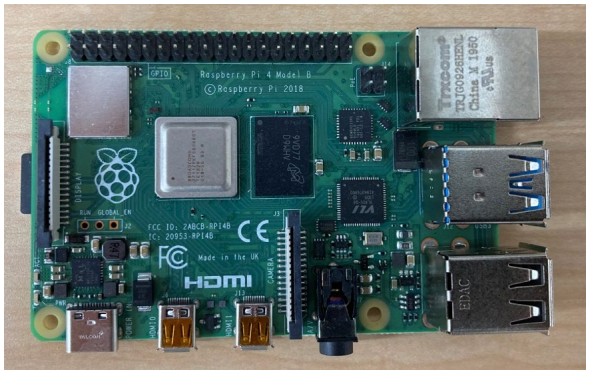

Figure 7. External appearance of Signal processor.

TABLE I. SPECIFICATIONS OF SIGNAL PROCESSOR

OS	Ubuntu 20.04.2 LTS
CPU	(GNU/Linux 4.5.0-00185-g3bb556b armv7l)
Memory	1.5GHz quad-core Cortex-A72 (ARM v8) 64-bit SoC
LAN	8GB
USB	RJ-45×1：IEEE802.3i（10BASE-T）、IEEE802.3u（100BASE-TX）、IEEE802.3ab（1000BASE-T）
UART	USB3.0 Standard A Connector×2
FPGAROM	UART×2
Storage	16GB(MicroSD,OS)

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Figure 8. Digital Accelerometer.

TABLE II. SPECIFICATIONS OF DIGITAL ACCELEROMETER

Model	EPSON M-A352VD10
Range	±15 G
Noise Density	0.2 μG/√Hz (Average)
Resolution	0.06 μG/LSB
Bandwidth	460 Hz
Output Range	1000 sps (selectable)
Digital Serial Interface	SPI
Outside Dimensions (mm)	48 × 24 × 16
Weight	25 grams
Operating Temperature	-30 ℃ to +85 ℃
Power Consumption	3.3 V, 13.2 mA(Typ.)

F. Camera sensor

Figure 9 and Table 3 respectively show the appearance and specifications of the camera sensor. Baumer VCXG-02C, a high-speed Gigabit Ethernet camera module, was used as the camera sensor.

It is compact, has low power consumption, has excellent performance in low-light environments, and can acquire images at the time of a trigger by inputting an external trigger. Furthermore, it features reliable and stable data transfer with an internal buffer for retransmission, and is equipped with an overlap trigger mode that allows trigger shooting at a frame rate equivalent to free-run shooting.

Figure 9. Camera sensor.

TABLE III. SPECIFICATIONS OF CAMERA SENSOR

Model	Baumer VCXG-02C
Active Array Size	640 x 480
Sensor	CMOS ON Semiconductor：PYTHON 300
Pixel Size	4.8 μm x 4.8 μm
Shutter	Global Shutter
Power Supply	12-24 VDC/2.6W
Image Formats	BayerRG / RGB / BGR / Mono
Frame Rate(fps)	401(640 x 480)
Exposure Control	20μsec ～ 1sec
Operation Mode	Trigger/Free Run
Size(mm)	29 × 29 × 49
Weight(g)	120
Interface	GigabitEthernet（1000BASE）/ FastEthernet（100BASE）

Rolling shutter is a capture method that scans the entire frame vertically or horizontally. From the point of view of time-synchronized sensing, the biggest drawback of the rolling shutter is that it does not capture the same moment. Scanning itself is performed at high speed, but there is a time difference in the photographed object due to the sequential scanning. To overcome this shortcoming, a global shutter camera was adopted, which shoots a frame at a time. This allows for accurate timestamping of each captured image.

IV. TIME SYNCHRONIZATION PERFORMANCE EXPERIMENT OF THE CAMERA SENSOR

An experiment was conducted to verify the camera sensor's time synchronization performance. Figure 10 shows the experimental system configuration. A trigger signal generated by the oscillator and FPGA section is simultaneously sent to the camera sensor and LED control FPGA. Since the shutter of the camera sensor is synchronized with the lighting state of the LEDs, if images are acquired in accordance with the transition in the lighting state, it is considered that trigger-synchronized images are being acquired. The source of this signal is the CSAC, which is synchronized with the trigger signal passed to the sensor section, so the sensor and the camera sensor are synchronized.

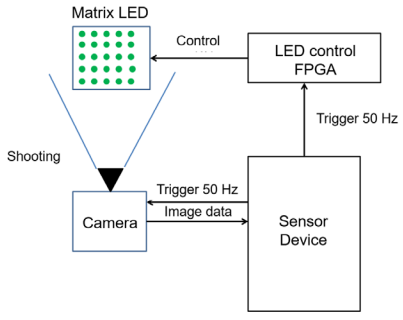

Figure 10. Camera data measurement system.

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The FPGA for LED control is configured to control the lighting of the LEDs at the time of the trigger signal clock (50 Hz). With a 5 x 5 LED matrix, the LEDs light from upper left to lower right, one by one, in accordance with the rising edge of the trigger signal. The camera sensor is fixed to photograph the LED matrix. Figure 11 shows the pictures taken by the camera sensor. Time elapses in 20 ms increments from upper left to lower right. Since the LEDs in the photos light one by one, images are acquired according to the signals input to the FPGA for LED control. In this figure, the period of 1 horizontal line of LEDs is 100 ms as the number of LEDs in each line is five. Each vertical line in the images is every 100 ms, and since all the LEDs are lit in the same way, none are left out. From these results, it was confirmed that images can be continuously acquired in synchronization with the trigger from the sensor device.

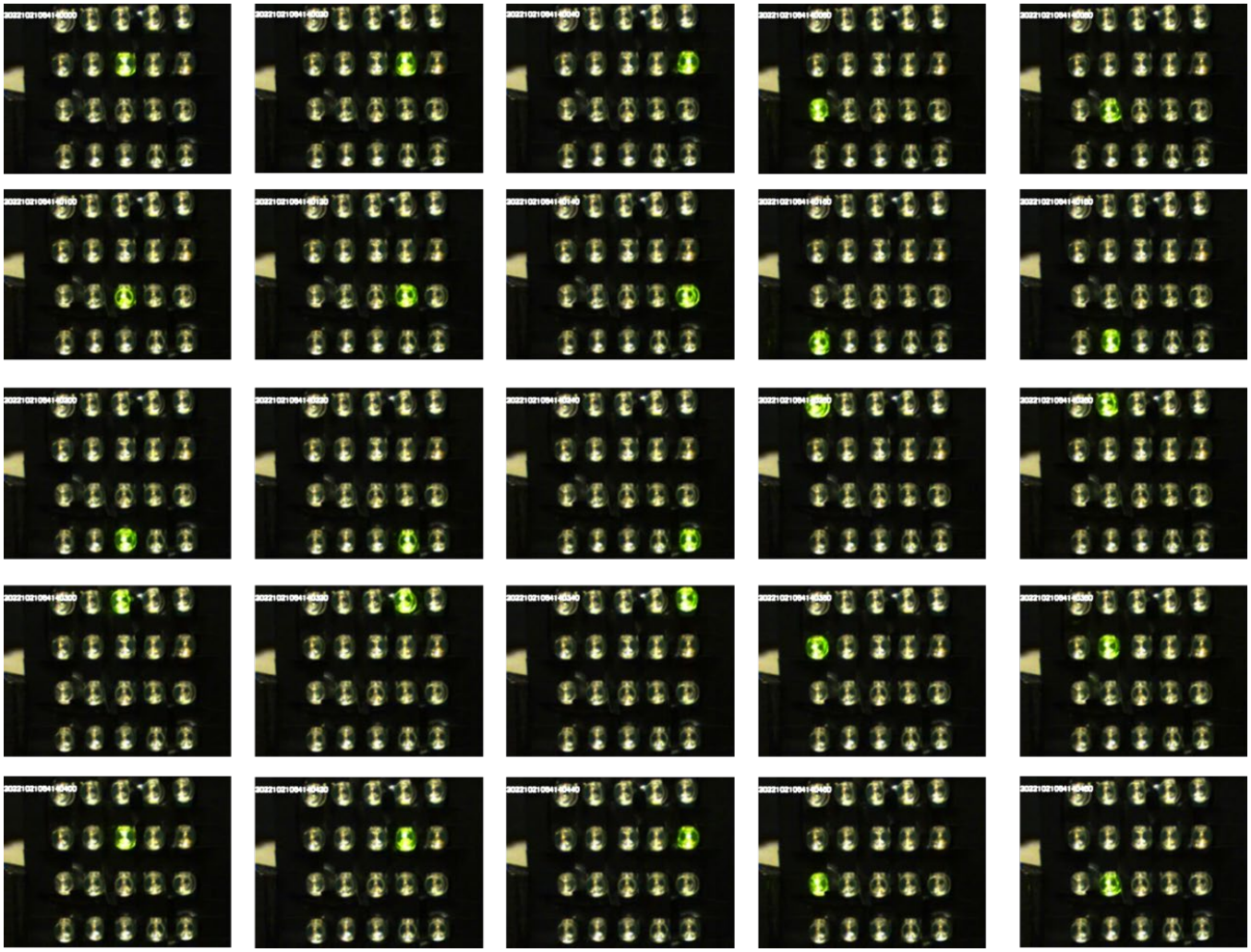

Figure 11. Continuous images from the experimental result.

The performance verification experiment on the time synchronization of developed camera sensor device was carried out as shown above. It is confirmed that time synchronization among the developed digital sensor devices with camera is achieved. The development of this digital sensing platform has enabled time-synchronized measurements between digital accelerometers, camera sensors, and many types of external input analog sensors, as well as multimodal analysis between measurement data.

V. TIME STAMP VERIFICATION EXPERIMENT

The time stamps added to the images acquired by the camera sensor were experimentally verified. Figures 12 and 13 show the experimental system configuration and GPS module, respectively. The camera sensor was used to capture images of the LEDs on the GPS module to see whether the increase in the number of seconds coincided with the seconds of the time stamp. When the power is turned on, the LED of TP1 turns off at a timing of 1 PPS of the GPS. The time to turn off the LED can be determined with a pulse width of 1 PPS,

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which in this case is 100 ms. In other words, the LED is OFF for 100 ms and ON for 900 ms every second. Figure 14 shows the results obtained every 20 ms. Since the time when the LED is OFF is set to 100 ms, the five images from 000 ms to 080 ms capture the state of the LED when it is OFF, and it can be seen that after 100 ms, the LED is ON, indicating that the seconds of the time stamp coincide with the OFF state of the LED. Figure 15 shows photos after 980 ms. After 980 ms, the LED is lit, but after the next 000 ms, it turns off, and after 100 ms, it is lit again.

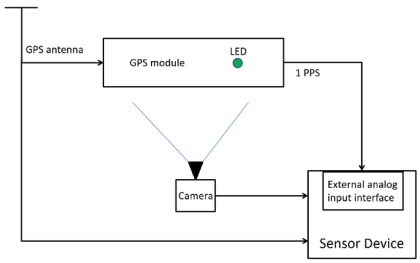
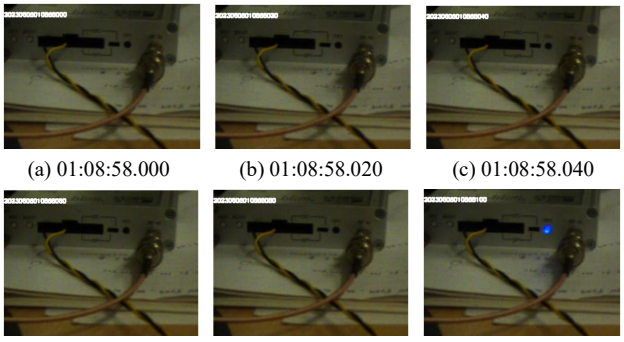


Figure 12. Experimental system configuration for time stamps.

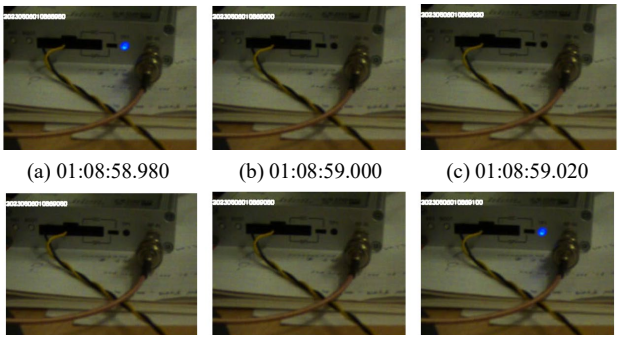
Figure 13. GPS module overview.



(a) 01:08:58.000 (b) 01:08:58.020 (c) 01:08:58.040

(d) 01:08:58.060 (e) 01:08:58.080 (f) 01:08:58.100

Figure 14. Sequential photos of experimental results.



(a) 01:08:58.980 (b) 01:08:59.000 (c) 01:08:59.020

(d) 01:08:59.060 (e) 01:08:59.080 (f) 01:08:59.100

Figure 15. Sequential photos of experimental results (after 980 ms).

From the above results, it was confirmed that 1 PPS of the GPS coincides with the seconds of the time stamp. Since the camera takes photos every 20 ms, it was thus possible to verify that actual phenomena coincided with the images, at least to within 20 ms.

VI. CONCLUSION

In this paper, the development of an autonomous sensing system that maintains highly precise absolute time information by applying a CSAC was reported. First, an autonomous time-synchronized sensing system and its circuit configuration were described, and a mechanism for adding ultra-high-precision absolute time information to sensor data by the CSAC, and the development of a sensor device, were described in detail. A function to add the same time stamp to the output from a camera sensor, the output from an internal digital accelerometer and the input from an external analog input interface, was implemented. The results of experiments to verify the time synchronization performance of the camera sensor were also reported. It is planned to verify the time synchronization performance of this new sensing system with regard to measurement data obtained by the camera sensor, the internal digital accelerometer and the external analog input sensor.

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