New Architecture for Efficient Data Sampling in Wireless Sensor Network Devices

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***Abstract*—When discussing powering wireless sensor network nodes, there are a few major energy consumers: communications, microcontroller and the sensor. We propose a wireless sensor network platform architecture minimizing the energy consumption of sensing. The architecture proposed herein is based on a reactive approach to sensing. A number of possible hardware approaches are evaluated and compared. This comparison indicates that analog storage between the sensing element and the sensor electronics can be a feasible method for reducing the energy consumption of the system.**

Keywords-low power WSN sensing; WSN node architecture; wireless sensor network node.

I. INTRODUCTION

One of the most common questions regarding wireless sensor networks, WSN, is what the power consumption at the sensor node must be. Much work has been done on low-powered sensor nodes and their communication abilities: see, for example, [1]–[7]. Some specific examples are schemes handling the reduction of communication [8], effective routing and multihop schemes, and the reactive partial waking up of WSN nodes [9].

Most often, the sensing element itself is disregarded from an energy budget point of view. The current state of the art for sensor interfacing is to convert the sensor data to digital form. The most common approach is using an A/D converter. Other well known approaches involves letting the sensor data influence a digital pulse train of which we easily can measure parameters like frequency, pulse width or duty cycle. None of these approaches puts the power consumption of the sensor into focus. All of these approaches are based on the assumption that all data should be transfered to some computational stage on the WSN node or any device higher up in the system architecture.

In this paper, we propose an architecture for low power interfacing of a sensing element to a WSN node. The architecture exploits the idea of detecting no or discardable changes in data. Such detection should then inhibit further processing of sensor data as early as possible. The proposed architecture is based on a reactive wake-up chain starting at the sensing element itself.

The basis for this WSN node architecture is the determination of changes in sensing element data as early as possible. In many real systems, data changes are small and are most often not of interest to the surrounding system. From an energy consumption point of view, we like to keep as much of the WSN node asleep as possible when determining whether a data sample constitutes a significant change compared with the previous sample.

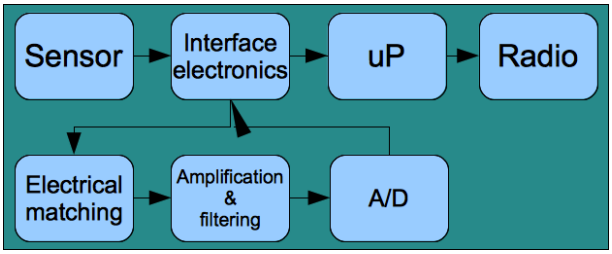

Figure 1. Traditional WSN node architecture, A1

Consider a WSN node architecture as in Figure 1. The most frequently used approach is to read the data into the μP store and compare it with the previous data. Energy is spent on sensing element sampling, signal amplification and filtering, A/D conversion and data comparison in the μP. This is the architecture you will find in most WSN and IoT (Internet of Things) nodes currently available see e.g. [10], [11].

This paper will, from an energy consumption point of view compare this generic WSN sensor interface architecture to architectures enabling early detection of discardable data changes.

A. WSN node architecture

Three different architectures targeting the early detection of useful data will be described and discussed from an energy usage perspective. As a base line, the generic architecture in Figure 1 will be used.

The first opportunity for comparison is by adding a digital memory and comparison function after the A/D conversion, as shown in Figure 2. Energy is spent on sensor sampling, signal amplification and filtering, A/D conversion and storage and comparison of the data in digital memory. Enabling the μP to sleep while performing sensor data sampling if there are no changes or small changes in sensor data will

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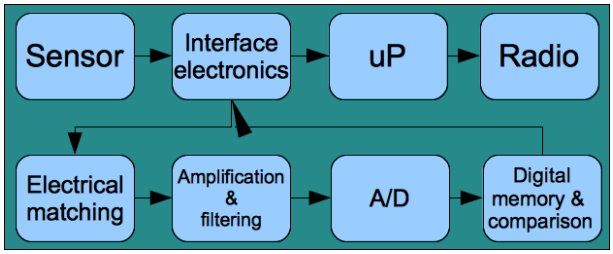

Figure 2. WSN node architecture, A2, with external digital sensor memory and comparison logic.

use energy only for the HW cost of digital memory, some configurable logic (to allow for the setting of change limits) and sending a wake-up signal to the μP.

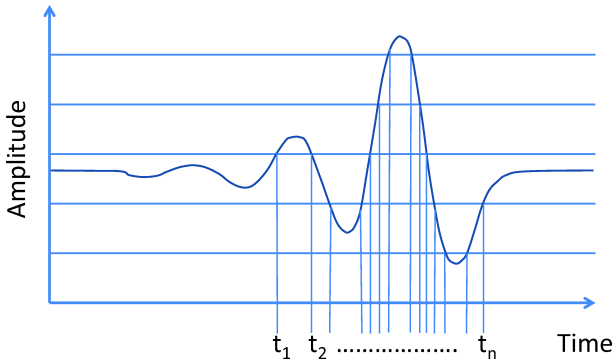

Figure 3. Illustration of level trigger sampling of a periodic signal.

Yet, one possibility is to replace the conventional A/D converter in the structures above with an Asyncronous, or Level-Crossing, ADC. As introduced in [12], [13], the level crossing ADC samples the signal when it passes a pre-determined threshold level, instead of at discrete time intervals as performed in traditional ADCs. Thus, the main output of the level-crossing ADC is the time elapsed as the signal has moved between two pre-determined levels, Figure 3. This architecture offers a couple of advantages over traditional techniques. Firstly, it allow the use of fewer quantization levels, as long as the time measurement can be performed with sufficient accuracy. Secondly, and in the context of this paper more important, the activity of the device is controlled by the behaviour of the signal that is to be sampled, allowing event-deriven data acquisition [14]. In the sensing scenario, the device will inherently idle as long as the signal stays between two threshold levels. Accordingly, no data is fed through to higher levels in the system, allowing for these to be help idle. These possibilities in the design of sensor front ends have been explored for Ultrasound measurement systems [15], as well as for other energy constrained sensor applications [16].

In terms of energy cost, the A/D conversion is dominant in the scenarios dicussed above. Thus, it is of interest to explore

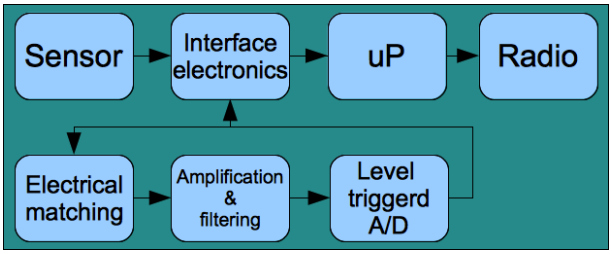

Figure 4. WSN node architecture, A3, with level triggered A/D conversion.

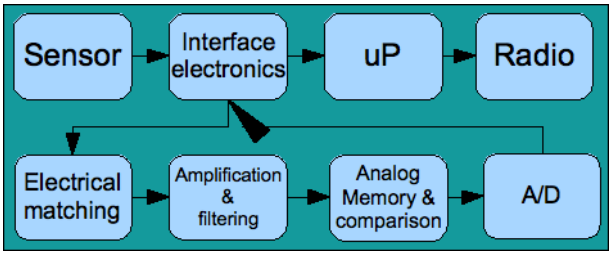

Figure 5. WSN node architecture, A4, with external analog memory and comparison logic before the A/D conversion.

the possibilities to completely remove the A/D converter. One scenario to achieve this is shown in Figure 4. Here, we introduce an analog memory with the capability of storing and comparing at least two values with associated logic and signalling to the μP. In this setup, energy is spent on sensor sampling, signal amplification, and filtering, and analog storage with its associated logic. Thus, the uP can sleep during sensning element data sampling if there are no, or small, changes in the sensed data.

Two ways to implement the analog memory are the use of Charge couple devices (CCD) and switched capacitor storage.CCDs operate by transferring stored charge packets along the surface of a semiconductor by manipulating the potentials of gate electrodes placed close to the semiconductor surface [17]. This forms essentially an analog shift register. While these devices has most commonly been used as image sensors, a number of works have over the years applied them as analog delay elements in signal processing applications.One critical advantage of using CCDs in analog delay circuits is the fact that as long as they are operated at a constant clock frequency, they are completely insensitive to matching between storage cells. In addition, the unique possibility of non-destructive readout at intermediate locations along the device have given rise to CCD based analog finite impulse response filters [18]. However, in order to move the charge packets along the surface of the semiconductor the potentials at the gates needs to change as a function of time. The charge required to affect the required change in potential is comparable to the total charge currently being transported through the device. Thus, for a CCD the power dissipation depends not only on the charge packet size required to attain

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the required SNR, but also directly on the number of storage elements.

In contrast to CCDs, the only charge required when storing an analog sample using a switch capacitor analog memory is the charge required for the signal it self and some small charge for driving the sampling switch. The charge will stay on its capacitor without further intervention until it becomes corrupted due to leakage. It can retrieved independently on any other stored charges on other capacitors in a random-access manner if desired. Switched capacitor analog memories are however subject to the mismatch between capacitors. Both CCDs and switched capacitor analog memories present interesting alternatives to direct digitalization in systems a signal needs to be delayed before digitalization, or where it is deemed simpler do sample the signal at a high rate and later digitize the stored signal at a slower rate [19].

II. Energy analysis of architecture

The time scale on which the property being measured can be expected to change is of major importance in the choice of data acquisition architecture.

In systems designed for rapidly changing signals the time-dependent corruption of reference values stored in analog circuits (e.g., due to leakage currents) is of minor consequence and the power required for the comparators represents a significant improvement compared to continuously digitizing the signal at the rate required to capture all relevant information present in the input signal.

At time scales where storage of analog values is unfeasible, some improvements may still be attainable by using a level crossing ADC (Analog to Digital Converter) where digital registers and a DAC (Digital to Analog Converter) is used for generating the analog reference value(s).

If the signal changes sufficiently slowly the minimal static power consumption required of even the best continuous-time circuits exceed the average consuption of a regular sampling data acquisition system. Here, dedicated logic controlling the sampling process, comparing to digital thresholds and waking the microcontroller only when significant changes have occurred can yield some improvements, if the added complexity can be justified. A sampling architecture is of course also favorable in any measurement system where the sensor it self accounts for a significant fraction of the power dissipation yet can be powered down efficiently between measurements.

Below, we comment on the procedure for calculation of power consumption for the components used in the different architectures.

- Analog memory
  From the voltage noise on a capacitor at equilibrium,

$$v_n = \sqrt{k_B T / C} \tag{1}$$

  the minimal capacitor, and thus average energy per sample required for some specified SNR can be calculated. For example to reach an SNR of 60 dB with a signal amplitude of 0.5 V, a capacitance of about 30 fF is required. If unipolar charge is stored, the average energy to store samples from a sinusoidal input signal would be about 22 fJ. This compares favorably to the best ADCs in the literature (e.g., 1V 11fJ per conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18 μm CMOS consumes 11pJ per 10-bit sample). A switched capacitor memory consumes this energy once per stored value. On the other hand, in a CCD all data is shifted one step at each data acquisition. Thus, the CCD will consume an energy n times the value above per sample, where n is the number of storage positions in the CCD.
  This method gives an estimate of the theoretical minimum power required to store analog values, and is used as a lower bound.
- Time sampling ADC
  Publication of performance for this type of converter is still relatively sparse. For this paper, we use data from [15], [16].
- ADC
  ADC performance data have been collected based on [20]. The data presented in the tables below is calculated based on the therein presented Figure of merit of 100 fJ/conversion step, relevant for work published in 2011.
- Amplifier
  Amplifier data are taken from commercially available devices.
- Microcontroller
  Micro contoler data is taken from commercially available devices
- Digital logic
  Data i taken from estimates of number gates and data on commercially available gate consumption.

To analyze the energy consumption of the presented architectures, we will use four different sensing situations:

- Temperature sensing using a PT100 element as the sensing element
  - bandwidth 1 Hz
  - resolution 10 bits
- Accelerometer measurement
  - bandwidth 1 kHz
  - resolution 10 bits
- Microphone - sound recording
  - bandwidth 20 kHz
  - resolution 14 bits
- Ultrasound pulse echo measurement in liquid - piezo ceramic transducers
  - bandwidth 1 MHz - 10 MHz

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– resolution 10 bits

This analysis is conducted using published state-of-the-art data (from our group and others) and data from commercial devices. This way, we can build an accurate picture of the total energy consumption of the proposed architectures. No circuit simulations are made here, nor have we built any complete devices.

The energy analysis is based on the following model. The total electrical power P_{tot} consumed by a WSN node can be described as:

$$P_{tot} = P_{sens} + P_{cond} + P_{A-mem} + P_{AD} + P_{D-mem} + P_{\mu P} \quad (2)$$

The total energy usage is then obtained by introducing the time needed for each operation (after which it can be turned off). To make the analysis reasonably simple, we assume that the architecture supports turning off E_{sens}, E_{cond}, once data has been stored either in analog or digital form.

For data sampling from one sensor, we assume a sensing and conditioning time t_{sens_cond}, an analog storing time t_{A-mem}, an A/D time t_{AD}, a digital memory time t_{D-mem} and a μP time $t_{\mu P}$. Thus, we obtain the total power E_{tot} used for data sampling from one sensor as:

$$E_{tot} = P_{sens} * t_{sens} + P_{cond} * t_{cond} + P_{A-mem} * t_{A-mem} + P_{AD} * t_{AD} + P_{D-mem} * t_{D-mem} + P_{\mu P} * t_{\mu P} \quad (3)$$

Provided that we have some understanding of the real values of these energies and times, we can calculate the total power consumption. In the following equation, we will do this for two sensor types, a PT-100 sensor and an ultrasonic pulse echo sensor, for each of the three architecture types A1, (see Figure 1), A2 (see Figure 2), A3 (see Figure 4), and A4 (see Figure 5).

A. Energy analysis PT-100 sensor

In this case, we assume the power consumption and time needed for a PT-100 sensor and its associated electronics, according to table I. For each of the three different architectures in Figures 1-4, we then calculate the expected span of energy consumption energy consumption based on data in Table I. The results if given in Table V. Based on the long time scales, analog memories and level triggered A/D have not been considered for this application.

B. Energy analysis accelerometer measurement

Here, we discuss the power consumption associated with the measurement of acceleration using a MEMS based 3D accelerometer. A potential usage scenario is given in Figure 6, where vibrations from passing by automotive are detected and processed. In Table II, the power consumption and related timing for the sensor and associated electronics are given. For each of the four architectures A1-A4 of Figure 1-5, we then calculate the expected span of (maximum and minimum) energy consumption based on data in Table II. The results are given in Table V.

Table I
ENERGY CONSUMPTION AND TIMING FOR A PT100 WSN SENSOR NODE.

Device	Energy consumption	Time awake [μs]
PT100	0.1-1 mW [21], [22]	10
Conditioning electronics	0.6 μW [23]	10
Analog memory	n/a	n/a
A/D (10 bit)	0.2 nW	cont
level trigged A/D	n/a	n/a
Digital memory	0.01-0.1 mW	1(storage time)
μP	1-10 mW [24]	30

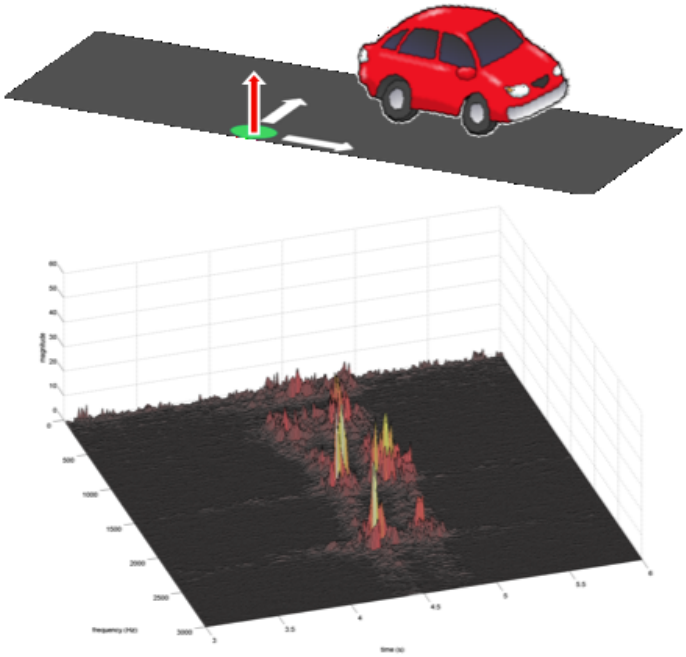

Figure 6. The application of accelerometer equipped WSN nodes for road application [25]

Table II
ENERGY CONSUMPTION AND TIMING FOR AN 3D ACCELEROMETER EQUIPPED WSN SENSOR NODE.

Device	Energy consumption	Time awake [μs]
Acelerometer	0.01 mW [26]	1 (1 μs long pulse excitation
Amplifier and filtering	1 μW [27]	10-20 (signal duration + startup time)
Analog memory	n/a	n/a
A/D (10 bit)	0.2 μW	cont
level trigged A/D	25 μW	cont
Digital memory	0.01-0.1 mW	10 (storage time)
μP	1-10 mW	30 (300 clock cycles at 10MHz)

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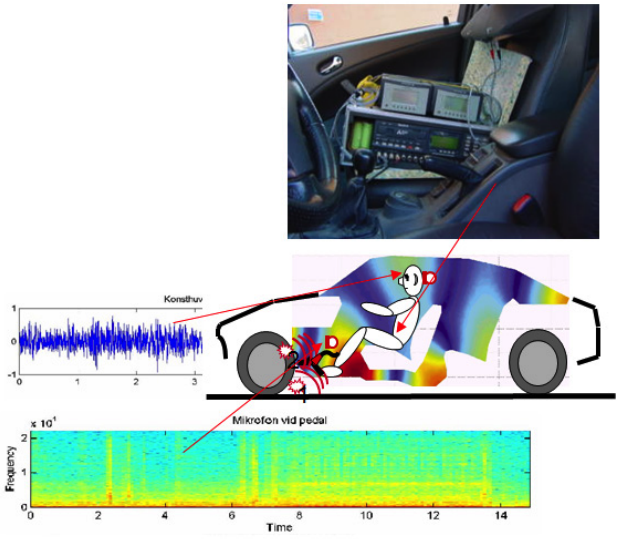

Figure 7. The application of microphone equipped WSN nodes for noise detection in automative test application

C. Energy analysis. Microphone - sound recording

Here, we discuss the power consumption and timing needed for the recording of short sounds. The WSN node is equipped with an capacitor based microphone. A potential usage scenario is given in Figure 7 In Table III, the power consumption and related timing for the sensor and associated electronics is given. For each of the four different architectures A1-A4 of Figures 1-5, we then calculate the expected span of (maximum and minimum) energy consumption based on data in Table III. The results if given in Table V.

Table III
ENERGY CONSUMPTION AND TIMING FOR AN MICROPHONE EQUIPPED WSN SENSOR NODE.

Device	Energy consumption	Time awake [μs]
Microphone	0.01 mW	1
Amplifier and filtering	0.04 mW [28]	cont
Analog memory	1 nW	cont
A/D	4 μW	cont
level trigged A/D	n/a	n/a
Digital memory	0.01-0.1 mW	10 (storage time)
μP	1-10 mW	30 (300 clock cycles at 10MHz)

D. Energy analysis ultrasound sensor 1-10 MHz

Here, we discuss the power consumption and time needed for a piezo electric transducer in an ultrasound pulse echo system used in liquid or solid media. A typical pulse echo measuring situation with typical sound signals is shown in Figure 8. In Table IV, the power consumption and related timing for the sensor and associated electronics areis given.

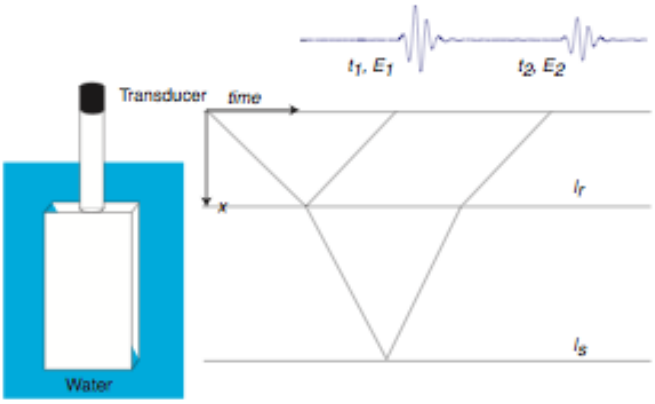

Figure 8. Ultrasound pulse echo measurement with associated acoustic signals

For each of the four architectures A1-A4 of Figure 1-5, we then calculate the expected span of (maximum and minimum) energy consumption based on data in Table IV. The results if given in Table V.

Table IV
ENERGY CONSUMPTION AND TIMING FOR AN ULTRASOUND WSN SENSOR NODE.

Device	Energy consumption	Time awake [μs]
Piezo excitation	0.01 mW [26]	1 (1 μs long pulse excitation
Amplifier and filtering	5 mW [29]	cont
Analog memory	0.5 μW	cont
A/D (10 bit)	2 mW	cont
level trigged A/D	175 mW	cont
Digital memory	0.01-0.1 mW	10 (storage time)
μP	1-10 mW	30 (300 clock cycles at 10MHz)

III. RESULTS AND DISCUSSION

Under the assumptions that we made, we have compiled power consumption data for four sensing scenarios. Data is given in table are shown in Table I til IV. The scenario operating energy consumption is computed for a 1 second period according to Equation 2 and shown in Table V.

Table V
LOW AND HIGH END ENERGY CONSUMPTION DATA IN JOULE FOR THE FOUR USAGE SCENARIOS AND THE 4 WSN NODE ARCHITECTURES.

	A1	A2	A3	A4
T_{low}	10^{-3}	$3*10^{-8}$		
T_{high}	10^{-2}	$3*10^{-7}$		
Acc_{low}	10^{-3}	$2*10^{-7}$	$3*10^{-5}$	
Acc_{high}	10^{-2}	$5*10^{-7}$	$3*10^{-5}$	
$Micro_{low}$	10^{-3}	$4*10^{-5}$		
$Micro_{high}$	10^{-2}	$4*10^{-5}$		
US_{low}	$8*10^{-3}$	$7*10^{-3}$	$2*10^{-1}$	$5*10^{-3}$
US_{high}	$2*10^{-2}$	$7*10^{-3}$	$2*10^{-1}$	$5*10^{-3}$

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It is obvious that the μP uses a large amount of energy. Thus, any architecture that can avoid waking up the μP has clear advantages from an energy consumption point of view. This puts reactive architectures enabling the sleep fo the μP at favor.

For the discussed reactive architectures the results indicates a dividing line between sensor signals having lower frequency (~20kHz) and sensors of having higher frequency content. Another indicated dividing line is how many bits of resolution that is needed. More bits eats more power for particularly traditional A/D converters.

The following general conclusions can be made:

- For low frequency sensor signal
  - uP energy cost dominates
  - A/D + digital memory comparison is favorable
- For higher frequency sensors
  - Data conversion energy cost dominates
  - Analog memory storage and comparison has the most potential
- Reactive architecture gives in all cases an improved energy budget

Thus, it is clear that in a sensing situation with a dynamic sensor signal, such as ultrasound, avoiding A/D conversion is a promising approach. If analog memory and comparison techniques can be developed similar to what we have seen for A/D converters, analog storage architecture will be a strong contender for future WSN designs.

IV. Conclusion and further work

The reactive architecture proposed here for minimal energy consumption of sensing on WSN platforms is promising. Based on an analysis of current state-of-the-art sensor interface electronics, an approach using analog storage provides interesting data when compared with more mature technology such as ADC and ADC combined with memory logic.

Future work will reveal whether if a reactive architecture based on an analog storage approach will show improvements in energy consumption similar to those of advanced ADC. If such improvements are shown, the analog storage approach has clear merit for use in future WSN node designs.

Acknowledgment

The authors would like to thank the ESIS project [30] supported by EU structural funds the Artemis Arrowhead project [31] for financial support.

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