High Repetition Rate Integrated Streak Camera in Standard CMOS Technology

Jean-Pierre Le Normand, Chantal-Virginie Zint, and Wilfried Uhring

InESS. Université de Strasbourg and CNRS
Strasbourg, France
e-mail: Jean-Pierre.Lenormand@unistra.fr; Virginie.Zint@unistra.fr; Wilfried.Uhring@unistra.fr.

Abstract— **The capabilities of an Integrated Streak Camera (ISC) prototype fabricated in an AMS 0.35 µm CMOS process to observe light pulses of few nanosecond FWHM (Full width at half maximum) with or without analog accumulation is presented. The sensor consists of a matrix of 64 * 64 pixels including an electronic shutter and an analog accumulation capability. The sensor can operate in single shot mode when the light pulse power is sufficient and in repetitive mode, i.e., it can measure a recurrent light pulse and accumulates the successive photo charges into an internal node, for low light detection. The repetitive mode improves the sensitivity and the signal to noise ratio of the system. The functionality of a streak camera is reproduced through a versatile integrated temporal sweep unit that generates a sampling period continuously adjustable from 125 ps to DC. The distributed architecture and the in-pixel embedded memory allows the sampling rate to exceed 400 GS/s. Results on the dynamic performance of the ISC are presented. The measurements showed a temporal resolution close to the nanosecond and a repetition rate of more than 50 MHz. A 6 ns FWHM light pulse spatially focused on a single pixel row has been successfully measured in single shot and in accumulation mode.**

Keywords - CMOS integrated circuits, image sensors, integrated optoelectronics, time domain measurements

I. INTRODUCTION

High speed imaging is used in many scientific fields to measure phenomena which are not observable with naked eyes [1]-[4]. Ultra fast video cameras take a succession of images to observe transient events of about a microsecond [5]. The observation of faster transients is possible using a streak camera [6][7] which produces the one-dimensional spatial (*x*) intensity (*I*) (a streak) of a light pulse event as a function of the time (*t*). The output of the camera is a two dimensional image *I=f(x,t)*. The streak camera offers the best temporal resolution in the field of direct detection in optics which can reach less than one picosecond [8]. However the use of vacuum tubes for this camera makes the system delicate, cumbersome and expensive. It also requires a high supply voltage (> 1 kV) and makes use of critical radio frequency electronics. The aim of our work is to develop an Integrated Streak Camera (ISC) in a standard CMOS technology that can reach a temporal resolution of the order of a few hundreds of picoseconds that actually corresponds to the use of streak camera for a lot of applications. Examples are photoluminescence from nanocrystals [9][10], velocimetry, interferometry to study

shock waves of various materials [11]-[13], or in-life sciences for fluorescence lifetime imaging [14][15] and Förster resonance energy transfer [16]. In 2003, the first prototype of ISC, based on a pixel array, demonstrated the feasibility of an ISC with a sampling period in the order of one nanosecond and a temporal resolution of about 6 ns [17]. Nevertheless, this sensor operates only in single shot mode and presents a low signal to noise ratio. Indeed, it requires a derivative reconstruction process that increases the high frequency noise and implies a low output dynamic range.

The pixel architecture developed for the second generation of the CMOS spatiotemporal camera includes an electronic shutter and an analog accumulation feature within the pixel in order to increase the system sensitivity. In [18], the static characterization of the accumulation mode has been reported. In this paper, an improvement of the complete architecture and the dynamic performances of the accumulation mode are presented. The new design increases considerably the signal to noise ratio for both the single shot and the repetitive mode. Moreover, the evaluated maximal repetition rate is above 50 MHz which is comparable to the fast repetition rate achievable with a conventional streak camera in synchroscan mode [19]. In the next section, we present the overall architecture and operation of the ISC and its pixel. After that, the dynamic characteristics and some experimental results of optical pulse measurements with and without accumulation are shown.

II. ARCHITECTURE OF THE INTEGRATED STREAK CAMERA

A. Overall architecture and operation principle

The functionality of the MISC (for Matrix based ISC) sensor is depicted in Fig. 1. For this matrix sensor architecture, in which the spatial axis is directed along the columns and the temporal axis is associated to the rows, the light signal can be correctly discriminated only if the spatial light intensity on a row is well known or, ideally, uniform. The advantage of creating a 2D array is to have several spatial channels in one chip, i.e., a conventional streak camera-like image *I=f(x,t)*. One can take advantage of the proposed illumination setup in [20] including a mechanical slit followed by a cylindrical lens in order to carry out the uniform light spreading operation while maintaining the
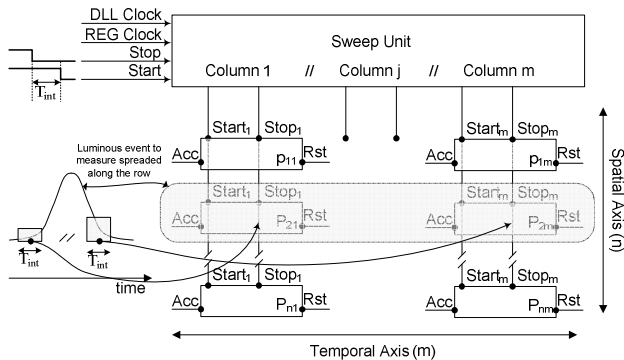
Figure 1. Architecture of the sensor and operation principle.

spatial resolution along the slit.

Let us consider a laser pulse train for the clarity of the explanation. We assume that this luminous event is punctual and focused on the slit, i.e., it is lighting uniformly a single row i of the MISC. For each pulse, the optical signal is integrated by the photodetector within the pixels p_{ij} with $j \in [1,m]$. The light is integrated during T_{int} for each pixel, but the beginning of the integration $Start_j$ for each column j is shifted by ΔT through the sweep unit. This operation is equivalent to the deflection of the electronic beam in an ordinary streak camera. Next, the corresponding photo-charges are stored and added to the previous ones inside the pixel by activating the Acc signal. Note that the operational sample rate of such a device is about 400 GS/s with a sample period ΔT of 150 ps and 64 lines. This very high data rate close to 10 Tb/s, cannot be continuously extracted from the sensor. In order to bypass the bottleneck of the I/O bus of the circuit, this architecture uses an embedded analog memory in each pixel to perform this operation. At the end of the acquisition, the data are extracted at a moderate rate of 20 Mpixel/s with a classical readout unit, not represented on Fig. 1.

The resulting signal of pixel p_{ij} is equivalent to a convolution between the illumination and a rectangle function with duration T_{int} and is given by:

$$ p_{ij} = \sum_{k=1}^{N} \left(\frac{1}{m} G_c \int_{j \cdot \Delta T}^{j \cdot \Delta T + T_{int}} E_{ki}(t) \cdot dt \right), \quad (1) $$

where N is the number of accumulations, G_c is the global conversion gain and E_{ki} is the k_{nth} optical signal received by the row i.

B. Description of the sweep unit

The sweep unit previously reported in [18] consists of a cascaded chain of inverter with constant delays and fixed sweep speed. The new architecture of the sweep unit, depicted in Fig. 2, generates a flexible sweep speed in the range from 125 ps/pixel up to the DC operation. It consists of two main delay generators. The fast sweep unit (FSU) is useful for sub-nanosecond sample period operation. It is

composed of a Delay Locked Loop (DLL) and two Voltage-Controlled Delay Lines (VCDLs). The observation time of the camera is set by the DLL reference clock period. The mirror VCDLs are driven by the same control voltages V_{hl} and V_{lh} as the master DLL and allow an asynchronous delay generation with respect to the reference clock. This makes it possible for the proposed generator to be launched from zero-tap position upon external triggering signal, ensuring the synchronization between the beginning of the acquisition procedure and the luminous phenomenon to be captured. The output taps of the VCDLs are delayed by an adjustable delay ΔT given by the ratio of the DLL Clock to the number of columns m.

The voltage controlled cell is a current starved double inverter with NMOS control transistors. It presents a large delay range and has been optimized for the shortest delay achievable in the CMOS technology employed [21]. The master DLL ensures the stability over temperature and the absolute precision of the delay. Nevertheless, the VCDLs must be exactly matched to ensure the same temporal shifting and duration of integrating window. The $Start$ and $Stop$ trigger signals are generated externally. Using two independent command signals allows reducing the integration time down to 1 ns or less. Results from a similar FSU have been reported in [22] and are summarized on table I.

The slow sweep unit (SSU) is useful for nanosecond up to DC operation. It uses a fast D flip-flop shift register. The sample period ΔT is equal to the frequency period of the register clock frequency REG $Clock$. The linearity of such a delay generator is very good as it is linked to the clock stability. Nevertheless, in an asynchronous operation, the timing jitter of the generated $start_j$ and $stop_j$ signals with respect to the trigger signal $start$ and $stop$ is equal to the sample period peak-to-peak.
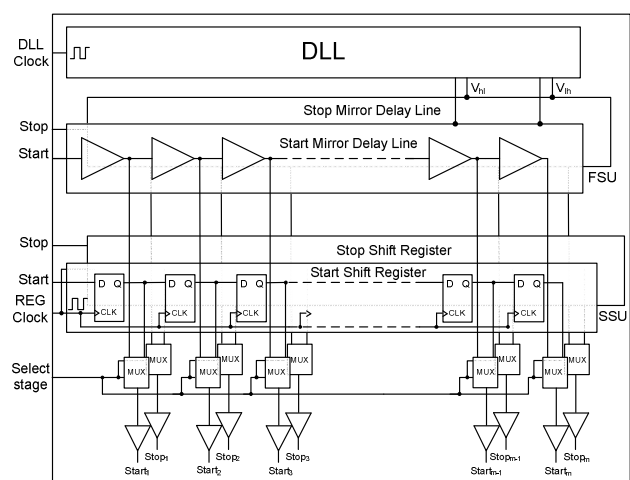

Figure 2. The sweep unit architecture.

C. *Description of the pixel*

The architecture of the pixel is shown in Fig. 3. A Nwell/Psub photodiode is used in order to have a broadband light sensitivity and a low capacitance to enhance the conversion gain. The Start$_i$ and Reset transistors reset the photodiode and the readout node (RN), respectively. Shuttering is carried out by the Stop$_i$ transistor and the charges are transferred from the internal node (IN) to the readout node by the Acc transistor. The *Acc* and *Reset* commands are global for the entire matrix.

The static operation and characterization of the MISC obtained under continuous illumination in single shot and in accumulation mode and has been reported in [23]. In the next section, the repetitive mode with analog on chip accumulation is described and some experimental results are shown.

III. ANALOG ACCUMULATION FEATURE

A. *Description of the analog accumulation operation*

The accumulation mode is performed by several acquisitions of one repetitive pulse. The initial phase consists in resetting the readout node with the Reset transistors. Then the readout node RN is left floating, ready to accumulate several low intensity acquisitions. Each acquisition is composed of four operating phases: the reset of the photodiode, the integration of the light, the sampling and the charge transfer from the internal to the readout nodes. During the reset of the photodiode the Stop transistor is held high to have the same potential on the photodiode and on the internal node (Fig. 3). The integration begins when the command of the Start$_i$ transistor is at low level and finishes when the command of the Stop$_i$ transistor falls at low level. Indeed, on the falling edge of the signal *Stop$_i$* the potential of the photodiode is sampled and hold in the IN. Finally, the charges stored in this node are transferred to RN by applying an intermediate voltage between V$_{RR}$ and V$_{RPD}$ to the gate of the transistor Acc (e.g., 2.5 V) during the transfer time T_{Acc} [18]. In the accumulation mode this
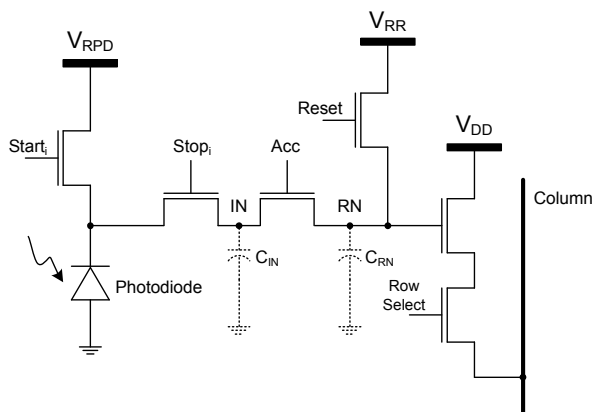
sequence is repeated several times, without resetting the readout node.

B. *Analog accumulation performances*

The maximal repetition rate of the acquisition is limited by the sum of the reset phase, the observation time $m \cdot \Delta T$ and the transfer time T_{Acc}. The reset phase occurs in less than 1 ns. The functions of the RN voltage versus the photodiode reset voltage (V$_{RPD}$) for different transfer durations from 1 ns up to 10 μs, with V$_{RR}$ = 3.3 V and Acc = 2.5 V, are depicted on Fig. 4. These functions are composed of 3 regions. In the first region, the gain is zero, i.e., no charge is transferred as the Acc transistor is turned off, because V$_{RPD}$ is above a threshold voltage (V$_{TH}$) depending on T$_{Acc}$. The second region illustrates the charge transfer operation that occurs when the photodiode voltage V$_{RPD}$ is lower than the previous V$_{TH}$ and above a second threshold voltage depending of T_{Acc}. Below this last voltage, the Acc transistor is completely turned on and the RN and IN nodes are shorted, i.e., voltage V$_{IN}$ and V$_{RN}$ are equal, consequently, the gain gets lower [23]. The region 2 is the usable mode for the accumulation process and the simulation results show that the charge transfer efficiency is independent of the T_{Acc} duration if the photodiode reset voltage is well adjusted (Fig. 4). In this case, V_{RN} is given by

$$V_{RN} = \frac{C_{IN}}{C_{RN}}\left(V_{IN} - \left(V_{Acc} - V_{TH}\right)\right) + V_{RN_0} \qquad (2)$$

where V$_{RN0}$ the previous voltage of the RN. This indicates that the maximal repetition rate is mainly due to the temporal window as the reset and transfer phase can be reduced to a few nanoseconds.

This behavior arises from the transient phenomenon of the charge transfer. At the beginning of the charge transfer, the V$_{GS}$ of the Acc transistor is well above its threshold voltage but as soon as the charges are transferred, the potential of the internal node V$_{IN}$ increases very quickly,
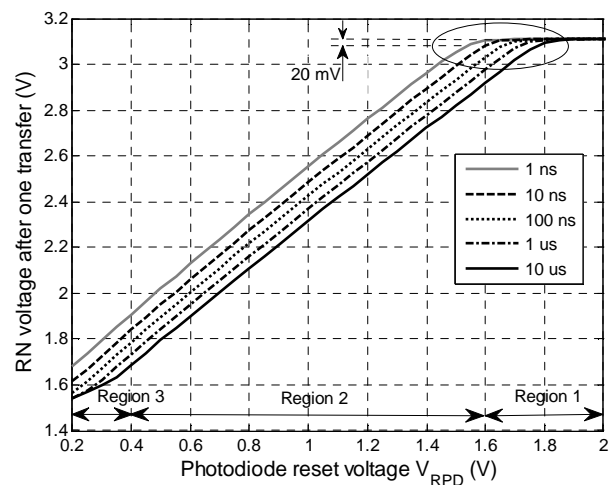

Figure 3. Pixel architecture of the MISC.

Figure 4. Simulation of the charge transfer efficiency for several T$_{Acc}$.

i.e., in less than 1 ns, reducing the V_{GS} down to the threshold. Then the transistor is turning off very slowly while the charge flow gets lower and lower. Consequently, when T_{acc} gets longer, more and more of those charges are transferred maintaining the transfer efficiency even with a higher V_{RPD}. For linear operation, the inflections in the V_{RN} to V_{RP} curves visible in the ellipse of the Fig. 4 must be avoid. Consequently, an overvoltage of 20 mV of dark signal must be added at each accumulation. Assuming a dynamic range of 1 V, the number of accumulations is limited to about 50 shots.

IV. MEASUREMENTS

A. Charge transfer efficiency

A 64×64 pixels prototype has been realized in the standard AMS 0.35 μm CMOS technology. In order to evaluate the highest repetition rate, the transfer gain efficiency versus the V_{RPD} for different T_{Acc} has been measured (Fig. 5).
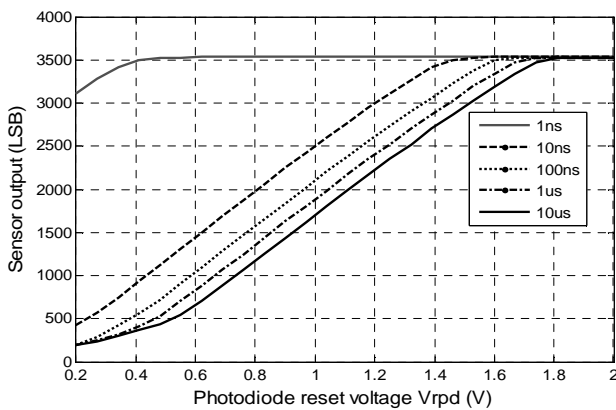

Figure 5. Measurement of the charge transfer efficiency for several T_{Acc}.

Fig. 5 shows that the transfer efficiency is effectively independent of T_{acc} if the photodiode reset voltage is well tuned. For T_{acc} equal 1 ns and 10 ns the curves are shifted to a lower V_{RPD} than expected by the simulation. This is due to the external pulse generator we use to generate the Acc control signal. Indeed, the rising and falling time of the signal delivered by this unit is about 1 ns, consequently, the effective T_{acc} is reduced for a pulse duration a few nanoseconds. Nevertheless, this measurement is the proof that T_{acc} can be reduced to a few nanoseconds, leading to a repetition period very close to the observation time.

B. Test bench for repetitive pulse observation

The experimental setup for the observation of repetitive optical pulses is show in Fig. 6. It is composed of a pulsed laser source, a synchronization unit, a delay line and an optical fiber. The accumulation is possible only if the MISC is synchronized with the source. Since the laser is subjected
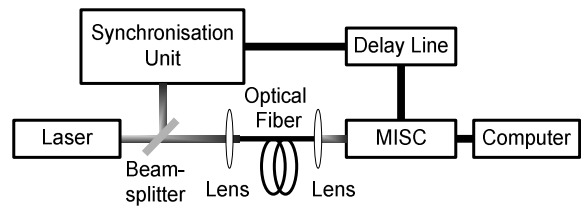

Figure 6. Experimental setup for repetitive pulses observation

to jitter, the synchronization is operated by using a photodiode trigger unit. The delivered trigger signal is split between the *Start* signal of the sweep unit and the *Stop* signal. A flexible very short delay (a few nanoseconds or less) of integration ΔT is externally added by a passive jitter-less delay line. The laser source is delayed by an optical fiber to fit the capture temporal window of the MISC. The electronic setup inside the camera is composed of a FPGA that delivers the remaining command signals (Acc transistor, readout, etc.), a 12 bits analog to digital converter and the digital acquisition board. For this measurement, the FSU has been used with a 22 MHz reference clock which corresponds to an observation window of 45.5 ns and a sample period of 710 ps.

C. Observation of light pulses in accumulation mode

A vanadate Q-switched diode pumped solid state laser which delivers pulses of 6 ns FWHM, at 532 nm, with a frequency repetition of 100 Hz has been used as the optical source. The laser beam was spread with a cylindrical lens in order to illuminate uniformly one row on the array sensor. A luminous pulse of low intensity, spatially focused on 20 μm, has been observed with three different operation modes of our sensor. The integration time used to obtain measurements presented on Figs. 7, 8 and 9 was fixed at 1 ns. With this short T_{int}, the convolution effect can be neglected with a pulse FWHM of several nanoseconds. On
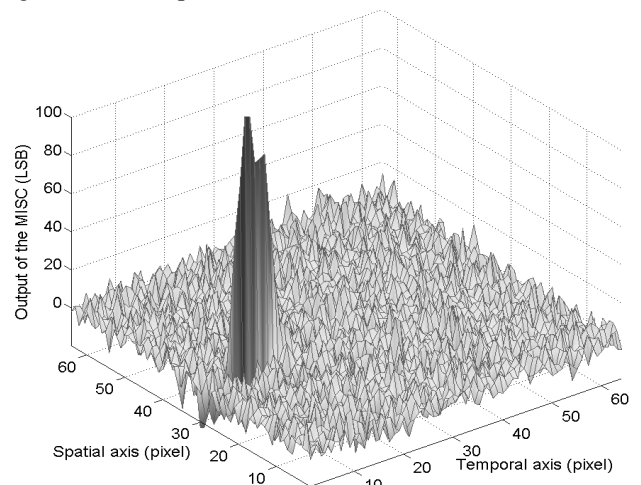

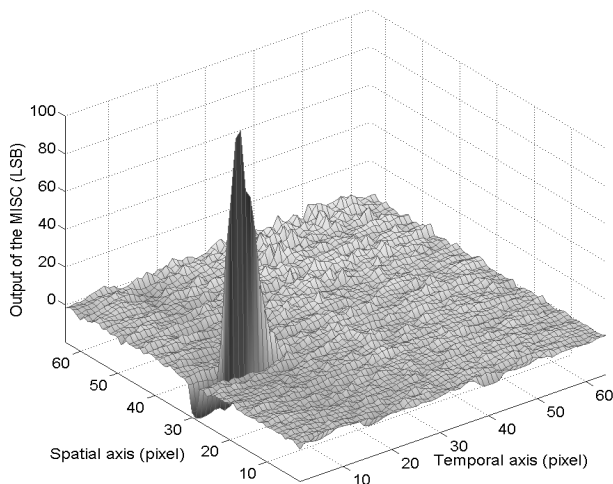Figure 7. Measurement of a 532 nm laser pulse obtained in the single shot mode acquisition.

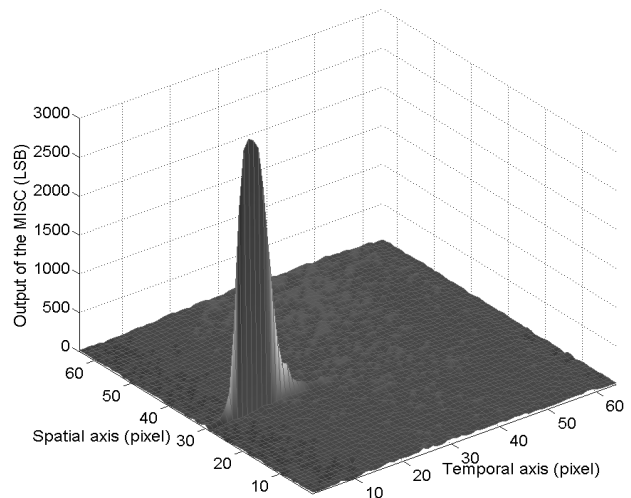Figure 8. Measurement of a 532 nm laser pulse obtained with the computed averaging of 200 laser pulses.

Figure 9. Measurement of a 532 nm laser pulse obtained with 20 analog accumulations.

all these images the dark level of each pixel has been subtracted in order to remove the fixed pattern noise (FPN).

Fig. 7 shows the luminous pulse measured in single shot mode. It is not easy to discern the pulse shape among the noise. Indeed, the signal to noise ratio (SNR), i.e, the ratio between the normalized Gaussian power and the normalized RMS noise, is evaluated to 29.

Fig. 8 presents the same signal measured without analog accumulation but with 200 frame software acquisitions, i.e., the resulting picture is the computed averaging of several single shot laser pulses. Of course the level of the luminous pulses has the same order of magnitude, but in this case, the effect of the readout noise is expected to be attenuated by a ratio of $200^{0.5}$. The measured SNR is 155. The improvement of the SNR by a factor 5.4 is less than then expected one. The difference probably results by some speckle effects than are not averaged with this technique.

Finally, Fig. 9 presents the luminous pulse resulting from 20 on-chip analog accumulations, without external acquisition. The signal amplitude is about 20 times higher than the one obtain in single shot with its associated photodiode KTC noise, whereas KTC noise of the RN and the readout noise are kept constant. Indeed, there are just one Reset of RN and one readout per acquisition The result shows that the readout noise is the dominant noise, thus, to first approximation, the expected SNR improvement ratio is roughly 20 while neglecting the photodiode KTC noise, the photonic noise and the speckle effect. The SNR obtained in this mode is 215, i.e. a improvement ratio of 7.4 compare to the single shot. This is higher than the software averaging for an order of magnitude less acquisition. Consequently, the analog on chip accumulation capability is a powerful feature, which improves the SNR of an ISC. Moreover, the repetition rate in this mode is not limited by the readout

time but only by the transfer time. It is thus not limited to a few hundred of Hz but can be higher than 50 MHz.

D. Temporal resolution

During these measurements, the measured FWHM is 8 ± 0.5 pixels. As the sampling period is 710 ps/pixel, it means that the observed pulse duration is 5.7 ± 0.4 ns FWHM, which is very close to the 6 ns measured by a fast PiN photodiode and an oscilloscope. Consequently, the temporal resolution is better than 6 ns at 532 nm. Measurement of a femtosecond laser pulse at 400 nm with an integration duration ΔT of 400 ps indicates that the temporal resolution is 1.1 ns FWHM (see Fig. 10). Preliminary results obtained with the picoseconds laser diode generator described in [24] show a temporal resolution very close to the nanosecond too at 650 nm whereas it is degraded to more than 3 ns at 808 nm. This
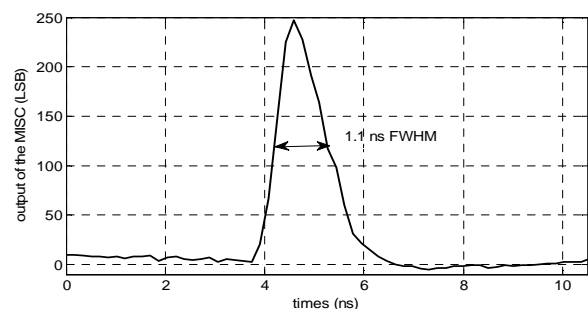

Figure 10. Measurement of a 400 nm femtosecond laser pulse obtained with the computed averaging of 500 laser pulses.

degradation of the temporal resolution is due to the slow transient response of the used Nwell/Psub photodiode at such a long wavelength.

TABLE I.   PARAMETERS AND PERFORMANCES OF THE MISC

Quantity	Value
Pixel pitch	$20\mu m \times 20\mu m$
Fill factor	47 %
Conversion gain	4.8 ± 0.4 µV/e
Sweep speed (ΔT/pixel)	From 125 ps/pixel up to DC
Sweep speed drift	<0.05%/°C
Timing jitter	<70 ps p-p@150ps/pixel (FSU) [22] < 700 ps p-p@770ps/pixel (FSU) [22] <ΔT p-p Slow sweep unit (async SSU)
Temporal axis linearity	Better than 1%
Temporal resolution	1.1 ns @ 400 nm 3.6 ns@ 808 nm
SNR single shot	29
SNR with 200 software accumulation	155
SNR with 20 on chip analog accumulation	215
Max frame per second	500 Hz
Repetition rate in analog accumulation mode	From single shot up to 50 MHz
Max accumulated shot	50

V. CONCLUSION

This work showed that it is possible to realize an integrated streak camera in CMOS technology operating in a accumulation mode at a high repetition rate of more than 50 MHz. This system, carried out in a 0.35 µm AMS CMOS technology, allows the observation of short luminous phenomena in repetitive mode by analog accumulation of the photo-charges inside the sensor with a temporal resolution close to the nanosecond. The analog accumulation feature increases the SNR proportionally to the number of accumulations. However, the maximum number of accumulations is limited to 50 to avoid nonlinear operation. Combination of both the analog and software accumulation could be used to enhance the SNR to a higher value.

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