Comparative Analysis of 130nm PDSOI and 28nm FDSOI Technologies for 5G Power Amplifier Applications

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***Abstract*— This paper analyzes 130 nm Partially Depleted (PD) Silicon-On-Insulator (SOI) and 28 nm Full Depleted (FD) SOI technologies and proposes the design of two Power Amplifiers (PAs) for 5G Narrow Band-Internet of Things (NB-IoT) applications. They were fabricated and measured, demonstrating the gain adjustment capability of FDSOI technology via back-gate voltage, allowing approximately 3.6 dB of gain adjustment. Both PAs consist of a gain stage (driver) and a power stage, using pseudo-differential and cascode topologies. The 28 nm PA includes an additional stacked transistor in the power stage to accommodate a higher drain bias voltage. Both PAs met the required performance parameters in post-layout simulations, achieving maximum Power-Added Efficiency (*PAEmax)* of 49% and 38.5%, gain of 36 dB and 34 dB and saturated Power (*Psat)* of 32 dBm and 28.8 dBm, respectively for 130 nm and 28 nm, placing them at the state-of-the art.**

Keywords- Power Amplifier; CMOS; 130 nm PDSOI; 28 nm FDSOI; 5G applications; Nb-IoT.

I. INTRODUCTION

The transition from 4G Long Term Evolution (LTE) to 5G has revolutionized the Internet of Things (IoT) with the advent of massive IoT, enabling the connection of numerous devices simultaneously. Narrow Band-Internet of Things (NB-IoT), a key 5G standard within Low-Power Wide-Area Networks (LPWAN), addresses the need for massive IoT by supporting battery-powered devices with extended lifespans and optimized installation costs. Operating on licensed 3GPP bands, NB-IoT offers higher data rates compared to unlicensed LPWAN technologies like LoRa and Sigfox. It achieves extensive coverage through transmission repetitions and increased signaling power, while its Single-Carrier Frequency Division Multiple Access (SC-FDMA) modulation reduces Peak-to-Average Power Ratio (PAPR), improving Power Amplifier (PA) efficiency and ensuring suitability for massive IoT applications [1].

Silicon-on-insulator (SOI) technology is pivotal for overcoming RF integration challenges in IoT circuits. Leveraging the high integration capabilities of Complementary Metal-Oxide-Semiconductor (CMOS), SOI reduces parasitic capacitances with a BOX layer, enhancing performance by over 20% [2]. While SOI improves reliability, energy efficiency, and reduces variability compared to bulk CMOS [3], NB-IoT's SC-FDMA modulation imposes strict PA design requirements, demanding linear operation and efficiency at low power. Advanced SOI technologies like Partially Depleted SOI (PDSOI) and Full Depleted SOI (FDSOI) provide tailored solutions, excelling in isolation and low-power scenarios, respectively [4].

This paper analyzes the 130 nm PDSOI and 28 nm FDSOI technologies and proposes the design of two PAs for the 5G NB-IoT applications (see Fig. 1). The gain and linearity adjustment capability via the back-gate voltage of FDSOI technology is demonstrated. Both circuits consist of PAs with a gain stage (driver) and a power stage, using pseudo-differential and cascode topologies.

Following, Section II compares 130 nm PDSOI and 28 nm FDSOI technologies, highlighting their components and PA design methodology. Section III presents post-layout simulation and measurement results, including performance analysis, gain tuning via back-gate voltage for the 28 nm PA, and a state-of-the-art comparison. Section IV concludes with findings and future research directions.

II. DESIGN METHODOLOGY

This design methodology section presents a study on technologies and the designed PAs. Details about the metal layers of the 130 nm FDSOI and 28 nm PDSOI technologies are presented, followed by comparing both technologies

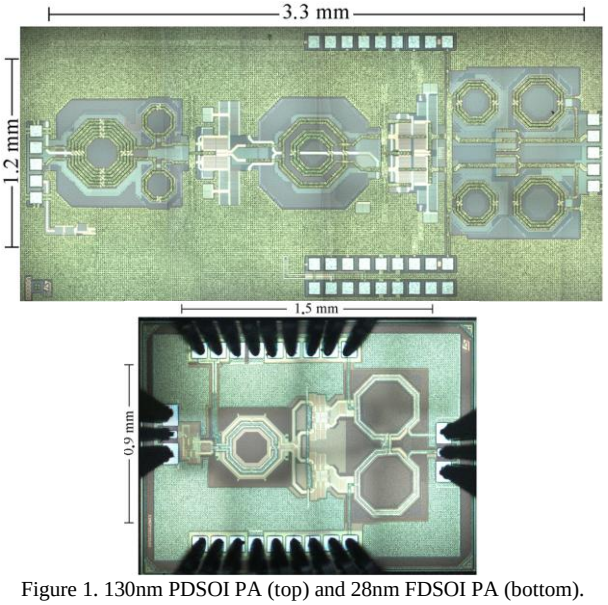

Figure 1. 130nm PDSOI PA (top) and 28nm FDSOI PA (bottom).

inductors, capacitors, and transistors. Based on this analysis, the following subsection provides details of the schematics of the two designed PAs, highlighting their similarities and differences.

A. *Evaluation of Passives and Transistors of SOI Technology*

Fig. 2 presents the metal layers of the 130 nm PDSOI and 28 nm FDSOI. The first observation concerns the difference in the number of available metal layers and their thickness. Indeed, the smaller the technology node, the higher the integration density, which also requires an increase in interconnection density. Several solutions are implemented to increase this density [5]. The rise in metal layers and the reduction of the minimum etching widths are the most common and easiest to apply. However, reducing the minimum etching width impacts the maximum thickness metal layers can have due to manufacturing processes. This consequently explains the reduction in the thickness of the metal layers in the 28 nm FDSOI.

Figs. 3 and 4 show an example of the inductor and capacitor performances for each technology, respectively. The comparison was made with inductors using an octagonal topology [6]. In 28 nm FDSOI, the inductors are designed on the three thick levels ALU-IB-IA (see Fig. 2) to reduce resistivity and increase the quality factor at low frequency. In 130 nm PDSOI, the two thick metal levels ALU-M4U (see Fig. 2) are used. For the same topology, the inductor achieves a quality factor Q of 28 at 2 GHz in 130 nm PDSOI, compared to 15 in 28 nm FDSOI. However, high-value inductors exhibit better high-frequency behavior in 28 nm FDSOI due to a higher self-resonant frequency, indicating lower parasitic capacitances. For capacitors, the quality factor at 2 GHz in the 130 nm technology is around 300 for a capacitance of 1.1 pF (see Fig. 4). For the 28 nm technology, the quality factor at 2 GHz is 40 for a capacitance of 0.88 pF. Indeed, the 28 nm technology has much thinner and more resistive metal layers than the 130 nm technology. On the other hand, the capacitors in 130 nm occupy larger silicon areas.

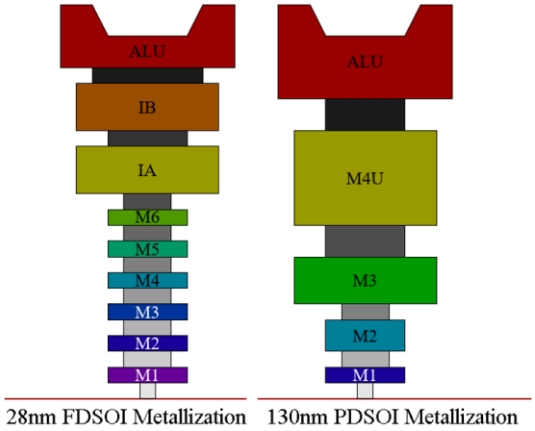

Figure 2. Metal layers of 28 nm FDSOI and 130 nm PDSOI technologies.

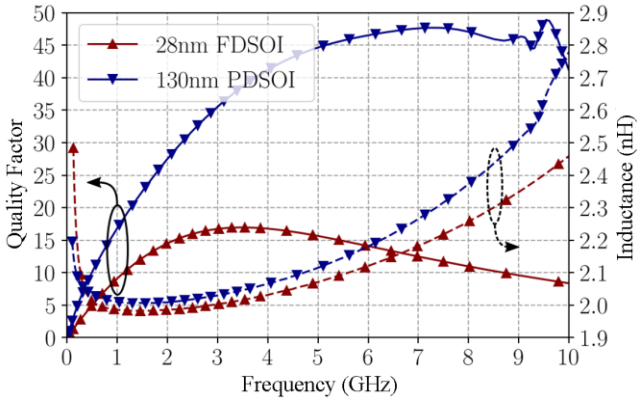

Figure 3. Comparison of inductances from 28 nm FDSOI and 130 nm PDSOI technologies.

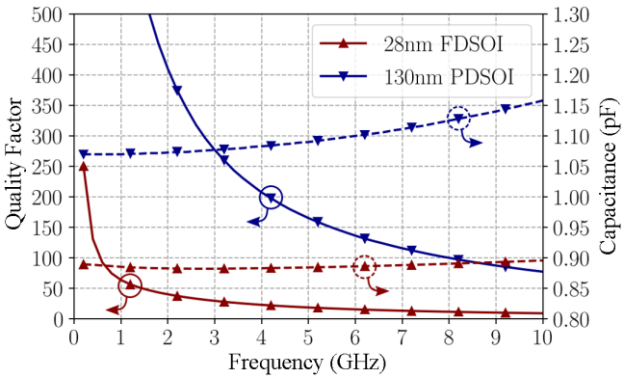

Figure 4. Comparison of capacitances in 28 nm FDSOI and 130 nm PDSOI technologies.

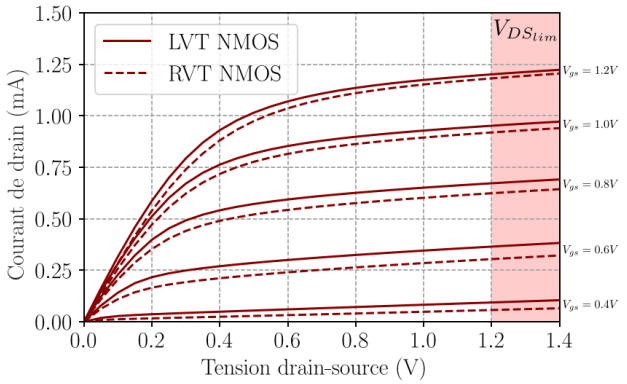

Figure 5. Output Transfer Characteristics Id(Vds) in 28 nm FDSOI.

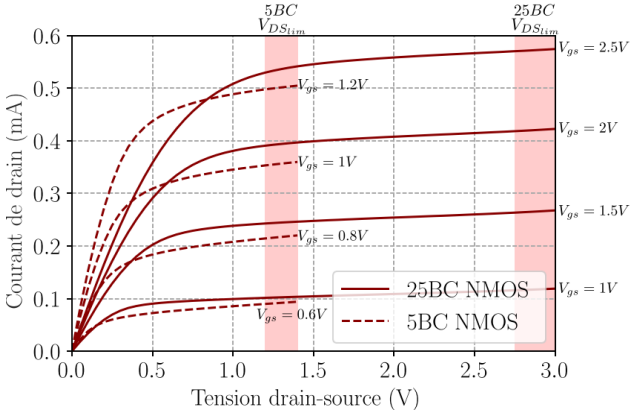

Figure 6. Output Transfer Characteristics Id(Vds) in 130 nm PDSOI.

Figs. 5 and 6 show NMOS transistors' output transfer characteristics for RF applications for PA design. The transistors from 28 nm FDSOI have a higher current density, reaching 1.2 mA at the maximum *Vgs* voltage, compared to 0.58 mA for the thick oxide transistor in 130 nm PDSOI. Additionally, the 28 nm transistors have lower threshold voltages, around 250 mV, compared to approximately 350 mV for the 130 nm transistors, enabling operation at lower voltages.

The 130 nm PDSOI technology offers better performance in terms of transistor quality in the saturation region. Indeed, the slopes *∂Id/∂Vds* in the saturation region are lower for the 130 nm PDSOI transistors than for the 28 nm FDSOI transistors. This also represents that the *gds* in 130nm are lower than in 28nm. The consequence is achieving more linear transistors for large-signal applications.

B. Power Amplifier Design Methodology

The two PA architectures were designed (see Figs. 7 and 8) based on the preliminary sizing of the transistors and the analysis of the presented passive components. Both architectures were designed to achieve comparable performance and NB-IoT restrictions in post-layout simulations. This allows for evaluating their fabricated circuit measurements to compare the two technologies and discuss their advantages and limitations concerning the target application.

Each circuit includes a driver stage with a single-ended input and pseudo-differential cascode topology at the output. Additionally, both circuits feature a pseudo-differential cascode power stage. The 28 nm design (see Fig. 7) employs a triple-cascode topology in its power stage to enable a supply voltage (*Vdd*) closer to the 130 nm technology, facilitating a fairer comparison. Both circuits were designed to achieve post-layout simulations (PLS) at the central frequency of 1.85 GHz, a bandwidth exceeding 400 MHz, a gain of 35 dB, a maximum Power-Added Efficiency (PAE_{max}) above 30%, and power back-off PAE (PAE_{PBO}) above 20%.

The 130 nm PDSOI PA, depicted in Fig. 8, incorporates a pseudo-differential cascode power stage alongside a pseudo-differential cascode driver setup. This configuration ensures a straightforward design and excellent performance tailored for NB-IoT applications. The design achieves higher output power by employing pseudo-differential architecture while minimizing constraints on the ground return path by suppressing even harmonics. Furthermore, the cascoded transistor arrangement enhances the amplifier's gain, allowing it to meet the 35 dB target specification. To ensure stability, given the high gain, neutralization capacitors (C_{neutro}) are incorporated. The matching networks are designed to enable broadband operation facilitated by a broadband matching transformer. In the 130nm technology, for the power stage, transistors were dimensioned with W_{total}=1200 µm and for the driver stage W_{total}=300 µm and the circuit was biased with *Vdd*=5V.

Fig. 7 shows the complete schematic of the PA in 28 nm FDSOI technology. Two power cells are combined in the

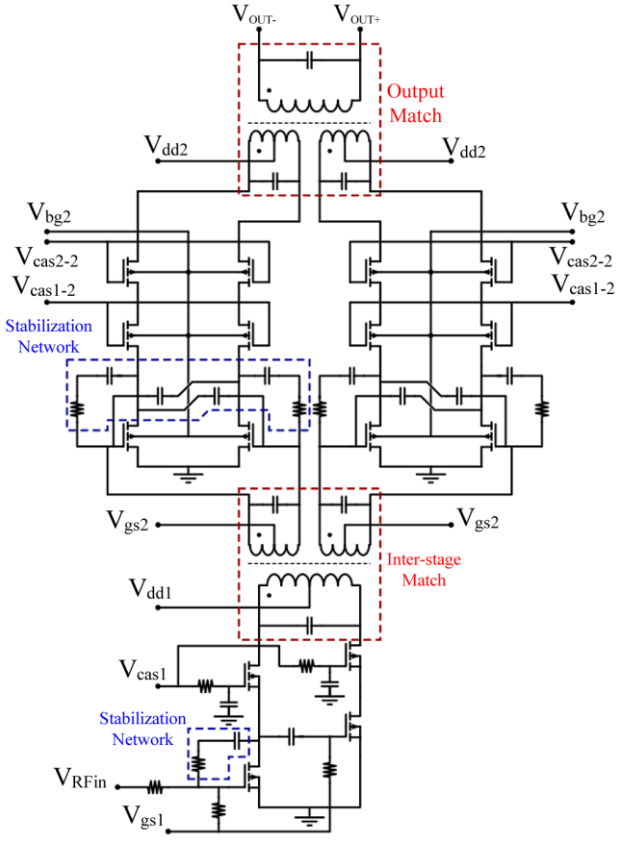

Figure 7. PA in 28 nm FDSOI technology schematic.

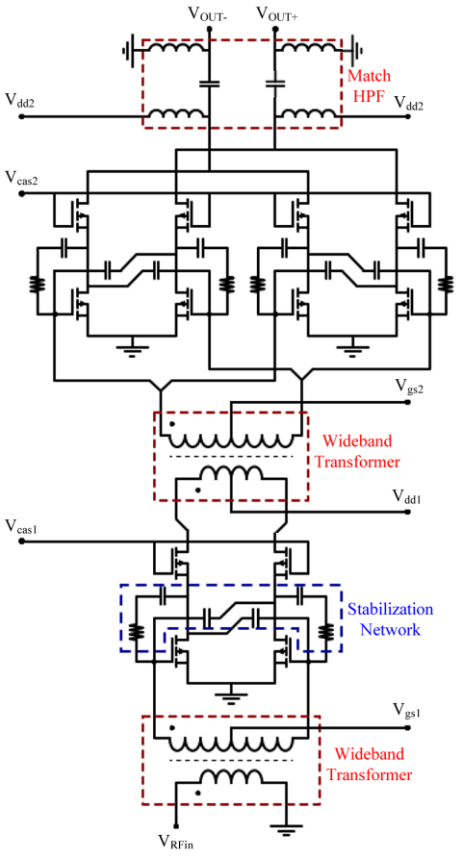

Figure 8. PA in 130 nm PDSOI technology schematic.

power stage to compensate for the technology's power limitations. The PA consists of two triple-stack power cells, enabling a total output power of 28 dBm. The output matching network uses a distributed active transformer (DAT) to optimize the load impedance at the output through series recombination. The inter-stage matching is designed around a 2-to-4 transformer, which performs impedance matching while distributing power across each power cell. Finally, the driver employs a cascode active balun topology, eliminating the need for a passive input balun. In the 28nm technology, the power stage used transistors with W_{total}=900 µm and for the driver stage W_{total}=225 µm, and the circuit was biased with *Vdd*=3V

This circuit explores the potential for improving output power using stacked architecture and back-gate biasing, aiming to meet the power requirements of NB-IoT applications. The back-gate voltage permits fine-tuning of the gain and linearity performance, as will be shown in the results section.

III. RESULTS AND DISCUSSIONS

A. Post-layout Simulation and Measurement Performance

Figs. 9 and 10 present the PA in 130 nm PDSOI and the PA in 28 nm FDSOI technologies S-parameters post-layout simulation (PLS) and measurements performance from 1 GHz to 3 GHz, respectively. The 130 nm PA presents an almost constant *S21* performance (between 35 dB and 39 dB) from 1.55 GHz to 2.4 GHz, an *S22* near -3 dB, and an *S11* less than to -5 dB in this frequency range. The 28 nm PA presents flatter behavior, with a maximum *S21* performance of 33 dB between 1.5 GHz and 1.8 GHz, *S22* less than -5 dB, and *S11* less than -15 dB.

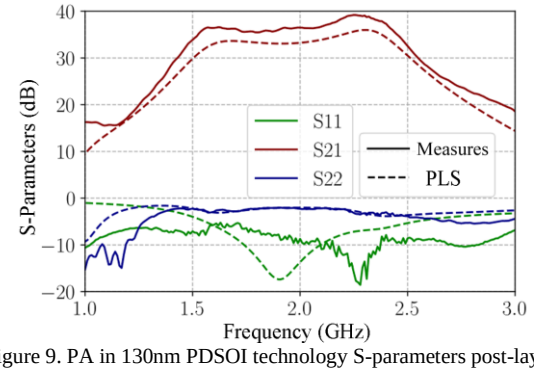

Figure 9. PA in 130nm PDSOI technology S-parameters post-layout simulation (PLS) and measurements performance.

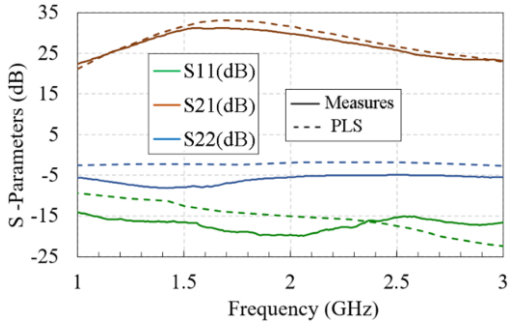

Figure 10. PA in 28nm FDSOI technology s-parameters post-layout simulation (PLS) and measurements performance.

Fig. 11 presents the PA in 130 nm PDSOI technology gain and PAE performances for post-layout simulation and measurements in the frequency of 1.85 GHz. The measured gain performance presents a class AB characteristic shape, with 34.5 dB in low power and a maximum of 36 dB; the maximum PAE reaches 48.5% at a P_{sat} of 31 dB in PLS and 38% in measurements at a P_{sat} of 28 dBm.

Fig. 12 presents the PA in 28 nm FDSOI technology gain and PAE performances for post-layout simulation in the frequency of 1.85 GHz. The gain performance achieves 33.26 dB in low power and a maximum of 34.72 dB; the maximum PAE reaches 38.5% at a P_{sat} of 28.5 dB. The transistors were optimized until the edge of stability parameters predicting that losses in further components would assure stability. However, the implemented circuit presented stability issues in high-output power.

B. Fine Tuning Gain with Back Gate Transistor Bias in 28nm FDSOI Technology

In CMOS SOI technology, access to the transistor's back-gate provides additional control over the device's characteristics that can be leveraged to modify key performance parameters of a PA, such as output power, gain, and PAE. Changing the back-gate bias (*Vbg*) effectively modulates the transistor's threshold voltage *Vth*. A lower threshold voltage can increase the transistor's current driving capability, which may increase the power output and, potentially, the gain, depending on the biasing conditions.

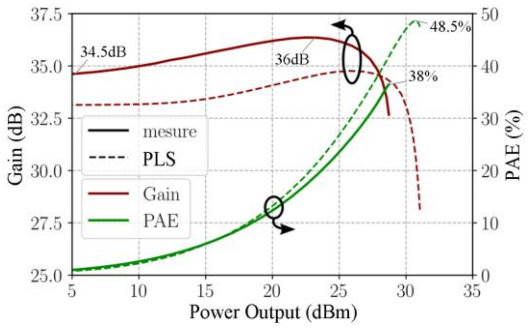

Figure 11. 130nm PA gain and PAE post-layout simulation and measured performances in 1.85 GHz.

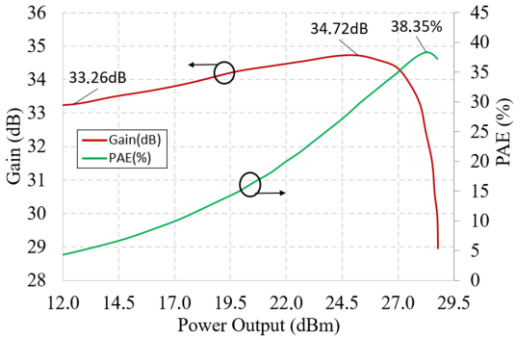

Figure 12. 28nm PA gain and PAE post-layout simulation performance in 1.85 GHz.

However, this also can lead to higher power consumption and decreased efficiency.

Fig. 13 presents the measured performance of gain versus P_{out} for the PA in 28 nm with three different levels of *Vbg* voltage. For *Vbg=2V*, the transistors are more biased for maximum conduction, resulting in the highest initial gain of 31.3 dB and a curve with the typical shape of a class AB PA, reaching 21.8 dBm of linear output power. A *Vbg=1V* offers a more balanced operation, with a lower initial gain (30.2 dB) but greater linearity up to higher output power levels (*OCP1*=22.2 dBm). Meanwhile, *Vbg=0V* shows the lowest gain (27.7 dB) due to reduced transistor conduction but the highest linear output power (*OCP1*=23.6 dBm).

These results demonstrate how the back-gate voltage in 28nm FDSOI technology can be leveraged to optimize amplifier performance according to specific requirements for gain and linearity.

C. 130nm and 28nm Power Amplifier Comparisons

This subsection compares the two PAs in size and performance. As seen earlier at the start of the results section, the PA implemented in 28 nm technology occupies an area corresponding to 34% of the area occupied by the PA in 130 nm technology.

Comparing Figs. 9 and 10, the PA based on 130 nm PDSOI technology outperforms the 28 nm FDSOI in S-parameters performance. The *S21* gain of the 130 nm PA remains around 35 dB in the central range (1.6 to 2.3 GHz), while the 28 nm PA reaches 30 dB only in the range between 1.5 and 1.9 GHz. However, the *S22* and *S11* of the 28 nm PA are more negative (below -5 dB and -15 dB, respectively), indicating better impedance matching at the input and output, with lower signal reflection.

PA gain (dB) and PAE (%) performances can be compared by Figs. 11 and 12. In PLS, the 130 nm PA achieves a higher maximum output power (~31 dBm) than the 28 nm PA (~28.5 dBm), making it more suitable for high-power applications. Considering the PLS performance, the 130 nm PA achieved a saturated output power of 31 dBm and the 28 nm PA achieved approximately 28.5 dBm, making the 130 nm technology more suitable for high-power applications, as expected. The 130 nm amplifier also provides slightly higher gain at lower output power levels. Furthermore, the 130 nm PA shows superior PAE performance in PLS, achieving a maximum of 48.5%, while the 28 nm PA achieves 38.35%. Comparing

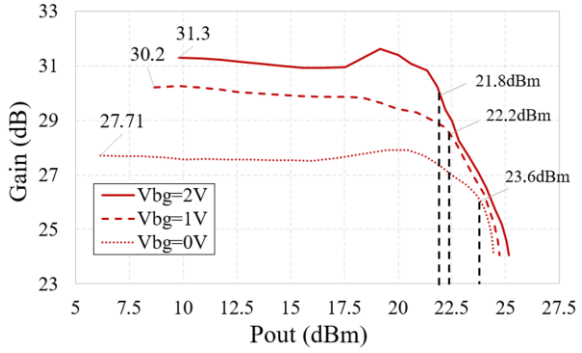

Figure 13. 28nm FDSOI PA gain versus P_{out} measured performances for 3 levels of back-gate voltage.

measurements, Fig. 11 shows that the 130 nm PA achieves a P_{sat} of 28.82 dBm and a P1dB of 27.29 dBm, while the 28 nm PA, in Fig. 13, reaches a P_{sat} of approximately 25.5 dBm and a P_{1dB} of 23.6 dBm.

Although the performance values of the circuit made with 130 nm technology are higher, the circuit in 28 nm technology allows for gain and linearity performance adjustment through back-gate voltage. This enables the choice to operate in either a high-gain mode or a high-linearity mode, depending on the communication requirements.

D. State-of-the-Art Analysis

A comparison with the state of the art is conducted to conclude the performance assessment of the PAs presented in this section. Table I summarizes the state-of-the-art PAs and the performance metrics of the PAs developed in this research.

Considering 5G and NB-IOT applications requiring modulations with high PAPR, the comparison was primarily made with promising topologies and techniques, such as Doherty, Envelope Tracking, and other high-efficiency classes.

It is observed that the two developed PAs outperform all PAs in Table I in terms of gain. Regarding *Psat*, the PA in 130 nm outperforms the works [5] [7] [8] [9] [10]. Regarding PAE, the PA in 130 nm outperforms the works [6] [8] [9] [10], and the PA in 28 nm outperforms the work [8].

Regarding output power, the developed PAs are promising, as they are being compared with Doherty PAs, which consist of two or more PAs in parallel. If double the power were considered for the presented PAs, they would be comparable to Doherty's maximum power-level topologies.

The 130nm PDSOI pseudo-differential PA demonstrates an overall performance superior to the 28nm FDSOI design. PAs [11] and [12] leverage off-chip passive components, which enhance performance due to significantly higher-quality factors than integrated passives. The PA architecture in [13] employs an envelope tracking technique, yielding a substantial improvement in PAE. Lastly, PA [14] is based on a switched amplifier architecture, enabling higher power density.

The PA designed in 28nm FDSOI is competitive with the state-of-the-art performance; however, the low-quality factor of integrated passives tends to reduce the maximum achievable PAE.

IV. CONCLUSION

This paper compares two PAs with some topological differences but similar application intents. Both consist of PAs with a gain stage (driver) and a power stage (PA), using differential and cascode topologies. The PA implemented in 28 nm technology presents a 3-stacked transistor in its power stage to allow for a higher drain bias voltage. This adjustment was deemed fair within the functional comparison, as the technology features thinner layers, necessitating such adaptations. The two employed technologies, 130 nm, and 28 nm, can produce PAs suited for the intended application.

This paper compares the passive and active elements of the two technologies, showing that the 130 nm PDSOI technology has much thicker layers than the 28 nm FDSOI

TABLE I - COMPARING WITH THE STATE-OF-ART

Ref.	Freq. (GHz)	Psat (dBm)	P1dB (dBm)	PAE max (%)	PAE 6dB (%)	Gain (dB)	Topology	Technology	Supply (V)
[15]	2.3	32.8	32	59	40	27.5	LDMOS Doherty	130nm SOI**	3.4
[16]	2.4	35.1	34	53		29.5	Doherty	130nm SOI	5
[5]	1.95	30.5	29.7	53	40	26.5	Doherty	180nm SOI	4
[7]	1.85	31.9	N/A	56.2		14.2	ET PA	180nm bulk	4
[6]	2.6	33.1	N/A	43.5	N/A	28.1	4-stack E/Fodd	45nm SOI	3
[8]	2.4	30.3	N/A	36.5	29.1	N/A	C-commutées	40nm Bulk	2.4
[9]	2.4	31.6	N/A	49.2		N/A	Digital Outphasing	45nm bulk	2.4
[10]	1.85	30.7	28.8	44.4	28	11	Quasi-Doherty	180nm SOI	3
PA 130*	**1.85**	**32**	**30**	**49**	**26.6**	**34**	**Cascode Classe-AB**	**130nm PDSOI**	**5**
PA 28*	**1.85**	**28.8**	**28.3**	**38.5**	**20.8**	**33**	**Triple stack Classe-AB**	**28nm FDSOI**	**3**

*PLS | **SOI with LDMOS option

technology, making it more suitable for power emission. However, the 28nm technology also enables this functionality while occupying three times less space, albeit at a considerably higher cost and with lower performance, given its primary orientation towards digital circuits.

The results indicate that the performance of the circuit fabricated in 130 nm technology is superior to that of the 28 nm circuit. The comparison between PLS and measurements also shows that the 130nm technology is more predictable and mature, as the measurements for the 28 nm circuit deviated further from the PLS predictions.

The 28 nm FDSOI technology enables fine-tuning of the PA's gain through back-gate voltage, thus providing additional operational freedom.

The developed PAs exhibit superior gain performance compared to the state-of-the-art. They are promising in power when used in efficiency-boosting topologies that combine multiple PAs to increase PAE at backoff and maximize output power.

For future research, it is suggested that we explore the use of these PAs in efficiency-enhancing topologies and power-combining strategies, Doherty and Envelope Tracking, facilitating comparisons with the state-of-the-art and contributing to the development of circuits for 5G and NB-IOT applications.

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