Efficient Symbol Detector for MIMO Communication Systems

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***Abstract*—In this paper, an area-efficient symbol detector is proposed for multiple-input multiple-output (MIMO) communication systems with two transmit and two receive antennas. The proposed symbol detector can support both the spatial multiplexing mode and spatial diversity mode in a single hardware, and shows the optimal maximum likelihood (ML) performance. By applying the multi-stage pipeline structure and using the complex multiplier based on polar-coordinate, the complexity of the proposed architecture is dramatically decreased. The proposed symbol detector was designed in hardware description language (HDL) and synthesized to gate-level circuits using 0.13um CMOS standard cell library. With the proposed architecture, the total logic gate count for the detector is 393K, which is reduced by 57% compared with the conventional architecture.**

Keywords-MIMO; ML; multi-stage pipeline; spatial diversity; spatial multiplexing; symbol detector

I. INTRODUCTION

As the demand for a high-rate and reliable wireless data transmission increases, MIMO techniques have attracted considerable attention in recent wireless communication systems such as IEEE 802.11n wireless local area network (WLAN), IEEE 802.16e mobile worldwide interoperability for microwave access (WiMAX), and 3GPP long-term evolution (LTE) [1].

The MIMO techniques can basically be classified into spatial diversity (SD) scheme [2] and spatial multiplexing (SM) scheme [1]. In SM scheme, since independent data streams are transmitted from the individual transmit antennas, the overall data rate is significantly increased as the number of transmit antenna increases. Meanwhile, since SD systems transmit multiple streams bearing the same information, the link reliability is considerably improved from the spatial diversity gain even though there is no increase in data rate.

In SD scheme, the optimal ML symbol detection can be easily accomplished by simple linear combination at receiver [2]. However, since the ML detection for SM scheme requires exhaustive search for all transmitted symbols from all transmit antennas, its complexity is proportional to C^{N_T} (C is the constellation size and N_T is the number of transmit antennas) and exponentially increases as C and N_T increase. Therefore, its real-time implementation is infeasible when a large number of antennas are used together with high constellation size, e.g., 64QAM.

In order to solve this complexity problem, there have been vigorous researches in recent decades [3]-[12]. Among them, modified ML (MML) detection algorithm, which can reduce the complexity by the ratio of $1/C$, was proposed in [10], and was applied to several implementations as in [11]-[12]. Since the recent communication systems mostly support two transmit and two receive antennas to be incorporated into mobile device, MML detection can be considered to be suitable for the symbol detector of those systems because its complexity is proportional to only C.

Although MML detection provides a lower complexity than the classical ML detection, its complexity is still too high to be implemented in real time especially when supporting 64QAM because 64 complex calculations for Euclidean distance should be performed in parallel. Also, since SD scheme such as space-time block coding (STBC) [2] and space-frequency block coding (SFBC) [13] should be supported together with SM scheme in most systems, the design of the efficient hardware architecture is really important for the MIMO symbol detector.

In this paper, we propose an area-efficient MIMO symbol detector supporting both SD and SM modes and present its design and implementation results. By fully sharing the common function blocks and applying the multi-stage pipelining, the proposed detector is implemented with very low-complexity.

This paper is organized as follows: In Section II, MIMO system model is presented, and ML and MML symbol detection algorithms are introduced in Section III. The hardware architecture for the proposed symbol detector is described in Section IV, and the implementation results are presented in Section V. Finally, Section VI concludes the paper.

II. SYSTEM MODEL

Fig. 1 depicts the MIMO system model with N_T transmit and N_R receive antennas $N_T \geq N_R$. The receive signal vector is given by

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$$\mathbf{y} = \mathbf{H}\cdot\mathbf{X}+\mathbf{N} = \begin{bmatrix} \mathbf{h}_1 & \mathbf{h}_2 & \cdots & \mathbf{h}_{N_T} \end{bmatrix}\cdot\mathbf{X}+\mathbf{N} = \begin{bmatrix} h_{11} & h_{21} & \cdots & h_{N_T 1} \\ h_{12} & h_{22} & \cdots & h_{N_T 2} \\ \vdots & & \ddots & \vdots \\ h_{1N_R} & h_{2N_R} & \cdots & h_{N_T N_R} \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_{N_T} \end{bmatrix} + \begin{bmatrix} n_1 \\ n_1 \\ \vdots \\ n_{N_R} \end{bmatrix}, \quad (1)$$

where $x_j, (j=1,2,\cdots,N_T)$ is the signal transmitted from the j-th transmit antenna, $y_i, (i=1,2,\cdots,N_R)$ is the signal transmitted from the i-th transmit antenna; and $h_{j,i}\,(j=1,2,\cdots,N_T,\quad i=1,2,\cdots,N_R)$ is the fading channel between the j-th transmit antenna, and the i-th receive antenna. Also, $n_i, (i=1,2,\cdots,N_R)$ is an independent and identically distributed (*i.i.d.*) complex zero-mean Gaussian noise with variance σ^2 per dimension.

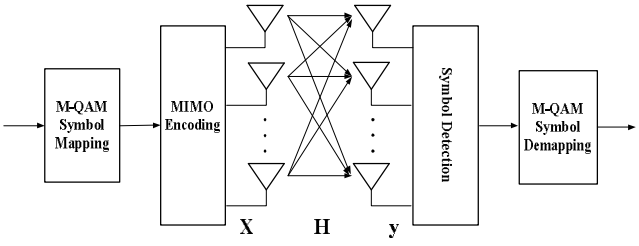

Figure 1. MIMO system model with N_T transmit and N_R receive antennas

III. SYMBOL DETECTION ALGORITHMS

A. ML Symbol Detection Algorithm

The ML detection method, which achieves the best performance by searching for the transmitted signal vector that leads to the minimum Euclidian distance from the received signal vector, can be represented as

$$\mathbf{X}_{ML} = \arg\min_{\mathbf{X}} \left\| \mathbf{y}-\mathbf{H}\cdot\mathbf{X} \right\|. \quad (2)$$

Since its complexity exponentially increases as the number of transmit antennas and the constellation size increase, its real-time implementation is infeasible. For example, in case of N_T=2 and 64QAM, 64^2=4096 searches is required for each received signal vector.

B. Prior Research in Symbol Detection Algorithm

As an alternative of MLD, the concept of sphere detection (SD) was introduced in [4] and has further discussed in various publications [5]–[6]. In order to avoid the exponential complexity of the MLD, the search for the closest lattice point is restricted to include only vector constellation points that fall within a certain search sphere. This approach allows for finding the ML solution with only polynomial complexity for sufficiently high signal-to-noise ratio (SNR) [4]. However, SD has a disadvantage that the computational complexity varies with different signals and channels. Hence, the detection throughput is non-fixed, which is not desirable for the real-time hardware implementation. To resolve this problem, the MLD with QR decomposition and M-algorithm (QRM-MLD) was proposed in [7]. At each search layer in QRM-MLD, only the best M candidates are kept for the next level search and therefore, it has the fixed complexity and throughput which is suitable for pipeline hardware implementation. However, its complexity is still exponentially increasing with the number of transmit antennas, which may bring very large computational complexity when high spectral efficiencies are required to support higher communication rates [9].

C. MML Symbol Detection Algorithm

The MML technique that reduces dramatically the computational complexity of ML technique without degradation performance was introduced in [10]. Table I describes the symbol detection algorithm based on MML detection, where **C** is the set consisting of the constellation points and Q(-) represents a slicing (quantization) function. As depicted in Table I, with the MML symbol detection, the required computational number of MML metric for symbol detection is C^{N_T-1}, while that of ML metric is C^{N_T}. The MML algorithm reduces the computational complexity of the ML algorithm significantly, however, especially when supporting 64QAM, its complexity is still too high to be implemented in real-time. Therefore, efficient architecture design for the real-time implementation is required.

TABLE I. MML SYMBOL DETECTION ALGORITHM

Step	Description
(1)	*metric = big number,*
(2)	$a = \mathbf{h}_2{}^H\mathbf{y}$,
(3)	$b = \mathbf{h}_2{}^H\mathbf{h}_1$,
(4)	$norm = \left\|\mathbf{h}_2\right\|^2$,
(5)	*for l = 1 : |C|,*
(6)	$x_1 = \mathbf{C}(l)$,
(7)	$\tilde{\mathbf{y}}_1 = \mathbf{y}-\mathbf{h}_1 x_1$,
(8)	$x_2 = Q(a-bx_1)$,
(9)	$metric\_temp = \left\|\tilde{\mathbf{y}}_1-\mathbf{h}_2 x_2\right\|^2$,
(10)	*if metric_temp < metric*
(11)	$x_{ML} = [x_1\ x_2]^T$,
(12)	*metric = metric_temp,*
(13)	*end,*
(14)	*end.*

IV. DESIGN OF HARDWARE ARCHITECTURE FOR THE PROPOSED MIMO SYMBOL DETECTOR

The efficient hardware structure of the MIMO symbol detector to support all MIMO transmission modes is presented in this section. In order to achieve the more

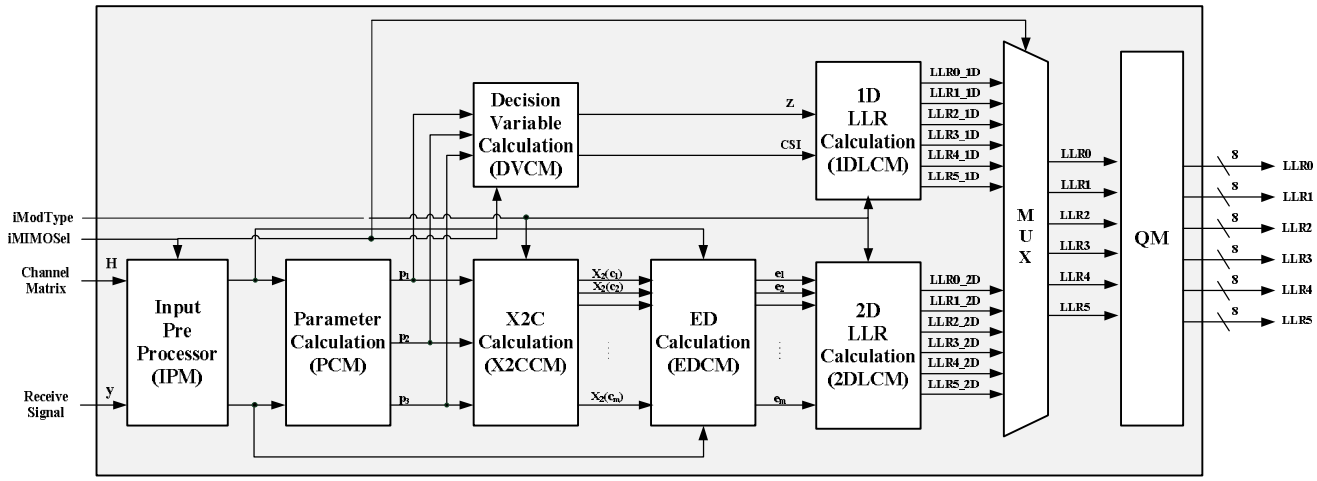

Figure 2. Block diagram of the proposed symbol detector for 2x2 MIMO systems.

reliable performance and higher-rate data transmission, the latest wireless communication systems specify to support SD mode such as single-input multiple-output (SIMO), multiple input single-output (MISO), STBC and SFBC as well as SM mode. If the symbol detector for each mode is designed independently, it is not efficient because the hardware complexity is a very burdensome to be implemented in real time. By sharing commonly used function block for all MIMO modes, the complexity of the proposed architecture is dramatically decreased.

Fig. 2 shows the proposed hardware structure of 2x2 MIMO symbol detector and Table II summarizes the procedure of proposed symbol detection to support all of transmission modes. The proposed structure of MIMO symbol detector is composed of input preprocessor module (IPM), parameter calculation module (PCM), decision variable calculation module (DVCM), X2C calculation module (X2CCM), Euclidean distance calculation module (EDCM), 1D LLR calculation module (1DLCM), 2D LLR calculation module (2DLCM) and 8-bit quantization module (QM).

A. Input Preprocessor Module (IPM)

Fig. 3 shows the hardware block diagram of IPM, which set the input data of PCM for MIMO mode by reordering the estimated channel vectors and received signal vector. Especially, the column-switching of the channel matrix, **H**, is performed for multi-stage pipelining in case of SM mode. Since the vertical coding [13] for SM mode is generally specified in most recent wireless communication standards such as IEEE 802.16e mobile WiMAX and 3GPP LTE, LLR values from each transmit antenna need not to be generated simultaneously. Therefore, LLR values are generated sequentially by column-switching in IPM and the hardware blocks are fully shared to reduce the complexity in the proposed architecture.

TABLE II. ALGORITHMIC STEPS FOR THE PROPOSED 2X2 MIMO SYMBOL DETECTOR

STEP	BLOCK	OPERATION		
1	INPUT	$\mathbf{H}=\begin{pmatrix} h_{11} & h_{21} \\ h_{12} & h_{22} \end{pmatrix},\ \mathbf{y}=\begin{pmatrix} y_1 \\ y_2 \end{pmatrix}$		
2	IPM	Input of PCM, **a**, **b**, **c**, **d**, and **e** is set as depicted in Table **III**.		
3	PCM	$p_1=\mathbf{a}^H\mathbf{b}\ ,\ p_2=\mathbf{c}^H\mathbf{d}\ ,\ p_3=\lVert\mathbf{e}\rVert^2$		
4	X2CCM	Spatial Multiplexing (SM) Mode	Spatial Diversity (SD) Mode	
		$x_2(c_m)=\mathbf{Q}\left(p_1-p_2c_m,\ p_3\right),\left(m=\mathbf{1},\ \mathbf{2},\ \ldots\ ,C\right)$	DVCM	The DVCM calculates the CSI and decision variables by using p_1, p_2 and p_3.
5	EDCM	$e_m=\lVert\mathbf{y}-\mathbf{h}_1c_m-\mathbf{h}_2x_2(c_m)\rVert^2$		
6	2DLCM	LLR = *min*(bit 0 group) – *min*(bit 1 group)	1DLCM	Simplified demapping scheme in [14] is applied.
7	QM	The QM quantizes the LLR values in 8 bit.		

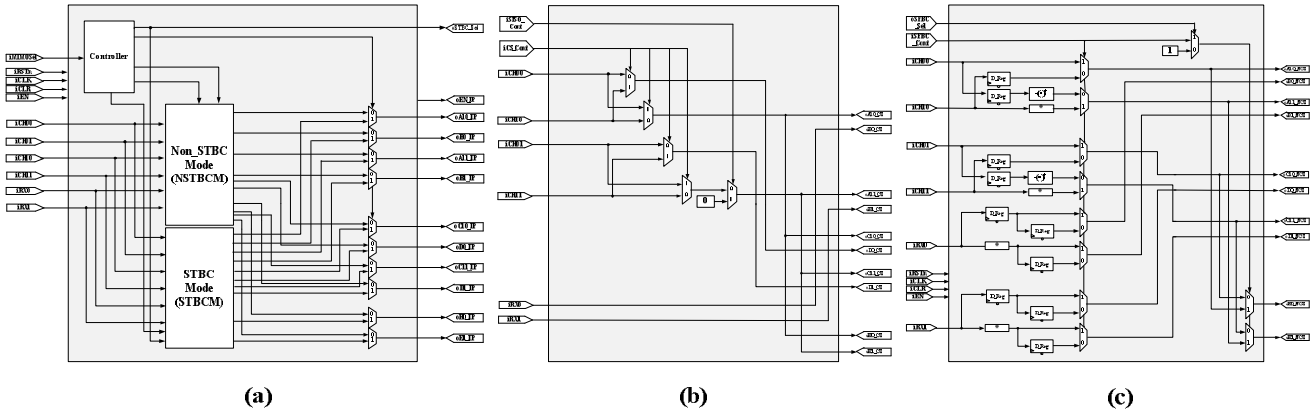

Figure 3. Block diagram of (a) IPM, (b) NSTBCM, and (c) STBCM

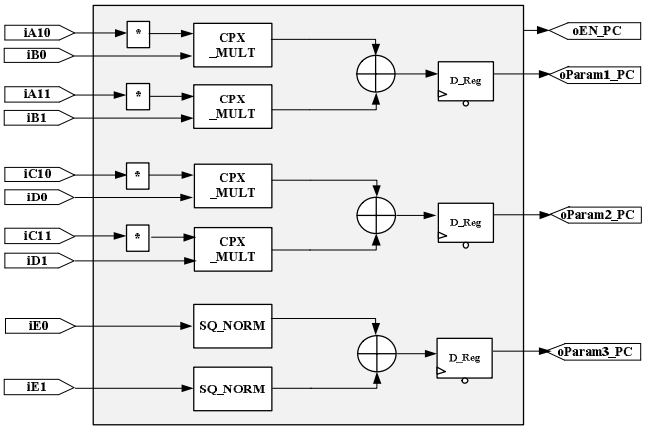

Figure 4. Block diagram of PCM

B. Parameter Calculation Module (PCM)

As shown in Fig. 4, PCM calculates the parameters, p_1, p_2 and p_3, which are the commonly required operations for both SD and SM modes. In case of SD mode, p_1 and p_2 are used for calculating the decision variables in DVCM and p_3 is utilized as the channel state information (CSI). In case of SM mode, all the parameters are mapped to the input data of X2CCM.

C. X2C Calculation Module (X2CCM)

As shown in Fig. 5, X2CCM consists of the polar-coordinate based multiplier (PBM) and slicer module (SCM). SCM makes the output, $x_2(c_m)$, $m=1,2,\cdots,C$, and is implemented without division operations through the scaled-constellation as in (5).

$$x_2(c_m)=\mathbf{Q}\left(\frac{\mathbf{h}_2^H}{\|\mathbf{h}_2\|^2}\left[\mathbf{y}-\mathbf{h}_1 c_m\right]\right)=\mathbf{Q}\left(p_1-p_2 c_m,\, p_3\right). \quad (5)$$

In order to calculate $p_2 c_m$ in (5), C number of complex multiplications should be performed in parallel, which makes it very difficult to design of X2CCM. For example, in case of 64QAM, 64 complex multiplications are required.

TABLE III. INPUT DATA MAPPING SCHEME OF PCM FOR MIMO MODE

MODE	$p_1=\mathbf{a}^H\mathbf{b}$		$p_2=\mathbf{c}^H\mathbf{d}$		$p_3=\|\mathbf{e}\|^2$	
SISO / SIMO	$\mathbf{a}=\begin{pmatrix}h_{11}\\0\end{pmatrix}\Big/\mathbf{a}=\begin{pmatrix}h_{11}\\h_{12}\end{pmatrix}\quad\mathbf{b}=\begin{pmatrix}y_{11}\\y_{12}\end{pmatrix}$		-		$\mathbf{e}=\mathbf{a}$	
MISO	1st clk.	2nd clk	-		1st clk.	2nd clk.
	$\mathbf{a}_1=\begin{pmatrix}h_{11}\\h_{21}^*\end{pmatrix}\mathbf{b}_1=\begin{pmatrix}y_{11}\\y_{12}^*\end{pmatrix}$	$\mathbf{a}_2=\begin{pmatrix}h_{21}\\-h_{11}^*\end{pmatrix}\mathbf{b}_2=\begin{pmatrix}y_{11}\\y_{12}^*\end{pmatrix}$			$\mathbf{e}_1=\mathbf{a}_1$	$\mathbf{e}_2=\mathbf{a}_2$
STBC & SFBC	1st clk.	2nd clk.	1st clk.	2nd clk.	1st clk.	2nd clk.
	$\mathbf{a}_1=\begin{pmatrix}h_{11}\\h_{21}^*\end{pmatrix}\mathbf{b}_1=\begin{pmatrix}y_{11}\\y_{12}^*\end{pmatrix}$	$\mathbf{a}_2=\begin{pmatrix}h_{21}\\-h_{11}^*\end{pmatrix}\mathbf{b}_2=\begin{pmatrix}y_{11}\\y_{12}^*\end{pmatrix}$	$\mathbf{c}_1=\begin{pmatrix}h_{12}\\h_{22}^*\end{pmatrix}\mathbf{d}_1=\begin{pmatrix}y_{21}\\y_{22}^*\end{pmatrix}$	$\mathbf{c}_2=\begin{pmatrix}h_{22}\\-h_{12}^*\end{pmatrix}\mathbf{d}_2=\begin{pmatrix}y_{21}\\y_{22}^*\end{pmatrix}$	$\mathbf{e}_1=\mathbf{a}_1$	$\mathbf{e}_2=\mathbf{a}_2$
SM	1~4 clk. (LLR1)	5~8 clk. (LLR2)	1~4 clk. (LLR1)	5~8 clk. (LLR2)	1~4 clk.	5~8 clk.
	$\mathbf{a}_1=\begin{pmatrix}h_{21}\\h_{22}\end{pmatrix}\mathbf{b}_1=\begin{pmatrix}y_1\\y_2\end{pmatrix}$	$\mathbf{a}_2=\begin{pmatrix}h_{11}\\h_{12}\end{pmatrix}\quad\mathbf{b}_2=\begin{pmatrix}y_1\\y_2\end{pmatrix}$	$\mathbf{c}_1=\begin{pmatrix}h_{21}\\h_{22}\end{pmatrix}\mathbf{d}_1=\begin{pmatrix}h_{11}\\h_{12}\end{pmatrix}$	$\mathbf{c}_2=\begin{pmatrix}h_{11}\\h_{12}\end{pmatrix}\mathbf{d}_2=\begin{pmatrix}h_{21}\\h_{22}\end{pmatrix}$	$\mathbf{e}_1=\mathbf{a}_1$	$\mathbf{e}_2=\mathbf{a}_2$

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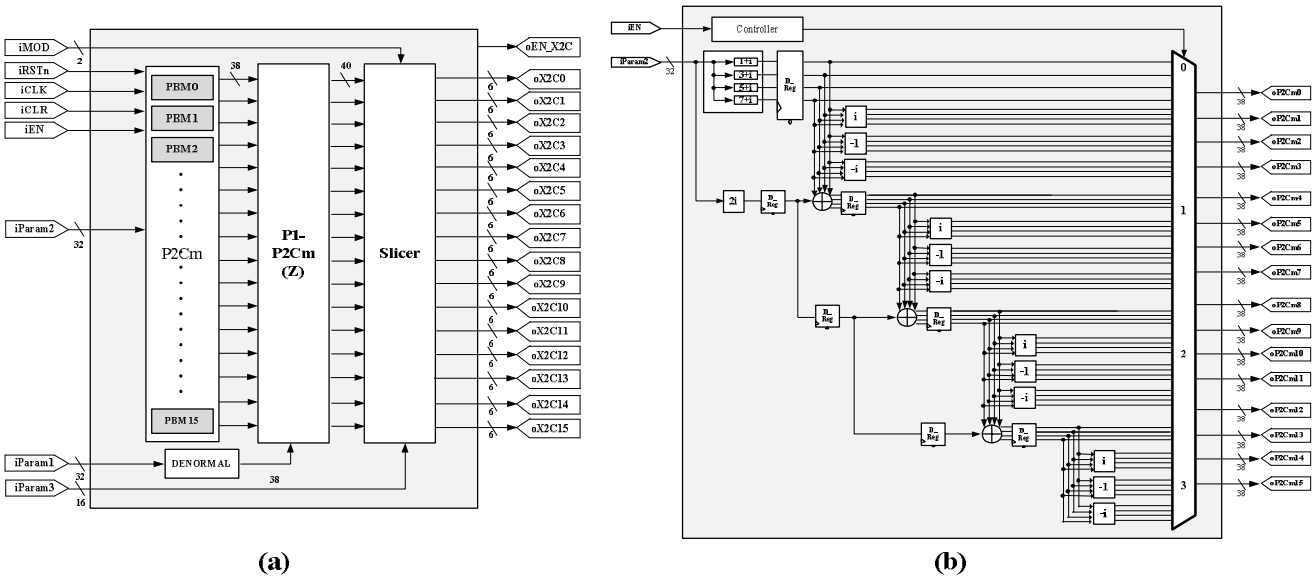

Figure 5. Block diagram of (a) X2CCM and (b) PBM

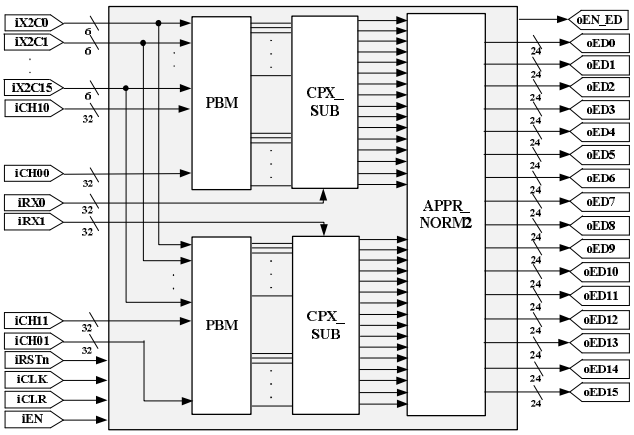

Figure 6. Block diagram of EDCM

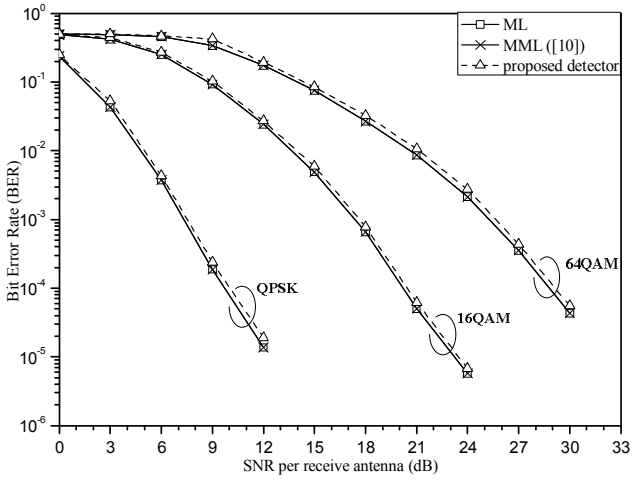

Figure 7. Performance evaluation results of the proposed symbol detector

In the proposed architecture, the complex multiplication is replaced by the PBM which can be simply implemented with sign-inverter, shifters and adders as in Fig. 5(b) because c_m in constellation is constant and symmetric. Especially, PBM is designed with 4-stage pipeline architecture to reduce the computational complexity by sharing the hardware resources. Although the throughput performance may be degraded, it is practically negligible because the throughput bottleneck of the baseband modem is mostly in the forward error correction (FEC) module such as turbo decoder. For example, when the proposed detector is applied to the mobile WiMAX baseband processor including turbo decoder with 6 iterations, it is verified from the timing analysis that 4-stage pipelining of PBM does not make any degradation of throughput performance.

D. ED Calculation Module (EDCM)

EDCM calculates the Euclidean distance, e_m, which is given by

$$e_m = \left\| \mathbf{y} - \mathbf{h}_1 c_m - \mathbf{h}_2 x_2(c_m) \right\|^2 . \quad (6)$$

As shown in Fig. 6, $\mathbf{h}_1 c_m$ and $\mathbf{h}_2 x_2(c_m)$ is computed by PBM, and norm calculation is approximated as in [15], which makes the negligible performance degradation as shown in the performance evaluation results of Fig. 7 for a Rayleigh fading channel with additive white Gaussian noise (AWGN). After calculating ED, log-likelihood ratio (LLR) values are computed from 1DLCM or 2DLCM, and the final quantized LLR value is generated by 8-bit QM for FEC module such as turbo decoder. The quantization is performed through the analysis for the distribution of the calculated LLR value from 1DLCM or 2DLCM.

V. IMPLEMNTATION RESULTS

The MIMO symbol detector supporting all MIMO modes with the proposed architecture was designed in HDL and synthesized to gate-level circuits using 0.13um CMOS standard cell library. Table IV depicts the logic synthesis results for 80MHz operating clock frequency of the proposed MIMO symbol detector, which shows that EDCM is the most complex block in the proposed detector.

Table V shows the comparison results of our design and the existing detectors. Even though the proposed detector can support all MIMO modes such as SD and SM, its complexity is rather reduced by 57% compared with that of [10]. Compared with the results in [16], the proposed detector has the similar complexity. However, it can support all MIMO modes and the optimal ML performance.

TABLE IV. LOGIC SYNTHESIS RESULTS OF THE PROPOSED MIMO SYMBOL DETECTOR

	Gate Count (K)	**Prop. (%)**
IPM	11.4	2.9
PCM	32.2	8.2
X2CCM	31.0	7.7
EDCM	255.8	64.5
1DLCM	4.2	1.2
2DLCM	28.0	7.1
QM	1.0	0.2
Etc.	*29.4*	*8.2*
Total	***393 K***	***100 %***

TABLE V. *COMPARISON RESULTS* OF THE PROPOSED DESIGN AND EXISTING DETECTORS

	[10]	**[16]**	**Proposed**
MIMO Configuration	SM Only	SM Only	SM & SD
Detection Algorithm	MML	LORD*	MML
Gate count	921 K	408 K	393 K

* LORD denotes Layered ORthogonal Lattice Detector, which supports near-ML performance.

VI. CONCLUSION

In this paper, we proposed an area-efficient hardware architecture for the MIMO symbol detector which can support all MIMO modes such as SD and SM. With the multi-stage pipelining, simplified multiplication based on polar-coordinate, and the approximation of norm operation, the complexity of the proposed detector is reduced by 57% compared with that of the conventional architecture. Since the recent wireless systems specify to support both SD and SM modes and need to be implemented with low-complexity and low-power consumption, the proposed MIMO symbol detector can be considered to be suitable for those systems.

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