Smart Noise–Linearity Breakdown in Homodyne Multi-Standard Radio Receivers

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Abstract—**This paper analyzes the noise–linearity breakdown in direct conversion multi-standard radio receivers embedding analog signal conditioning. The paper's main goal is to develop a systematic noise–linearity partitioning methodology to be used in splitting the multi-standard receiver noise and linearity budget between its high frequency (HF) part and its low frequency (LF) baseband part. To this aim, a new and efficient design methodology tailored towards multi-standard receivers, and based on manual analysis, is developed. By using the developed methodology, power saving is enabled in the HF part through changing the multi-standard receiver HF part noise and linearity performance with its RF front-end gain. While for the LF part, the analysis revealed the performance can be kept the same to allow power optimization through dedicated circuit design.**

Keywords-software defined radio; receiver electrical specifications; noise-linearity partitioning.

I. INTRODUCTION

The latest trends in wireless communications reveal standards tend to use multiple frequency plans, RF and IF bandwidths and different modulation schemes and techniques (e. g., IEEE 802.11n, IEEE 802.16e). On top of it, the wireless medium is packed with different standards. Thus, there is a strong need for reconfigurable hardware that can handle a diverse range of wireless signals, [1].

For a multi-standard receiver front-end the homodyne quadrature down-converter is the optimum choice, [2]. This has been validated through several circuit implementations in CMOS processes, [1, 3-5]. The multi-standard receiver front-end principle block schematic is shown in Fig. 1, redrawn from [1].

To mitigate the different frequency plans specific to a multi-standard implementation, the receiver is assumed to have multiple RF inputs and hence, multiple Low Noise Amplifiers (LNAs), [6]. Through the multiplexer, the wanted RF path is fed to the complex down-conversion mixer driven by a quadrature LO signal having the same frequency with the RF carrier. These blocks represent the receiver's High Frequency (HF) part. Following the mixer, the receiver Low Frequency (LF) part is comprised by the analog signal
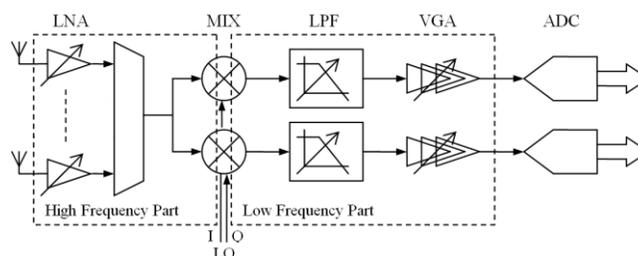

Figure 1. Quadrature homodyne multi-standard receiver block schematic, [1].

conditioning blocks: the Low Pass Filter (LPF) and the Variable Gain Amplifier (VGA).

This paper analyzes the noise–linearity breakdown in direct conversion multi-standard radio receivers embedding analog signal calibration. The paper introduces a new design methodology, stemming from a first order system level analysis based on manual analysis that enables a systematic approach of the noise–linearity partitioning that splits the multi-standard receiver noise and linearity budget between its HF and LF parts.

To this aim, firstly, Section II presents the need for smart gain partitioning in multi-standard wireless receivers. Secondly, Section III presents the smart noise partitioning strategy for multi-standard homodyne receivers based on the key tradeoff between the receiver HF part power consumption and its LF part area. In Section IV, the smart linearity partitioning strategy is revealed to complete the receiver electrical specifications breakdown. Finally, Section V wraps up the paper by presenting the conclusions.

II. THE NEED FOR SMART GAIN PARTITIONING

The wireless environment is an extreme one with respect to the signal reception. Generally, *three* generic receive scenarios are possible, as derived from the analysis in [7].

First of all, the received signal is very weak. In this case, the receiver noise performance is critical.

Secondly, the received signal is weak and surrounded by blockers and interferers, as specified by the receiver blockers diagram.
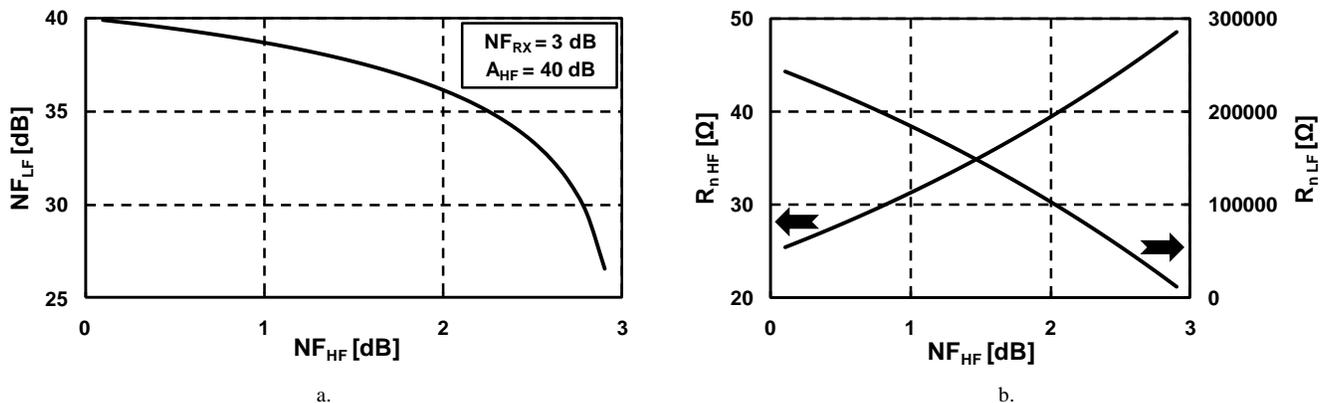
Figure 2.   a. NF_{LF} and b. $R_{n\,HF}$ and $R_{n\,LF}$ vs. NF_{HF}
($NF_{RX} = 3$ dB and $A_{HF} = 40$ dB)

In [8], a generic receiver blockers diagram has been introduced to allow mapping of all blockers and interferers of the envisaged standards. Under these conditions, the proper signal demodulation is constraint by both the receiver's noise and linearity performance.

Thirdly, the received signal is strong, and, thus, a high linearity is required from the receiver.

Hence, in order to mitigate all the received scenarios, the authors introduce in [7] the smart gain partitioning strategy tailored towards multi-standard radio receivers. Basically, the smart gain partitioning foresees (i) the receiver gain is programmable depending on the input signal level and is split in between its HF and LF part (i. e., between the LNA and the VGA) and (ii) the receiver noise and linearity performance (i. e., NF_{RX} and $IIP3_{RX}$) adjust with its HF part gain, A_{HF}.

In [7], *four* gain settings are foreseen for A_{HF} to increase the receiver robustness to blockers and interferers. The maximum receiver gain, $A_{HF\,max}$, is limited to 40 dB due to linearity reasons. The chosen gain step is 12 dB. Thus, the receiver will have *four* different NF_{RX} and $IIP3_{RX}$, depending on the A_{HF} gain settings (i. e., 4, 16, 28 and 40 dB).

Given the derivation of the key electrical specifications for a multi-standard radio receiver from [6], it resulted (i) the minimum receiver NF_{RX} is 3 dB (i. e., at maximum receiver gain, when the signal is at the receiver sensitivity level), while (ii) the maximum $IIP3_{RX}$ is +12 dBm (i. e., at minimum receiver gain, when the received signal is at its maximum level).

Further on in this paper, we are accounting a degradation of 1 dB / dB with A_{HF} gain change of both NF_{RX} and $IIP3_{RX}$.

III.   NOISE PARTITIONING STRATEGY

The overall receiver noise budget, represented by the receiver NF, NF_{RX}, is partitioned between the receiver LF and HF parts.

According to Friis equation the receiver global NF, NF_{RX}, can be calculated from the individual contributions of HF and LF parts:

$$NF_{RX} = 10\log\left(F_{HF} + \frac{F_{LF} - 1}{A_{HF}^2}\right), \qquad (1)$$

where F_{HF}, respectively F_{LF}, represent the noise factors of the HF part, respectively LF part, and $A_{HF} = A_{LNA} \cdot A_{MIX}$ is the receiver's HF front-end gain and it is equal to the product between the LNA gain, A_{LNA}, and the mixer gain, A_{MIX}.

Equation (1) shows that the LF part noise contribution is reduced by the RF front-end gain. Thus, knowing $NF_{HF} = 10\lg(F_{HF})$, the LF part noise figure, NF_{LF}, results as:

$$NF_{LF} = 10\log\left[1 + A_{HF}^2\left(10^{NF_{RX}/10} - 10^{NF_{HF}/10}\right)\right], \quad (2)$$

Both, the receiver HF and LF parts noise figures can be expressed as a function of their equivalent noise resistance, [1]:

$$\begin{cases} NF_{HF} = 10\log\left(1 + \dfrac{4R_{n\,HF}}{R_S}\right) \\[2mm] NF_{LF} = 10\log\left(1 + \dfrac{4R_{n\,LF}}{R_S}\right) \end{cases} \qquad (3)$$

where $R_{n\,HF}$ is the receiver RF front-end equivalent noise resistance, $R_{n\,LF}$ is the receiver baseband chain equivalent noise resistance and R_S is the antenna's resistance.

The noise partitioning is most critical when the receiver input signal is at its lowest value. Hence, A_{HF} is at its highest value $A_{HF\,max} = 40$ dB to keep $NF_{RX} = 3$ dB. For this case, Fig. 2 plots the NF_{LF}, $R_{n\,HF}$ and $R_{n\,LF}$ versus NF_{HF}.
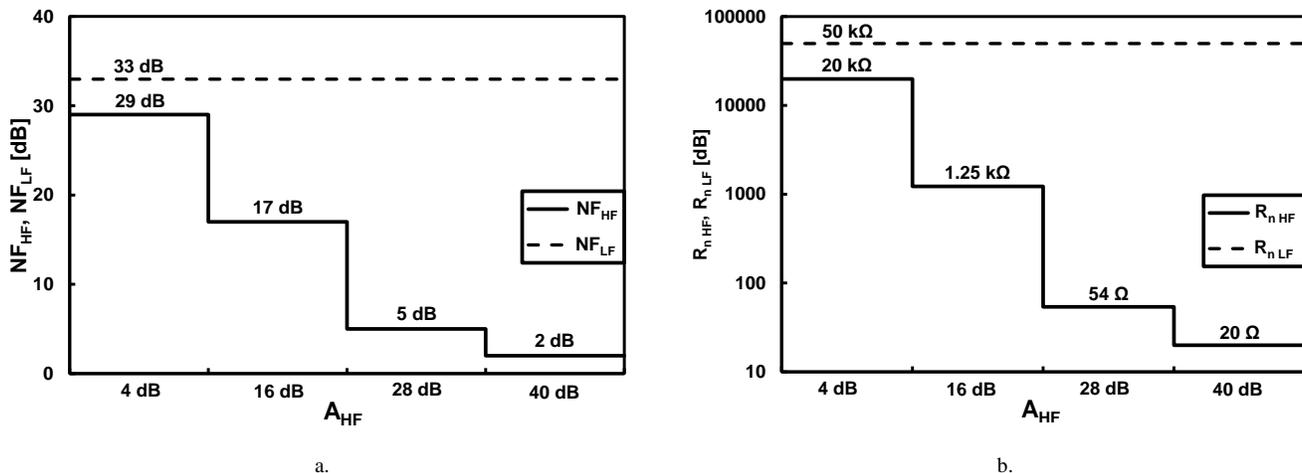
Figure 3.   a. NF_{HF} and NF_{LF} vs. A_{HF} and b. $R_{n\,HF}$ and $R_{n\,LF}$ vs. A_{HF}

The $R_{n\,HF}$, respectively $R_{n\,LF}$, calculated by (3) and shown in Fig. 2, represent the link between the receiver HF part power consumption, respectively LF part area, and its noise performance. Because of the large $A_{HF\,max}$, $R_{n\,LF}$ is much larger than $R_{n\,HF}$ (i. e., a few orders in magnitude), as shown in Fig. 2.b. Hence, the receiver HF part consumes more power than its LF part to achieve the same noise when referred at the receiver input.

Therefore, in order to reduce the receiver power consumption, the smart noise partitioning allows the receiver HF part to contribute more to the overall NF_{RX}. This translates to choosing a larger $R_{n\,HF}$, while allowing a bit smaller $R_{n\,LF}$. But, a smaller $R_{n\,LF}$ translates to a larger receiver area, as larger capacitances must be chosen to keep the same IF bandwidth, [1, 9].

Therefore the plot from is Fig. 2.b shows the key trade-off that shapes the noise partitioning: the trade-off between the receiver power consumption, represented by $R_{n\,HF}$, and its area, set by $R_{n\,LF}$.

Hence, in the case where the minimum receiver NF is required, NF_{HF} is accounting 2 dB, while the baseband chain and the ADC, share the remaining 1 dB from the 3 dB global NF_{RX}. This translates to a NF_{LF} of about 33 dB.

As mentioned, for the other receiver gain settings, the gain partitioning foresees the NF_{RX} reduction at a rate of 1 dB/dB with the A_{HF} decrease. The smart noise partitioning of the noise budget between NF_{HF} and NF_{LF}, accounts the degradation of only NF_{HF}, while keeping the same NF_{LF}. This potentially allows power saving in the front-end RF part, since its noise requirements are relaxed with the A_{HF} decrease. While for the baseband part the same NF_{LF} is foreseen regardless of the RF front-end gain setting, since power reduction would affect the LF part building blocks linearity.

Thus, the baseband blocks design is simplified and their power optimization is enabled though dedicated designs (e.

g., by using low power optimized fully differential amplifiers as the building brick of all baseband blocks, [10]).

Fig. 3.a plots the NF_{HF} and NF_{LF} for versus the A_{HF} gain settings. Equivalently, by reverting (2), and knowing NF_{HF} and NF_{LF}, both $R_{n\,HF}$ and $R_{n\,LF}$ can be calculated. Fig. 3.b reveals $R_{n\,HF}$ and $R_{n\,LF}$ for the four A_{HF} settings.

IV.   LINEARITY PARITITIONING STRATEGY

The linearity partitioning strategy tackles the receiver overall $IIP3$, $IIP3_{RX}$, budget split between its HF and LF parts. Hence, it calculates $IIP3_{RX}$ as a function of the RF front-end $IIP3$, $IIP3_{HF}$, and of the baseband chain $IIP3$, $IIP3_{LF}$:

$$\frac{1}{IIP3_{RX}^2} = \frac{1}{IIP3_{HF}^2} + \frac{A_{HF}^2}{IIP3_{LF}^2} \tag{4}$$

Linearity constraints are important at high signal levels, when A_{HF} is small. For this case (i. e., $A_{HF}=4$ dB), by using eq. (4), Fig. 4.a plots $IIP3_{LF}$ vs. $IIP3_{HF}$ for $IIP3_{RX}=12$ dBm.

As expected, the plot reveals that for a more linear RF front-end we can tolerate more non-linearity from the LF chain. But, given the high operation frequency, a more linear RF front-end burns more power to achieve the same linearity when compared with the LF part blocks. Moreover given the low baseband signal bandwidth (i. e., maximum 20 MHz for W-LAN 802.11n amongst envisaged standards), the LF part circuits can very efficiently make use of negative feedback based on low power feedback amplifiers to achieve a high linearity (e. g., [9, 11, 12]).

Hence, the smart linearity partitioning accounts equal contributions from the receiver HF part and from its LF part when referred to the input (i. e., $IIP3_{LF}/A_{HF}$). Thus, it results:

$$IIP3_{HF} = IIP3_{LF}/A_{HF} = IIP3_{RX} \cdot \sqrt{2} \tag{5}$$
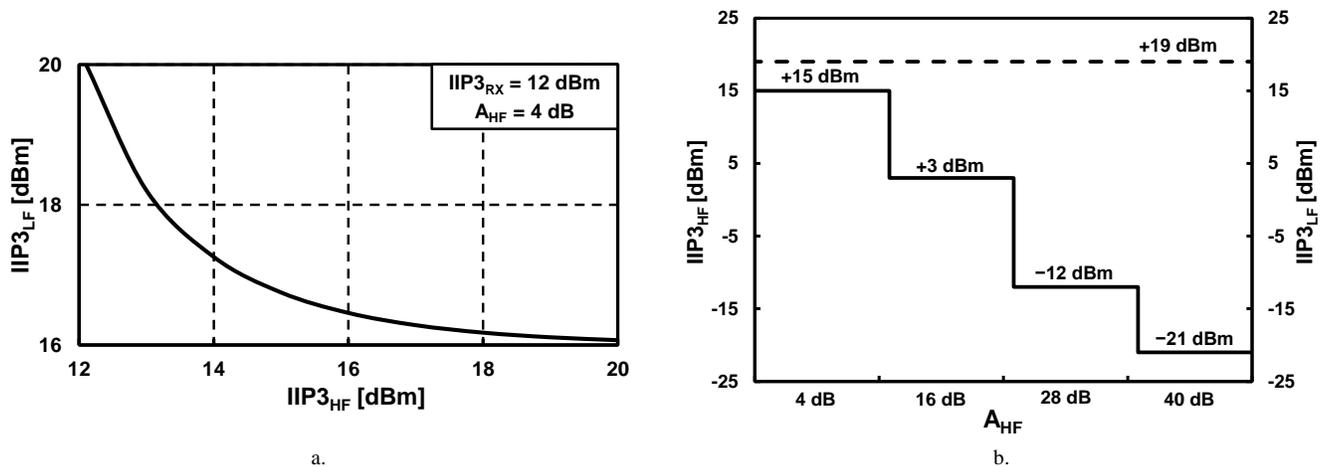
Figure 4. a. $IIP3_{HF}$ vs. $IIP3_{LF}$ and b. $IIP3_{HF}$ and $IIP3_{LF}$ vs. A_{HF}.

The smart gain partitioning foresees the $IIP3_{RX}$ reduction at a rate of 1 dB/dB with the A_{HF} increase. Similarly to the noise partitioning, the smart linearity partitioning allows the degradation of only the RF front-end linearity performance (i. e., $IIP3_{HF}$). Hence, given the smart linearity partitioning from eq. (5), Fig. 4.b reveals $IIP3_{HF}$ and $IIP3_{LF}$ for the four A_{HF} settings. And again the same conclusion arises: since the LF part linearity performance is the same regardless of A_{HF} (i. e., $IIP3_{LF} = +19$ dBm), the LF part blocks design is simplified and it can optimized by designing dedicated building blocks.

V. CONCLUSIONS

This paper analyzed the noise–linearity breakdown between the HF part and LF part of a direct conversion multi-standard radio receivers embedding analog signal conditioning. In order to enable a systematic approach of the noise–linearity partitioning, the paper introduces a new design methodology tailored towards multi-standard receivers, stemming from a first order system level analysis based on manual analysis.

By using the developed methodology, power saving is enabled in the HF part through changing the multi-standard receiver HF part noise and linearity performance with its RF front-end gain. While for the LF part, the analysis revealed the performance can be kept the same to allow power optimization through dedicated circuit design.

The paper emphasizes the general characteristic of the proposed smart noise–linearity partitioning methodology, as it fits best a true re-configurable multi-standard receiver implementation.

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REFERENCES

[1] S. Spiridon, *Analysis and Design of Monolithic CMOS Sofware Defined Radio Receivers*, PhD Thesis, Ed. Tehnica, 2011.

[2] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2nd Ed., 2004, pp. 710-713.

[3] J. Craninckx et. al, "A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13μm CMOS," *Digest of Technical Papers of the International Solid State Circuit Conference*, ISSCC 2007, pp. 346-347 and 607.

[4] V. Giannini et. al, "A 2mm² 0.1-to-5GHz SDR Receiver in 45nm Digital CMOS," *Digest of Technical Papers of the International Solid State Circuit Conference*, ISSCC 2009, pp. 408-409.

[5] M. Ingels et. al, A 5mm² 40nm LP CMOS 0.1-to-3GHz multistandard transceiver, *Digest of Technical Papers of the International Solid State Circuit Conference*, ISSCC 2010, pp. 458-459.

[6] S. Spiridon et. al, "Deriving the key electrical specifications for a multi-standard radio receiver," *Proceedings of the First International Conference on Advances in Cognitive Radio*, COCORA 2011, April 2011, pp. 60-63.

[7] S. Spiridon et. al, "Smart gain partitioning for noise – linearity trade-off optimization in multi-standard radio receivers," *Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems*, MIXDES 2011, June 2011, pp. 466-469.

[8] S. Spiridon, C. Dan, M. Bodea, "Filter partitioning optimum strategy in homodyne multi-standard radio receivers," *Proceedings of the 7th Conference on Ph.D. Research in Microelectronics and Electronics*, PRIME 2011, July 2011, pp.9-13.

[9] S. Spiridon, F. Op't Eynde, "Low power CMOS fully differential programmable low pass filter," *Proceedings of the 10th International Conference on Optimization Of Electrical And Electronic Equipment*, OPTIM 2006, May 2006, pp. 21-25.

[10] S. Spiridon, F. Op't Eynde, "An optimized opamp topology for the low frequency part of a direct conversion multi-standard radio transceiver," *Proceedings of the First International Symposium on Electrical and Electronics Engineering*, ISEEE 2006, October 2006, pp. 11-16.

[11] S. Spiridon, F. Op't Eynde, "Low power CMOS fully differential variable-gain amplifier," *Proceedings of the 28th Annual International Semiconductor Conference,* CAS 2005, October 2005, vol. 2, pp. 383-386.

[12] V. Giannini et. al, "Flexible baseband analog circuits for software-defined radio front-ends," *Journal of Solid State Circuits*, vol. 42, no. 7, July 2007, pp. 1501-1512.