Deriving the Key Electrical Specifications for a Multi-Standard Radio Receiver

Silvian Spiridon, Florentina Spiridon, Claudius Dan and Mircea Bodea
Faculty of Electronics, Telecommunications and Information Technology
"POLITEHNICA" University of Bucharest, Romania
e-mail: silvian.spiridon@gmail.com, florentina.spiridon@gmail.com, claudius.dan@gmail.com, mirceabodea@yahoo.com

***Abstract*—This paper focuses on finding the key electrical specifications for a multi-standard radio receiver compatible with the major commercial wireless standards. By developing a standard independent methodology, the paper addresses systematically the large amount of information comprised in the envisaged standards. Based on the systematic approach, the multi-standard receiver main electrical requirements are defined and their values determined. The presented results constitute the starting point in building a multi-standard wireless receiver.**

Keywords-software defined radio; receiver electrical specifications.

I. INTRODUCTION

At the beginning of the mobile Internet age, it becomes clear there is a strong need of mobile equipment able to maximize its wireless connectivity.

There are several reasons that make extremely attractive the usage of multi-standard radio transceivers to enable the wireless interoperation of such mobile equipment.

First of all, a multi-standard solution is efficient as only one design is required to handle the mobile device wireless communication. Thus the number of different dedicated ICs or IP blocks inside a large SoC is reduced. This simplifies the overall communication platform integration. Secondly, since only one design is required to cover for the all the targeted wireless standards all cost related to the IP development and testing are minimized.

The ideal multi-standard receiver was proposed by Mitola in [1]. The Software Defined Radio Receiver (SDRR) shown in Fig. 1.a is the optimal choice from system level perspective, as it comprises only an ADC. In reality, due to practical implementation constrains, a multi-standard receiver requires a signal conditioning path in between the antenna and the ADC. The SDRR concept shown in Fig. 1.b relaxes the ADC specifications by ensuring for the wanted signal additional selectivity and amplification.

A possible SDRR implementation is shown in Fig. 1.c, [2]. The receiver is based on the direct conversion architecture, the optimum choice for a multi-standard enactment, [3]. Also, the homodyne receiver is embedding a full signal conditioning path. The received signal is amplified by the Low Noise Amplifier (LNA) and then downconverted to baseband.

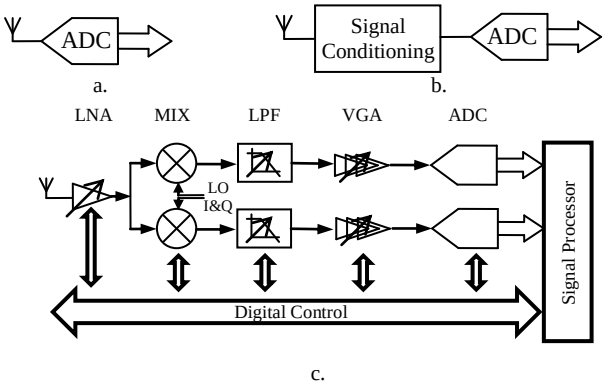

Figure 1. a. Mitola SDRR Concept, b. SDRR embeding signal conditioning and c. SDRR with complete analog signal conditioning

The blockers and interferers are removed by the channel selection Low Pass Filter (LPF) and then the Variable Gain Amplifier (VGA) boosts the useful signal to optimally load the Analog to Digital Converter (ADC).

Through digital control the SDRR blocks main characteristics (e. g., bandwidth, noise, and linearity) can be changed dynamically depending on the particular standard requirements or even on the particular communication burst necessities.

The paper's main goal is to identify the key electrical requirements and their values for a SDRR based on the Fig. 1.c concept targeting compatibility to the major commercial wireless standards listed in Table I. Based on a systematic approach, the paper introduces a standard independent methodology for evaluating the SDRR performance.

Section II defines the SDRR receiver sensitivity, NF and gain requirements, while Section III analyses the blocker and interferers impact on the SDRR linearity requirements. Section IV concludes the paper.

II. DEFINING THE SDR SENSITIVITY, NOISE FIGURE AND GAIN REQUIREMENTS

A. Sensitivity and Noise Figure

One of the most important parameters of a wireless receiver is its sensitivity, S_{RX}. The sensitivity is defined as the minimum input signal the receiver must be able to demodulate within a specified Bit Error Rate (*BER*).

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TABLE I. TARGETED MAJOR COMMERCIAL WIRELESS STANDARDS KEY SPECIFICATIONS

Wireless Standard		Frequency Plan [MHz]		Modulation Type	SNR_0 [dB]	RF Signal BW / Channel Spacing [MHz]	Specified Sensitivity [dBm]	Sensitivity @ NF_{RX} = 3 dB [dBm]
		Downlink	*Uplink*					
GSM, [4]	GSM 850	869 ÷ 894.8	824 … 849.8	GMSK	9	0.2	–102	–109
	GSM 900	935 ÷ 960	890 … 915					
	DCS 1800	1805 ÷ 1880	1710 … 1785					
	PCS 1900	1930 ÷ 1990	1850 … 1910					
UMTS, [5]	I	2110 ÷ 2170	1920 ÷ 1980	QPSK	−18 (@ 12.2kbps)	3.84 / 5	–117	–123
	II	1930 ÷ 1990	1850 ÷ 1910					
	III	1805 ÷ 1880	1710 ÷ 1785					
Bluetooth, [6]		2402 ÷ 2480		GFSK	16	1	–70	–94
DECT, [7]		1880 ÷ 1980, 2010 ÷ 2035		GFSK	13	1.2 / 1.736	–83	–97
WLAN IEEE 802.11b (DSSS), [8]	1 / 2 Mbit/s	2400 ÷ 2485		DBPSK / DQPSK	−4 / −2	14 / 5	–80	–104 / –102
	5.5 / 11Mbit/s			CCK	9 / 11		–76	–91 / –89
WLAN IEEE 802.11a,g (OFDM), [8]	6 / 9 Mbit/s	5150 ÷ 5350 & 5725 ÷ 5825 (a) 2400 ÷ 2485 (g)		BPSK	4 / 5	16.6 / 20	–82 / –81	–95 / –94
	12 / 18 Mbit/s			QPSK	7 / 9		–79 / –77	–92 / –90
	24 / 36 Mbit/s			16QAM	12 / 16		–74 / –70	–87 / –83
	48 / 54 Mbit/s			64QAM	20 / 21		–66 / –65	–79 / –78

Thus, the Signal-to-Noise Ratio at the RX output, SNR_{out}, has to be above a minimum value SNR_0. SNR_0 value is set by the received useful signal modulation characteristics and it incorporates the digital demodulator non-idealities.

Based on the analysis presented in [9], the SNR_0 as a function of the *BER* has been determined for the basic modulation schemes. Table I notes the targeted standards signal modulation and the corresponding SNR_0 values. The SNR_0 has a negative value for UMTS and WLAN 802-11 standards, as it accounts the processing gain specific to direct sequence spread spectrum systems, [10].

The usage of SNR_0 facilitates the finding of the multi-standard receiver key electrical parameters by enabling a standard independent approach.

As each standard specifies a sensitivity level, given the useful signal RF bandwidth, BW_{RF}, the receiver NF, NF_{RX}, is calculated as:

$$NF_{RX} \le S_{RX} - 10\log BW_{RF} - SNR_0 - N_0, \qquad (1)$$

where $N_0 = k_B T = -174$ dBm/Hz represents the noise power spectral density at the antenna output for T = 290 °K.

In practice, an overhead to SNR_0 should be considered in (1), since the overall receiver SNR is degraded by multiple factors, not only by noise (e. g., imperfect impedance matching, multipath channel).

The receiver NF specifications for all the wireless standards can be calculated with (1) by accounting the specified sensitivity levels from Table I.

A NF as the one derived by (1) can be obtained at the expense of larger power consumption of thy receiver.

In order to maximize the link budget, most commercially available dedicated receivers push their sensitivity level towards smaller and smaller values by decreasing NF_{RX}.

Hence, a true re-configurable multi-standard solution must embed a receiver with a small NF (typically < 3 dB) in order to be able to achieve a low enough sensitivity for all the targeted standards. Table I also comprises the required sensitivity levels, assuming NF_{RX} = 3 dB, for all the envisaged wireless standards.

B. Maximum gain requirements

In general, the receiver signal conditioning path gain is constraint by the received signal strength.

Any wireless receiver with an analog signal conditioning path embeds at least one variable gain block (for example VGA in Fig. 1.c). Thus, for each communication burst an Automated Gain Control loop (AGC) measures the Receiver Signal Strength Indicator (RSSI) and changes the receiver gain accordingly, in order to avoid the ADC overloading and to optimally load it.

The receiver maximum gain requirements are constraint by the ADC full scale level, FS_{ADC}, and the specified receiver sensitivity.

In order to optimally load the ADC, the receiver signal conditioning path maximum gain, G_{RX}, is given by:

$$G_{RX} = \frac{k \cdot FS_{ADC}}{S_{RX}}, \qquad (2)$$

where $k < 1$ accounts the head room taken to avoid the ADC overloading.

TABLE II. THE MULTI-STANDARD RECEIVER MAXIMUM GAIN REQUIREMENTS

Wireless Standard		G_{RX} [dB]
GSM		115
UMTS		129
Bluetooth		100
DECT		103
WLAN IEEE 802.11 b,g (DSSS)	1 / 2 / 5.5 / 11 Mbit/s	110 / 108 / 97 / 95
WLAN IEEE 802.11 a,g (OFDM)	6 / 9 / 12 /18 24 /36 /48 /54 Mbit/s	101 / 100 / 98 / 96 93 / 89 / 85 / 84

For a multi-standard receiver embedding analog signal conditioning (see Fig. 1.c), k is set by the Variable Gain Amplifier (VGA) gain step (e. g., 6 dB, [11]). Equation (2) assumes all interferes and blockers have been totally filtered out before the ADC. This corresponds to the case of complete analog channel selection.

Table II presents the receiver signal conditioning path maximum gain requirement for all the envisaged standards calculated based on equation (2) for a 1 V FS ADC and for a receiver matched to 100 Ω with k = 0.9; the NF_{RX} of the receiver was assumed to be 3 dB. For direct sequence spread spectrum systems (e. g., WLAN 802.11b) the gain requirement is smaller, as in practice other signals will be present as well inside the received bandwidth.

Nonetheless, we can conclude, based on Table II data, that the low sensitivity levels of the targeted wireless standards require a large maximum gain for the multi-standard receiver.

III. BLOCKERS AND INTERFERERS IMPACT ON THE MULTI-STANDARD RECEIVER CHARACTERISTICS

Besides the useful signal, other interferers and blockers can be present at the antenna input. The list comprising all interferes and blockers under which influence the receiver must still be able to properly demodulate the wanted signal represents the receiver blocker diagram. For each wireless standard such a receiver blocker diagram is specified.

Based on the targeted standards blockers diagrams analysis it results there are two major issues due to blockers and interferes:

- the receiver output clipping, due to the large receiver gain requirements and to the large difference between the useful signal and the blocker levels (i. e., typically > +40 dBc);
- intermodulation distortions that fall in-band, due to the receiver not perfectly linear transfer characteristic.

The receiver output clipping can be handled by making the LNA and VGA blocks gain variable. Through

On the other hand intermodulation distortions are un-wanted products that potentially fall in-band and cannot be disseminated from the useful signal. Thus the wanted signal demodulation is affected due to the SNDR degradation. Further on the analysis presented in this Section focuses on finding the values for the Figures of Merit (FOMs) used in evaluating the radio receiver linearity performance: the $IIP2$ and $IIP3$.

A. Finding the SDR IIP2

While receiving the RF input power may change significantly because of the reception of unwanted blockers/interferers. Due to the receiver even order distortions, the received signal DC offset component will change. This *dynamic offset* effect upsets the received signal demodulation, especially if the envisaged modulation concentrates a large part of the symbol spectral power at low frequencies. This is the case for older standards like GSM, as the latest wireless standards use modulation schemes that do not carry information at low frequencies.

The figure of merit quantizing the analog front-end second order distortions is the second order intercept point, $IP2$. The SDRR input referred IP2, $IIP2_{RX}$, is given by, [12]:

$$iIP2_{\mathrm{RX}} = 2 \times P_{blocker} - P_{in} + SNR_0 , \quad (3)$$

where $P_{blocker}$ is the blocker level and P_{in} is the wanted signal level.

Based on the targeted standards analysis, it results the worst case scenario is met for the GSM standard that requires $IIP2_{RX}$ = +46 dBm, [2].

B. Finding the SDR IIP3

For most wireless receivers, given the fully differential circuit implementation, the dominant non-linear contribution comes from the third order coefficient of power series expansion of their transfer characteristic. The maximum in-band level of the third-order intermodulation product, P_{IM3}, must be smaller than the useful RF signal level with SNR_0:

$$P_{IM3} \le P_{in} - SNR_0 \quad (4)$$

In practice, a supplementary head room to SNR_0 should be considered, since the overall receiver SNR is degraded by multiple factors, not only by the down-converted spurs.

Given (4), the receiver IIP3, $IIP3_{RX}$, must meet the condition specified by the equation:

$$IIP3_{\mathrm{RX}} \ge P_{\mathrm{interferer}} + \frac{P_{\mathrm{interferer}} - P_{IM3}}{2} \quad (5)$$

where $P_{\mathrm{interferer}}$ is the power per interferer of two interferers that cause the in-band third order distortion.

A special case is represented by OFDM Signals. An OFDM signal comprises frequency orthogonal sub-carriers, [9]. Receiver non-linearity leads to formation of bogus signals in-band due to sub-carrier intermodulation. The figure of merit in evaluating the third order intermodulation products thus formed is the Composite Triple Beat (CTB).

As is pointed out in [13] the worst case for the CTB products level is found in the centre band of the OFDM signal spectrum:

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TABLE III. MULTI-STANDARD RECEIVER IIP3 REQUIREMENTS

Standard	Intermodulation conditions	RX IIP3[dBm]	
		Eq.	*Value*
GSM	$P_{interferer}$ @ −49 dBm, P_{in} @ −99 dBm	(5)	−19
UMTS	$P_{interferer}$ @ −46 dBm, P_{in} @ −114 dBm	(5)	−21
Bluetooth	$P_{interferer}$ @ −39 dBm, P_{in} @ −64 dBm	(5)	−18.5
DECT	$P_{interferer}$ @ −47 dBm, P_{in} @ −80 dBm	(5)	−24
WLAN IEEE 802.11b,g (DSSS)	$P_{interferer}$ @ −35 dBm, P_{in} @ −70 dBm CCK – 11 Mbit/s	(5)	−12
W-LAN IEEE 802.11g (OFDM @ 2.4 GHz)	Interferer intermodulation: $P_{interferer}$ @ Sensitivity, P_{in} @ +32…+15 dBc (6…54 Mbit/s)	(5)	−32
	Blocker intermodulation: $P_{blocker}$ @ −10 dBm, P_{in} @ −42 dBm, BPSK – 6 Mbit/s	(5)	+8.5
	Sub-carrier intermodulation: P_{in} @ −20 dBm, N = 52 carriers, 64QAM – 54 Mbit/s	(9)	+10
W-LAN IEEE 802.11a (OFDM @ 5 GHz)	Sub-carrier intermodulation: P_{in} @ −30 dBm, N = 52 carriers, 64QAM – 54 Mbit/s	(9)	+5

$$CTB[\text{dB}] \le -2\left(IIP3_{\text{RX}} - P_{in}\right) + 1.74, \quad (7)$$

where P_{in} is the OFDM signal power in all the carriers.

Hence, in order for the digital back-end to be able to still demodulate properly the wanted signal, the CTB level must be smaller than the useful RF signal level per carrier with SNR_0:

$$CTB \le P_{in} - 10\log N - SNR_0, \quad (8)$$

where N represents the number of OFDM sub-carriers.

In (8) SNR_0 represents the corresponding SNR headroom of the OFDM sub-carrier modulation.

Given (7) and (8), it results that in order to avoid destructive inter-carrier intermodulation, the $IIP3_{\text{RX}}$ must meet the following condition:

$$IIP3_{\text{RX}} \ge \frac{1}{2}\left(P_{in} + 10\log N + SNR_0 + 1.74\right) \quad (9)$$

Each wireless standard specifies a set of particular intermodulation conditions. Table III summarises the power per interferer of two interferers that cause the in-band distortion and the input signal power. By analysing all the targeted standards, the receiver *IIP*3 specifications were derived using (5) or (9) and noted in Table III. The large variations in the *IIP*3 requirements are a reflection of the extreme reception conditions specific to the wireless environment. In [12] it is shown a versatile receiver is able to mitigate all presented scenarios, by adjusted dynamically its linearity and noise performance with the received power.

IV. CONCLUSIONS AND FUTURE WORK

This paper conducted an analysis for finding the main requirements for a SDRR targeting compatibility with the major commercial wireless standards (see Table I).

Thanks to the standard independent systematic approach the presented analysis found the values for the key SDRR electrical specifications (i. e., NF_{RX}, $IIP2_{\text{RX}}$ and $IIP3_{\text{RX}}$) that ensure its compatibility with the envisaged standards.

Of course, a true SDRR has to be versatile and robust, such as it can adjust dynamically its performance (e. g., NF_{RX}, $IIP3_{\text{RX}}$) depending on the communication burst particularities. Nonetheless if a SDRR targets compatibility with the standards from Table I, it must meet the electrical specifications determined in this analysis.

So, the presented analysis constitutes the starting point in building the SDRR. Further on, the SDRR electrical specifications must be partitioned over its building blocks. The optimal specification partitioning must account the limitations due to the physical implementation (i. e., CMOS process) for each of the SDRR building blocks.

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