Design of Novel Integrated Data Acquisition System for Multi-Channel Sensing in Landing Gear

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***Abstract*— In this paper, it is intended to describe the design process, planning, and development of a new Data Logger System (DLS) that can be potentially used in acquiring sensor signals in the landing gear of aircraft. This paper is presenting the new concept and development process of the DLS that employs a novel low-power pulse mode circuit structure. It outlines the overview of the sensor acquisition system and manufacturing of the DLS housing to fit the partner's requirements. The conducted work is broken down into several phases, these include conceptual design, development, production, and testing.**

Keywords—data acquisition; low power; multi-channel sensing; landing gear.

I. INTRODUCTION

Timely and accurate detection of aircraft status signals such as the landing gear is a basic guarantee of its normal operation and also improves aircraft reliability and reduces potential risks through taking timely and effective measures [1]-[6].

The proposed DLS in this paper is adopting a novel data acquisition system to reduce overall system power consumption and provide an effective 32 multi-channel sensing capability that outputs signals with varying ranges. To accommodate the different parts of the DLS including power management and data processing, a modular housing design is being used to meet the requirements of a rigid system that can withstand the harsh environment in aircraft landing gear and provide flexible testing accessibility. The new design is addressing a major sensing data challenge in the aviation industry which required a reliable and sustainable system that runs effectively under severe environmental flying conditions. A new low-power strategy was adopted in our design based on power sampling for sensor array which allows the integration of additional sensors without complicating overall system development.

Section II is outlining the system design overview. The description of the new development will be presented in section IV. The structure design is given in section V, whereas the design verification and testing results are presented in section VI.

II. DESIGN OVERVIEW

The system design requirements obtained from the industry partner are summarized in Table I. The desired low average current could only be achieved by implementing a high-speed configuration that would complete all the action in a small fraction of the sampling period, remaining in sleep mode the rest of the time. This ratio (active/sleep) determines how much is comparatively high active mode consumption reduced to an acceptable low average.

That means, all the procedures (sampling, A/D conversion, and memory update) should be as short, as only possible compared to the sampling period. The description of the system, designed to meet these requirements follows.

To provide the shortest available sampling time, along with minimum power loss, no voltage regulator has been used to power the sensor circuitry (due to long power on/off time). The sensors are powered dynamically (with exponentially rising voltage); A high-speed comparator disconnects the sampling keys from the set of sampling capacitors when the sensor driving voltage achieves the threshold. It is assumed, that the response of the sensor is linear related to driving voltage. To avoid errors related to sensor output impedance, the signals from sensors are applied via buffer amplifiers as seen in the system diagram presented in Figure 1.

The maximum slew rate of sensor driving voltage is limited by the slew rate of buffering amps that could be as high as 2V/us. To avoid errors, related to the response time of the comparator, the driving voltage is also sampled, providing the possibility for further software correction.

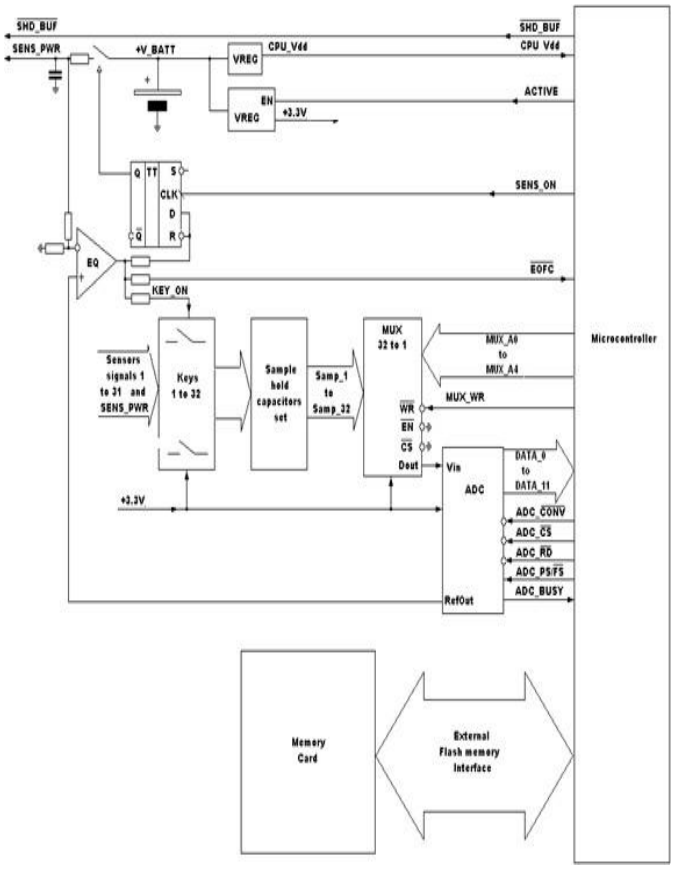

Figure. 1. Data acquisition system diagram

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TABLE I. TO BE DEVELOPED SYSTEM REQUIREMENTS

Number of channels	31
Sampling rate	128 Hz
Battery life (in operation mode)	1800 hrs.
Operation temperature range	-40 to +85 C
Overall dimensions	minimize
System weight	minimize
Typical consumption of the set of sensors	400 mA @ 5.0 V
Sensor type	Passive, resistive
Memory type and size	32 Gb, Flash
Data stored	Sensor reading and time stamp
External interface	USB

III. FEASIBILITY ANALYSIS AND SOLUTION APPROACH

Since the system is battery-powered and should provide long battery life, its power consumption becomes the determining factor for setting the system structure. The size and weight of the battery are limited as well, so the available battery of acceptable size is a pack of 4 cells (3.6 V, 2600 mAh, series-parallel), that is, 5200 mAh.

Typically, the capacity of the battery is limited by its discharge to approx. 5.5V is around 60-65% of the total and is actually 3120-3380 mAh. That yields, that the average current consumption should be within 1.73 -1.88 mA (for 1800 hours of operation). The desired low average current could only be achieved if the system is operated in pulse mode, completing all the necessary actions (A/D conversion, memory interfacing, etc.) in a small fraction of the sampling period, remaining in sleep the rest of the time.

The ratio of active/sleep mode of each element of the system will determine this element's average current, the sum of these, being the whole system average current, should be within the required limit. The second important point is, that the sensors used have a significantly different range of output signals (from volts to millivolts) on one hand and that the physical length of cables might be up to 1-1.5m. This makes the use of buffer amplifiers on sensors compulsory, to bring the signal levels to an acceptable range and avoid pickup on signal lines by providing low output impedance. More to the point, some types of sensors have differential output, while the common-mode voltage is high enough – that means, two types of buffering amplifiers are to be designed.

At the first stage of this work, however, to speed up the development, it was planned to test the system with comparatively simple non-inverting amplifiers and imitation of sensor signals from resistor dividers. After completing the conversion, the ADC is brought to the full-sleep mode by the microcontroller, bringing its consumption from 3.3mA in active mode down to 1uA.

IV. SYSTEM DESCRIPTION

This section will be presenting the design methodology and data processing control adopted in this work as illustrated by the following subsections.

A. Measurement Method

In order to provide the shortest possible sampling time, the sensors are powered dynamically (with exponentially rising voltage). During this time the keys remain closed, and sensor voltages are transferred to sample holding capacitors as shown in Figure 1.

It is assumed, that due to the passive and purely resistive nature of the sensors, their response is directly proportional to powering voltage. As soon as the powering voltage is applied to the inverting input of the high-speed comparator via the divider to achieve the threshold, the output of the comparator goes low, opening the keys, thus disconnecting sample holding capacitors from the signal lines, and at the same time switching off the sensor power by resetting the flip-flop.

Signal end of conversion (EOFC) is provided to MCU to indicate that the A/D conversion of the voltages present on sample holding capacitors may begin. To avoid any errors related to comparator delay time and threshold variation, the sensor power voltage is sampled in addition to sensor signals to provide the possibility to recalculate the obtained readings.

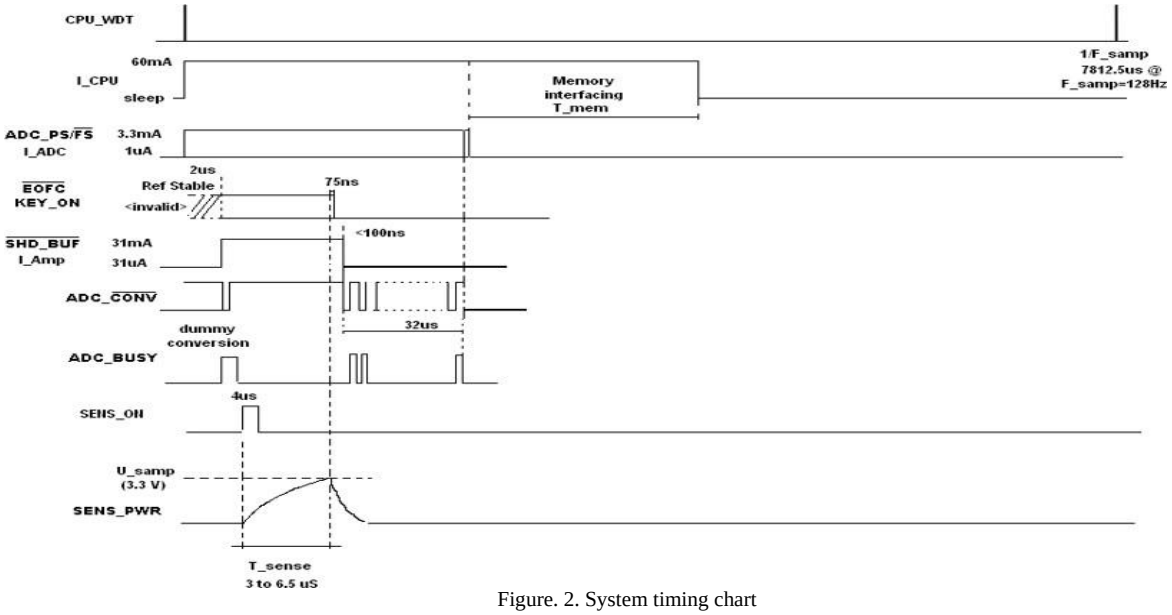

Figure. 2. System timing chart

B. *Considerations for A/D conversion*

Since the time for the conversion should be minimized, usage of ADC built-in to the microcontroller is inapplicable in principle, due to the very long conversion time. The (EOFC) signal is provided to MCU to indicate that the A/D conversion of the voltages present on sample holding capacitors may begin.

To achieve acceptable time from the structure depicted in Figure 1, The voltages, obtained on sampling capacitors, are applied via 32-to-1 multiplexor to a fast (800ns) ADC. The output code is a 12-bit parallel, which allows the controller to get one conversion result in one read instruction. That means, 32 words of data could be obtained in 32us. Additionally, the ADC used has its in-built clock source and stable reference voltage (used to provide threshold for comparator) as given in the system timing chart in Figure 2.

C. *Considerations for microcontroller choice*

The microcontroller should be able to accept the data from the ADC without delay and accept and generate all the necessary control signals without slowing down A/D conversion (that determines its minimum parallel bus speed). However, stricter requirement arises out of necessity to transfer the data to external memory. The data amount for a single transfer is 33 words of 16-bit (32 data and timestamp from RTC). This also requires choosing the fastest available interfacing to external memory.

V. STRUCTURAL DESIGN

The DLS is designed to be as compact as possible. The original concept, shown below in Figure 3, incorporates two separate modules, the Main module, and the Battery-Memory module.

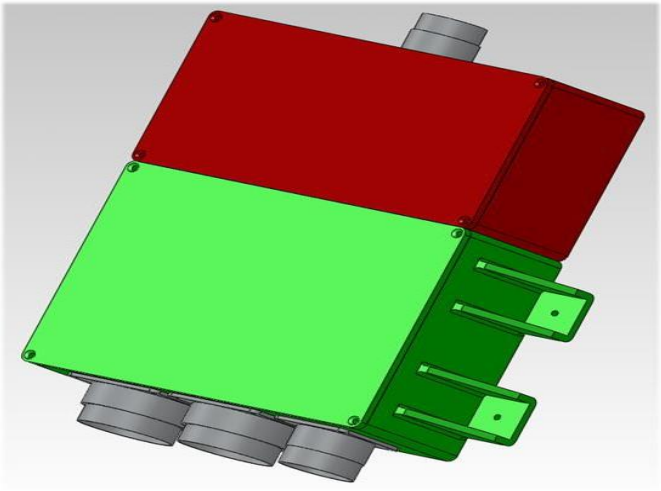

Figure. 3. DLS structural design

Now that the preliminary battery selection and media storage selection was performed and know the approximate volume requirements, a new concept design was proposed. The idea of the concept is that the battery cell can be removed for charging and the media storage also can be removed for data download as shown in Figure 4.

VI. DATA ACQUISITION VERIFICATION AND TESTING RESULTS

To verify the performance of both data logger systems a number of resistive potentiometers of various ranges were used as dummy sensors. From a design perspective, the main focus is to get the dynamic sensors' power circuitry working as desired and then extract the necessary ADC waveforms and match them with the device datasheet. Such practice was useful in debugging and testing to overcome many issues before getting the system prototype functioning as expected. Figure 5 shows some of the sensors' power and conversion signals, where obviously they are very comparable with the ones in Figure 2.

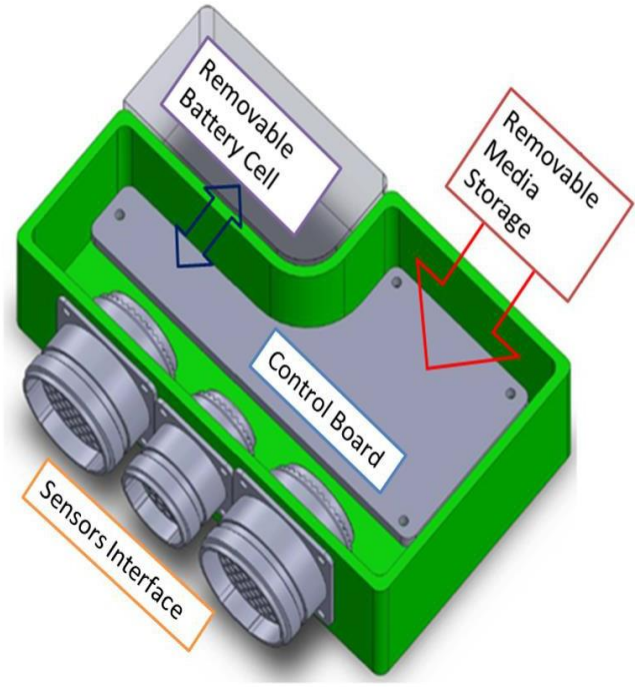

Figure. 4. Actual DLS design with power and data storage

Figure. 5. Dynamic power signals of DLS system-Power unit

A. *Integration with Industrial Sensor and Test Results*

The next phase of the testing process was to use a real industrial sensor interfaced to the Design system and use the developed Graphical Unser Interface (GUI) to monitor and record the multi-channel sensors' data acquisition via serial interface, these sensors are:

- Thermocouple temperature sensor
- Linear Displacement Potentiometer sensor (0-300mm)
- Pressure sensor (5 Ins max)
- Load cell strain gauge sensor

An interface board was manufactured with sensors mounted and all signals and power necessary connections are provided as shown in Figure 6.

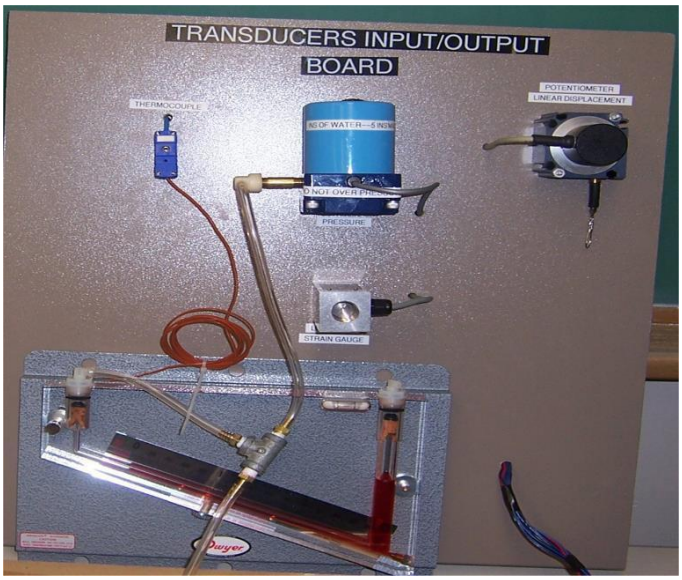

Figure. 6. Industrial sensor system setup using DLS

The DLS system performance was tested and verified using the sensors interface board and sensors readings were displayed by the developed GUI. Special single-ended input and differential amplifiers were designed for low-level sensor signals, like thermocouples and strain gauge sensors.

The enclosure of the DLS was designed using rapid prototyping. Figure 7 shows the side and top views of the designed enclosure where it can be seen the two main units are attached to fit both the system PCBs and battery.

The main functionality of the developed GUI is to show the incoming data from the DLS unit. The programming language used for programming this GUI was Visual Basic.NET from the Microsoft Visual Studio.NET package. The communication is done through COM ports and the data is sent in HEX format in a specific format (frame) which then is read in GUI and interpreted (parsed). The data is shown in a master graph for each channel as given in Figure 8 where each individual graph can be added and associated with specific given user options that can be set to modify the visual display of the GUI.

Figure. 7. DLS System enclosure

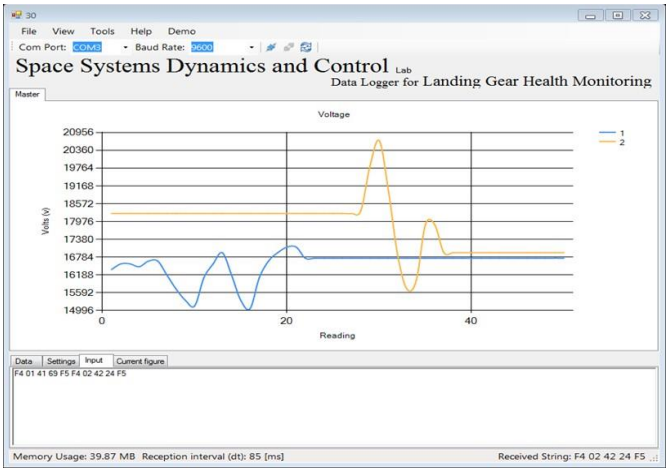

Figure. 8. Developed GUI to monitor the sensor readings recorded by DLS system.

B. *Measuring DLS power consumption*

The average current, consumption by the system is the sum of all quiescent currents of constantly powered elements (CPU in sleep mode (max.25uA), comparator (90uA max), flip-flop (2uA max) and two voltage regulators (2x35=70uA max)), and the average current of the components powered for a short time. Using the time chart, the following equation can be obtained :

$$I_{avg} = 187\text{uA} + \frac{I_{adc}T_{adc} + I_{amp1}T_{amp1+Isens} + (T_{adc} + T_{interf}) * I_{CPU}}{T_{sample}}$$

The equivalent time for sensor activity (under the condition of powering by constant 5V voltage) is less than 2us. (at 400mA current)

Then, at T_{sample} = 7812.5us,

$$I_{avg} = 187\text{uA} + \frac{3.3mA * 40us + 31mA * 4us + 400mA * 2us + (40us * T_{interf}) * 60mA}{7812.5\text{us}}$$

$$= 622\text{uA} + 60\text{mA}\frac{T_{interf}}{7812.5\text{us}}$$

That guarantees, that for interface time that is less than 143us, the average system current will remain within the limit. At the same time, if interfacing is fast enough, it is possible to reduce the speed of the system (for better accuracy and reliability).

The DLS current consumption was measured using in-circuit metering for two options, with and without pulse-mode operation concept as shown in Table II.

TABLE II. PEAK CURRENT CONSUMPTION MEASURING OF THE DLS

Operating option	Peak current draw (mA)
With Pulse-mode	0.714
Without Pulse-mode	2.26

VII. CONCLUSIONS

In this work, a novel sensor data logging system has been introduced. The system design is utilizing the pulse-mode dynamic power concept where output sensors are sampled through switched capacitors and then sensor power is turned off to start the ADC process. It was found the system power has been significantly reduced by more than (3:1) as can be seen in Table I to meet the requirements of low power consumption and extended battery lifetime.

The overall DLS design has been placed in a developed modular housing that incorporated the power source and storage components. A GUI has been developed to test the system output signals using industrial-rated sensors.

Planning for future work will be involving future testing on the sensing side and improving the power consumption performance. Also, the GUI is to be further developed to include more features on system-measured parameters.

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