A Novel High Speed Differential Ultra Low-Voltage CMOS Flip-Flop for High Speed Applications

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***Abstract*—In this paper we present a simple ultra low-voltage and high speed D flip-flop. The Flip-Flop may be used in any standard digital low-voltage CMOS applications. Furthermore, the ultra low-voltage Flip-Flop offers reduced data to output delay compared to conventional CMOS Flip-Flops. Different master latch configurations are presented and a differential symmetric ultra low-voltage Flip-Flop is presented. Simulated data using $HSpice$ and process parameters for $90nm$ CMOS are provided. Preliminary results show that the proposed Flip-Flop has a delay less than 20% compared to a conventional CMOS Flip-Flop.**

***Keywords*-CMOS, low-voltage, Flip-Flop, high-speed, Floating-Gate.**

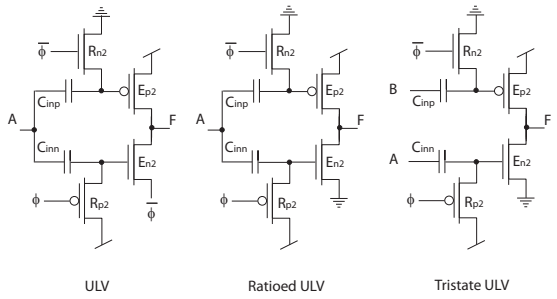

Figure 1. *The ULV logic.*

I. INTRODUCTION

The ever increasing problem associated with modern CMOS processes is the demand for digital CMOS gates operating at low supply voltages. The available supply voltage and threshold voltage is lowered as a consequence of the reduction in transistor length. When the supply voltage is decreased the speed of the logic circuits may be reduced due to reduced effective input voltage to the transistors. When the threshold voltage is reduced the off current running through transistors which are switched off will increase and thereby increase static power consumption and reduce noise margins. Voltage scaling reduces the active energy and unfortunately speed as well. Low voltage applications are often dominated by low speed and low energy requirements, typical battery-powered electronics. The optimal supply voltage for CMOS logic in terms of energy delay product (EDP) is close to the threshold voltage of the nMOS transistor V_{tn} for the actual process, assuming that the threshold voltage of the pMOS transistor V_{tp} is approximately equal to $-V_{tn}$ [1]. Several approaches to high speed and low voltage digital CMOS circuits have been presented [2][3][4].

Floating-gate (FG) CMOS gates have been proposed for ultra low-voltage (ULV) and low power (LP) logic [5]. However, in modern CMOS technologies there are significant gate leakages which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [5].

The ULV logic [6], [7] gates can be operated at a clock frequency more than 10 times than the maximum clock frequency of a similar complementary CMOS gate operating at the same supply voltage. For high clock frequencies, the switching energy consumed by the ULV gate will be reduced compared to a complementary gate.

In this paper we present an ultra low-voltage flip-flop (UFF) using ULV CMOS logic. The UFF offers a significant speed improvement compared to conventional sense amplifier FF (SAFF's) [8] hereafter called FF1. In section II a short introduction to ultra low-voltage logic is given. The simple UFF is described in section III [9]. Four new master configurations are presented in section IV including a low-power version. Symmetric ultra low-voltage differential FF's are presented in section V with simulated results using $HSpice$ simulator and $90nm$ TSMC process.

II. ULTRA LOW VOLTAGE LOGIC

The original ULV inverter and ULV NP domino inverters are shown in Figure 1. The recharge phase starts when the clock signal ϕ switches from 0 to 1. Assuming a NPULV Pϕ inverter there are two different situations dependent on the state of the gate. First, assume that the output is 1 or close to 1, the nMOS floating gate is close to $V_{offset+}$ and the pMOS floating-gate is close to $V_{offset-}$ due to a static input in the previous evaluation phase. In this case the

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only work to be done is a marginal refresh of the floating-gates and the output. Secondly, assume that the output is 0, the nMOS floating gate is close to $V_{offset+} + k_{in}V_{DD}$ and the pMOS floating-gate is close to $V_{offset-} + k_{in}V_{DD}$ due to a positive input transition in the previous evaluation phase. In this case the output needs to be pulled to 1 and this is done by the pMOS and nMOS transistors in parallel. Notice that the nMOS E_{n2} is positive biased at the time of the clock edge and will contribute significantly to pull the output from 0 to 1. When the output is getting close to 1 the recharged pMOS evaluate transistor E_{p2} will pull the output to 1. The nMOS floating-gate will initially have a potential of $V_{offset+} + k_{in}V_{DD} \approx 1.5 \times V_{DD}$ and a positive current will flow to $V_{offset+}$ or V_{DD} while the nMOS floating-gate will be recharged through a negative current drawn from $V_{offset-}$ or gnd. Simulation shows that the time required to precharge the NPULV logic is two to three times the raise and fall times for different supply voltages.

The evaluation phase starts when the clock signal ϕ switches from 1 to 0. In the evaluation phase there are two different situations depending on the input. If the input is stable, i.e. no transition, during the evaluation phase the output will remain close to 1. The circuit will in this situation consume significant static current. The static current is dependent on the applied offset voltages $V_{offset-}$ and/or $V_{offset+}$ as well. Assuming a positive input transition, the floating-gates will be moved by $k_{in}V_{DD}$ and the output will be pulled down to 0 in a similar manner as a complementary inverter. The active current will be larger due to the boost of the evaluate transistors.

The ULV inverters shown in Figure 1 recharge simultaneously when $\phi = 1$. The precharge level is different, the P_ϕ precharges to 1 and while the output of the N_ϕ precharges to 0. The P_ϕ gate is susceptible to a positive input transition when the evaluate phase starts, i.e. $\phi = 0$.

III. Simple ultra low voltage Flip-Flop

The transistor counts for the Flip-Flops presented in this paper are less than for conventional Flip-Flops. The layout area is dependent on the implementation of the floating capacitors. The capacitance values for the floating capacitors are typically less than $1fF$, and hence can be implemented using MOS transistor parasitic capacitances and metal-metal. The accuracy of the floating capacitors is not critical and high level metal can be used.

The simple ULV Flip-Flop is shown in Figure 2 [9]. The input D is loaded onto QMP and QMN when $\phi = 0$. When ϕ switches from 0 to 1, one of the evaluate transistors E_{n1} or E_{p1} will be activated due to a boosted voltage level of QMN or QMP. If $D = 0$ then QMP will be pulled down to $\approx -V_{DD}/2$ and a large current provided by the E_{p1} transistor will be used to set the output of a slave latch and Flip-Flop to $Q = \overline{D}$. If $D = 1$ then QMN will be pulled up to $\approx 3V_{DD}/2$ and a large current provided by the E_{n1}

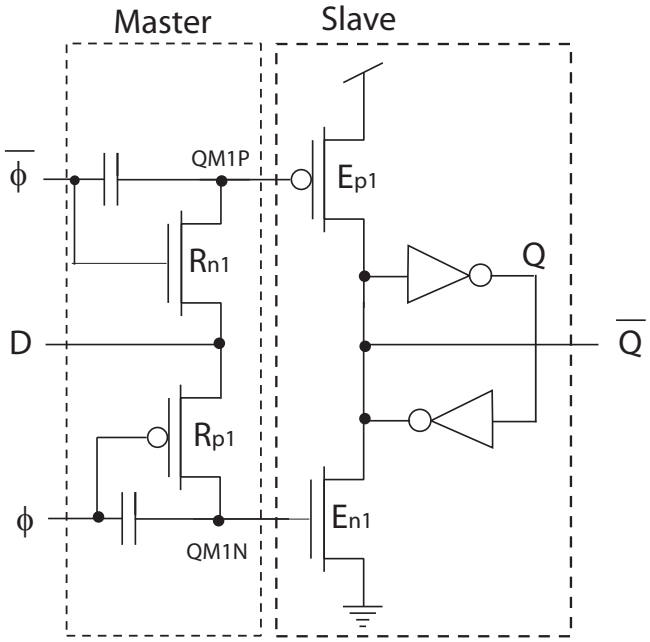

Figure 2. *Basic inverting ULV Flip-Flop.*

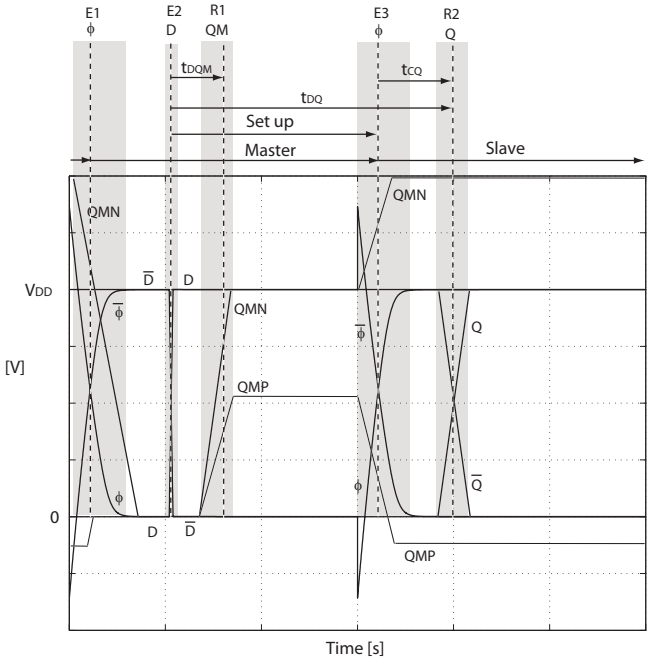

Figure 3. *Basic ULV Flip-Flop timing.*

transistor will be used to set the output of the Flip-Flop to $Q = \overline{D}$. The timing of the ULV Flip-Flop is shown in Figure 3. There are some critical events and timing restrictions that are important for performance of the ULV Flip-Flop:

1) E_1. Clock signal ϕ switches from 1 to 0. Any change in D will be loaded to QMP and QMN. If $D = 0$

then $QMP = D$ and $QMN \approx D$, and if $D = 1$ then $QMN = D$ and $QMP \approx D$. The slave latch will not be influenced by any changes in QMP or QMN due to the inverters at the output. The inverters must be strong enough to hold a stable output value when the master latch is transparent.

2) E_2. Input D is stable. The critical timing restriction is the setup time and thus only dependent on the delay through a pass transistor.
3) R_1. QMN and QMP will be set to D. More specifically, $V_{QMN} = V_{DD}$ if $D = 1$ and $V_{QMN} \approx V_{DD}/2$ if $D = 0$, and $V_{QMP} = 0V$ if $D = 0$ and $V_{QMP} \approx V_{DD}/2$ if $D = 1$.
4) $E_2 \rightarrow R_1$. Data to QM delay t_{DQM}.
5) E_3. Clock signal ϕ switches from 0 to 1. One of the evaluate transistors are activated trough a boosted QM voltage. The activated evaluate transistor will drive the output Q to $\overline{D}$ because the current level provided by the evaluate transistor is significantly larger than the current level of the inverters. This is the only event that may trigger the slave latch and determine the output of the Flip-Flop. The master latch becomes non active.
6) R_2. Slave latch will respond to QMN or QMP and set the slave latch output $Q = D$ and $\overline{Q} = DB$.
7) $E_1 \rightarrow E_3$. The master latch is active and output Q is stable due to the cross coupled inverters at the output.
8) $E_2 \rightarrow E_3$. Setup time for the input. This is the only significant delay of the ULV Flip-Flop.
9) $E_2 \rightarrow R_2$. Data to output time.
10) $E_3 \rightarrow E_1$. The slave latch is active and master latch is non active.

The simple ULV master latch is shown in Figure 2. D is loaded onto $QM1P$ and $QM1N$ when $\phi = 0$. More specifically if $D = 1$ then $QM1N = D = 1$ and $QM1P < D$ due to the body effect, and if $D = 0$ then $QM1P = D = 0$ and $QM1N > D$. When the clock signal ϕ switches from 0 to 1 the recharge transistors R_{n1} and R_{p1} closes and the capacitive input will increase the voltage level of $QM1N$ and decrease the voltage level at $QM1P$. In the case of D being equal to 1 the resultant voltage at $QM1N$ is $>> V_{DD}$ hence $>> D$ and$QM1P$ is ≈ 0 hence $\approx \overline{D}$. In this case the nMOS transistor E_{n1} is more enhanced than the E_{p1} transistor and the output $\overline{Q}$ will be pulled to $0 = \overline{D}$ through a large current provided by E_{n1}. The QM nodes will be floating until the next event determined by the clock switching from 1 to 0. Hence, the E_{n1} and E_{p1} transistors will be ON until this event and contribute to power consumption. One or both of these transistors should be turned OFF to save power while the slave is active.

The most critical timing issue in the ULV Flip-Flop is the setup time of the master latch. The elevated current level of the evaluation transistors in a slave latch, i.e. slave latch in Figure 2, will pull the output quickly to the right value. Typically, the clock to output delay is negative due to the extremely low rise and fall time of the output $\overline{Q}$.

IV. MASTER LATCHES

In this section we present new master latch configurations aimed for ultra low-voltage applications including a novel low power version. The master latches presented are different from previously published ULV Flip-Flops [9] in several aspects. The inputs to the Flip-Flops are used to control the recharge transistors and are used to reduce the static power consumption. By adding transistors to increase the control of the semi floating-gates, i.e. QM voltages, we can turn off the non active evaluation transistors. Compared to the ULV Flip-Flop in [9] all the presented master latches and Flip-Flops described in this paper are low power.

Different implementations of ultra low voltage master latches are shown in Figure 4. The basic master latch is shown in Figure 2 where the input D is applied through pass transistors. In Figure 4 2) additional recharge transistors, labeled K_{n2} and K_{p2}, are applied to the QM nodes. The effect of these transistors is provide a way to turn the evaluate transistors off and thereby reducing the power consumption when $\phi = 1$. The $QM2N$ and $QM2P$ will be affected while the clock signal switches and the full effect of the signal through the floating capacitor may be reduced. In Figure 4 3) a differential input master latch is shown where we use the $\overline{D}$ input to turn off the most active evaluate transistor. This configuration will not be as robust as the master latch in 2). The master latch shown in Figure 4 4) resembles the circuit in 2). The effect of the keeper transistors K_{n4} and K_{p4} will be delayed slightly compared to K_{n2} and K_{p2} and the effect of the signal applied to the floating capacitors are more evident. In Figure 4 5) the additional transistors are controlled by the output of the slave latch $\overline{Q}$. If the output $\overline{Q} = 1$ the K_{n5} transistor will be turned on and reduce the current running through transistor E_{n5} and hence reduce the power consumption and increase the noise margin of a slave latch.

Simulated responses for different master latches are shown in Figure 5. The supply voltage is $200mV$ and timing details for event E_1 and E_2 are shown. The master latches become active when ϕ switches from 1 to 0 and D is passed onto the QM nodes through the recharge transistors. At event E_2 the input changes from 0 to 1 and the QM are affected. $QM2N$, $QM2N$ and $QM4N$ will be pulled to 0 after right after the output of the slave is pulled to 0. Master latches 1), 3) and 5) require less set-up time than 2) and 4).

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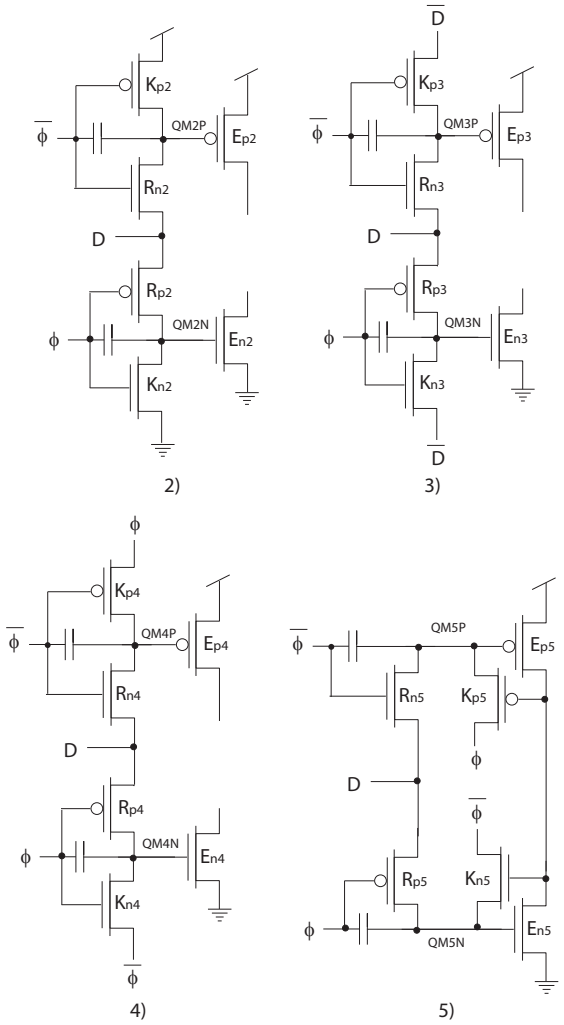

Figure 4. *Different master latch configurations. The input D can be used to provide a reference to E_{p1} and E_{p2}, and $\overline{D}$ can be used to provide a reference to E_{n1} and E_{n2}.*

V. SYMMETRIC DIFFERENTIAL ULTRA LOW-VOLTAGE FLIP-FLOPS

A symmetric and differential ULV Flip-Flop is shown in Figure 6. The master latches are similar to that of Figure 4 2) and the slave latches resemble the basic slave latch shown in Figure 2. The presented Flip-Flop is different from the Flip-Flop presented in [9] by using the input D, and $\overline{D}$, to power the evaluation transistors E_{n1}, E_{n2}, E_{p1} and E_{p2} directly. This reduces the signal path from input to output of the ULV Flip-Flops described. The most critical timing issue of the master latches presented is the set-up time. By using the D and $\overline{D}$ inputs directly to the evaluate transistors as if they were pass transistors the Flip-Flop will react more quickly because all evaluate transistors will the pull the outputs in the same direction.

In order to reduce the input load the evaluate transistors

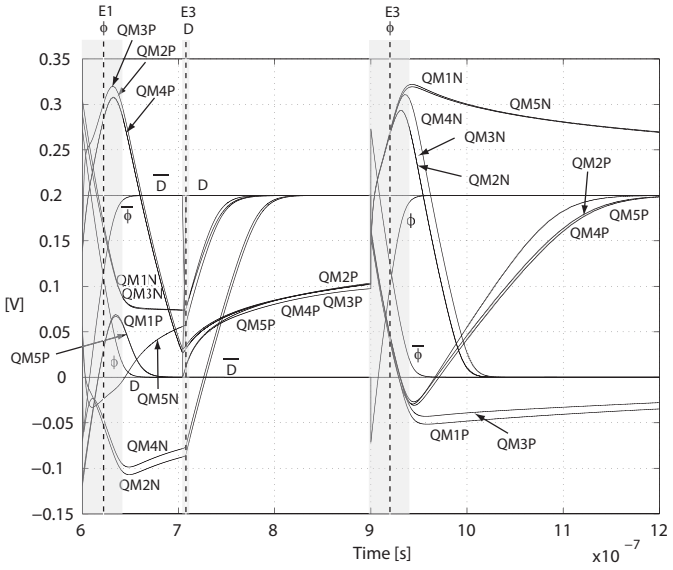

Figure 5. *Simulated response for different master latches.*

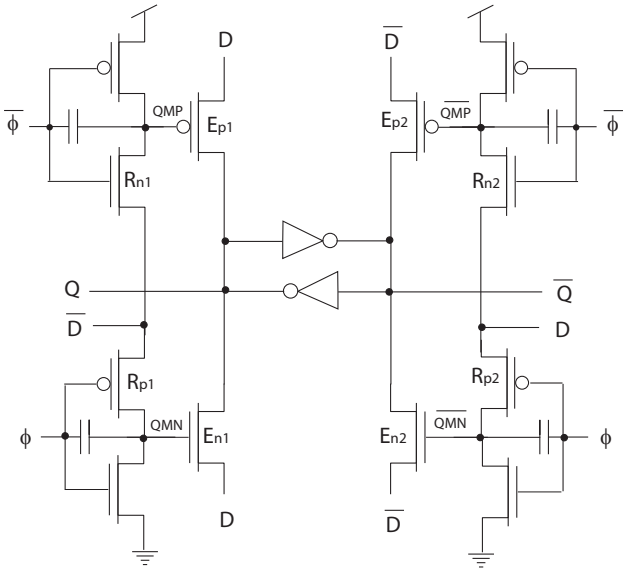

Figure 6. *The symmetric high-speed ULV Flip-Flop.*

E_{p1} and E_{p2} can be connected directly to V_{DD}, and E_{n1} and E_{n2} can be connected directly to gnd. This will only affect the response of the Flip-Flop slightly.

An alternative Flip-Flop with reduced input load and increased output- and clock load is shown in Figure 7.

A. Set-up details

In Figure 8 the set-up details for input $D = 1$ and $Q = 0$ are shown. The recharge transistor R_{n1} will pass the $\overline{D} = 0$ onto the gate of evaluate transistor E_{p1}. This node is labeled QMP. In the set-up phase QMP becomes 0 and QMN will be close to 0. Transistor E_{p1} will be activated when $\overline{\phi}$ switches from 1 to 0. At the same time the recharge transistor

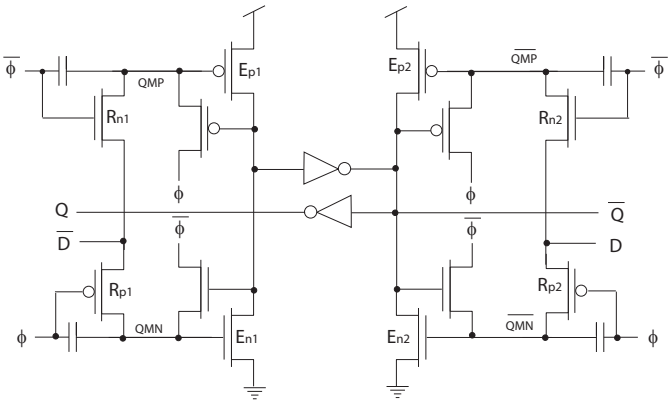

Figure 7. *Alternativ symmetric and low power high-speed ULV Flip-Flop.*

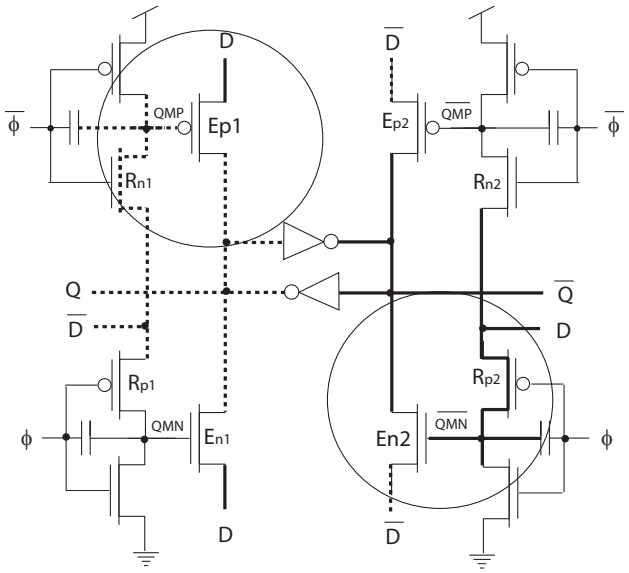

Figure 8. *The symmetric high-speed ULV Flip-Flop set-up details.*

$\overline{R_{p2}}$ will pass $D = 1$ onto the gate of transistor E_{n2} labeled $\overline{QMN}$. Transistor E_{n2} will be activated when ϕ switches from 0 to 1. The transistors E_{p1} and E_{n2} force the output Q and $\overline{Q}$ quickly to 1 and 0 respectively due to elevated current levels.

B. Simulated delay

V_{DD}	Conv.	Nik.	ULV
	t_{dq}	t_{dq}	$t_{setup} + t_{cq} = t_{dq}$
$300mV$	$22.6ns$	$8.55ns$	$3.57ns$
$350mV$	$10.0ns$	$3.65ns$	$1.69ns$

Table I
Simulated delay for conventional CMOS FF[10], Nikolic sense aplifier FF[8] and symmetric differential ULV FF.

Simulated delay, using $Hspice$ and parameters for a $90nm$ CMOS (RSMC) process, for the symmetric differential ultra low-voltage Flip-Flop in Figure 6 for supply voltages $300mV$ and $350mV$ are given in Table I. The data to output delay, i.e. setup time and clock to output delay, is compared to data to output delay of a conventional CMOS Flip-Flop[10] and the Nikolic sense amplifier Flip-Flop[8].

VI. Conclusion

In this paper we have presented high-speed low-voltage static Flip-Flop and different master latch configurations. Different low power master latch configurations are presented. The data to output delay for the ultra low-voltage Flip-Flop is significantly reduced compared to conventional CMOS Flip-Flop and sense amplifier Flip-Flop. The Flip-Flops is designed for ultra low-voltage digital systems, i.e. supply voltages below 0.5V. Compared to conventional Flip-Flops the delay of the proposed Flip-Flop is reduced to less than 50%.

References

[1] Chandrakasan A.P. Sheng S. Brodersen R.W.: "Low-power CMOS digital design" , *IEEE Journal of Solid-State Circuits*, Volume 27, Issue 4, April 1992 Page(s):473 - 484

[2] Verma N. Kwong J. Chandrakasan A.P.: "Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits" , *IEEE Transactions on Electron Devices*, Vol. 55, NO. 1, January 2008 Page(s):163 - 174

[3] K. Usami and M. Horowitz: "Clustered voltage scaling technique for low-power design", *International Symposium on Low Power Electronics and Design (ISLPED)*, 1995, Pages: 3 - 8

[4] Mutoh S., Douseki T., Matsuya Y., Aoki T., Shigematsu S., Yamada J.: "1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS" *IEEE Journal of Solid-State Circuits*, Volume 30, Issue 8, Aug. 1995 Page(s):847 - 854

[5] Y. Berg, D. T. Wisland and T. S. Lande: "Ultra Low-Voltage/Low-Power Digital Floating-Gate Circuits", *IEEE Transactions on Circuits and Systems*, vol. 46, No. 7, pp. 930–936,july 1999.

[6] Y. Berg, O. Mirmotahari, J. G. Lomsdalen and S. Aunet: "High speed ultra low voltage CMOS inverter", *In Proc. IEEE Computer society annual symposium on VLSI*, Montepellier France, April 2008.

[7] Y. Berg: "Novel High Speed and Ultra Low Voltage CMOS Flip-Flops", *In Proc. IEEE International Conference on Electronics, Circuits and Systems ICECS*. 2010 ISBN 978-1-4244-8156-9. s. 298-301, Athens, Greece.

[8] B. Nikolic, V.G Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu and M. T.-T. Leung: "Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements", *IEEE J. Solid-State Circuits*, vol. 35, pp.867-877, June 2006.

 ISBN: 978-1-61208-213-4

[9] Y.Berg: “Differential static ultra low-voltage CMOS flip-flop for high speed applications”, *In Recent researches in circuits, systems, mechanics and transportation systems : Proceedings of the 10th WSEAS International Conference on Circuits, Systems, Electronics, Control and Signal Processing (CSECS ’11)*. Montreux, Switzerland, December 29-31, 2011. World Scientific and Engineering Academy and Society 2011 ISBN 978-1-61804-062-6. s. 134-137.

[10] N.H.E Weste and D.M. Harris: Integrated circuit design”, Fourth edition 2011, ISBN 10:0-321-69694-8, *Pearson*.

 ISBN: 978-1-61208-213-4