The Impact of High Dielectric Permittivity of 2-D Numerical Modeling Nanoscale SOI Double-Gate Mosfet Using Nextnano Simulator

Samia SLIMANI, Bouaza DJELLOULI
Department of Electronic, Faculty of Science
Laboratoire de Modélisation et Méthodes de calcul LMMC, University of Saida
Saida, Algeria
e-mail: slimani.samia @gmail.com, djelbou@hotmail.com

***Abstract*—Performance of high-k Double-Gate SOI MOSFETs is studied and compared to silicon dioxide based devices. This is achieved by computing variation of threshold voltage, swing subthreshold, leakage current and drain-induced barrier lowering (DIBL) with respect to different gate bias (V_G) when gate length (L_G) decreases. This comparison is pinpointed taking SiO_2 and HfO_2 as gate oxides. Furthermore, quantum effects on the performance of DG MOSFETs are discussed. It is observed that less EOT with high permittivity reduces the tunnel current and serves to maintain high drive current, when compared with device using SiO_2 dielectric. Our results show that the characteristics of SOI Double Gate MOSFET with HfO_2 are superior to that of a device with SiO_2 dielectric**

***Keywords-high-k;* DG-MOSFET; quantum effects; nextnano3d; modeling.**

I. INTRODUCTION

Over the past years, silicon-based electronic technology has been improved through downscaling MOSFETs, resulting in higher device performance and density. However, it has been expected that this downscaling will reach its limits about the gate of 5 nm around the year 2020 or so. The 2006 edition of the ITRS (International Technology Roadmap for Semiconductors) forecasts a minimum feature size of 18 nm-node, a physical gate length of 7 nm for the year 2018 [1]. According to ITRS, a very thin gate insulator with EOT (Equivalent Oxide Thickness) less than 1 nm is required for both high performance and low power consumption CMOS devices. The thinner oxide lets more current leak between the gate and the substrate, driving up power consumption and better on- and off-state control [2]. In order to obtain a very thin EOT, we need to use high-k gate insulator such as HfO_2 which is the most promising candidate, since it possesses high dielectric constant and good thermal stability in contact with silicon [2, 3].

Another way to overcome short channel effects (SCE) is the use of multiple-gate structures on undoped SOI (Silicon On Insulator). One of these architectures is the Double Gate MOSFET (SOI DG-MOSFET) intended to control the channel very efficiently by applying a gate contact to both sides of the channel [4]. The intrinsic channel Double Gate MOSFET needs to rely solely on gate work function to achieve multiple threshold voltages on a chip due to the absence of body doping, which is efficient tool to adjust the threshold voltage in Double Gate MOSFET with doped channel [5, 6].

From the very beginning of semiconductor technology, it was thought that numerical, physics-based analysis of devices could help a great deal in their understanding. Nowadays, simulation and modeling of semiconductor devices have become one of the most important development methodologies in industry and research alike [7]. In this work we use the nextnano code to simulate a DG-MOSFET with high-k gate dielectric. This simulation tool is based on the self-consistent solution of the Schrödinger, Poisson and current equations [8, 9]. The coupled Poisson-Schrödinger system is solved by an approximate quantum charge density, which is employed inside of Poisson's equation in order to estimate the dependence of the density on the potential through Schrödinger's equation. Using this estimator the coupling between both equations is much decreased and rapid convergence is achieved. The electronic structure is calculated within a single-band or multiband k .p envelope function approximation. The included model for the carrier transport is a Wentzel–Kramer–Brillouin (WKB)-type approach also known as quantum-drift-diffusion (QDD) method, where the carriers are locally in equilibrium, charactized by a local Fermi level [10, 11].

The outline of the paper is as follows. Section II describes device structure. Section III presents some theoretical aspects. Section IV shows the simulation results using Quantum-drift-diffusion method. Using different gate oxide, the DIBL, subthreshold slope, and I_{on} current versus I_{off} current under different EOT are presented and compared, also the gate direct tunneling current as function of the gate voltage are presented. Section V concludes the paper.

II. DEVICE STRUCTURE

An even higher I_{on} current and decreased subthreshold slope can be obtained by the careful choice of a gate dielectric. Moreover a Physical gate length of 7nm is kept constant for easy comparison. At this channel length limits, the susceptibility of the transistor to short channel effects

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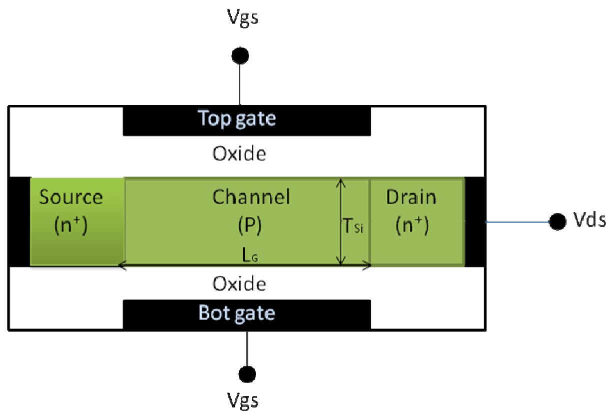

Fig. 1 Symmetrical DG-MOSFET considered in this work.

(SCE) is monitored in several ways such as threshold voltage (V_{TH}), leakage current (I_{off}) and drain induced barrier lowering (DIBL).

The structure of the proposed device is shown in Fig. 1. This symmetric structure is characterized by p-type doped Si channel of width 5nm. This channel is embedded between two heavily n-doped source and drain regions of length 10 nm that are connected to source and drain contacts. The junctions are assumed to be abrupt. The doping concentration of channel and source/drain are 10^{16} cm^{-3}, 10^{20} cm^{-3} respectively. The polysilicon gates with work function 4.1eV are separated from the Si channel by an oxide layer and the power supply voltage V_{DD} is 0.7V.

The 7nm length is chosen to study the performances of device, taking different Oxide thickness (5nm, 1.5nm, 1nm and 0.8nm) with the two Si channel width (5nm and 3nm) for both SiO_2 and HfO_2.

III. THEORETICAL ASPECTS

The model of carrier transport used in this paper is the quantum-drift-diffusion model as implemented in nextnano. This model uses the first moment of the Boltzmann equation to determine the current and the quantum mechanics to calculate the carrier density. The charge density $n_c(x)$ for carriers of type c is calculated by assuming the carriers to be in a local equilibrium characterized by local quasi-Fermi levels $E_{FC}(x)$

$$n_c(x) = \sum_i \left|\psi_{ic}(x)\right|^2 f\left(\frac{E_{Fc}(x) - E_{ic}}{k_B T}\right) \qquad (1)$$

ψ_{ic} and E_{ic} are respectively wave function and energy of eigenstate i that have been obtained from solving the multiband Schrodinger-Poisson equation [8].

The local quasi-Fermi levels $E_{F,c}(x)$ are determined by global current conservation $\nabla \cdot j_C = 0$, where the current J_c is assumed to be given by the semi-classical relation:

$$j(x) = \mu(x) n(x) \nabla E_{F,n}(x) \quad . \qquad (2)$$

The EOT (Equivalent Oxide Thickness) used in this work is that obtained by classical Electrostatic theory in planar devices where [12]:

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} T_{high-k} \quad . \qquad (3)$$

The SiO_2 and HfO_2 permittivities (k_{SiO2}, k_{high-k}) are 3.9 and 21.2 respectively, T_{high-k} : high-k material thickness.

IV. RESULTS

Using the proposed model, the DIBL is calculated for V_{DS} = 50 mV and plotted as a function of the oxide thickness (EOT) in Fig. 2. The evolution of the barrier for T_{Si} varying between 5nm and 3nm illustrates clearly the dependence of the drain-induced barrier lowering (DIBL) on permittivity and Si channel width. The range of variation of the DIBL for SiO_2 based device is from 0.02 eV for T_{Si} = 5nm to 0.063eV for T_{Si}=3nm. The DIBL is decreased for HfO_2 based device and varies from 0.015eV for T_{Si}=5nm and 0.023eV for T_{Si}=3nm. From this figure it can be concluded that HfO_2 has a great impact on the reduction of DIBL.

Fig. 3 illustrates the effect of high permittivity on subthreshold slope. It is well known that a small subthreshold slope is highly desired since it improves the ratio between the on- and off-currents. It is clear from figure 3 that for SiO_2 the subthreshold slope is degraded by almost 400 % when the oxide thickness is reduced from 0.8 nm to 5 nm for a channel width of 5 nm. While for HfO_2 the subthreshold slope is less degraded (only 148 %) for the same channel width. The figure also show that reducing the channel width (T_{Si}) to 3nm the same trends as already are observed for both SiO_2 and HfO_2. The subthreshold slope takes a minmum value 90 mV/dec at EOT=1.5nm. We can conclude that subthreshold characteristics of SOI DGMOSFET based HfO_2 are clearly better than SiO_2 based device, but remains far from ITRS recommendation as the subthreshold slope S should not be higher than 80mV/dec.

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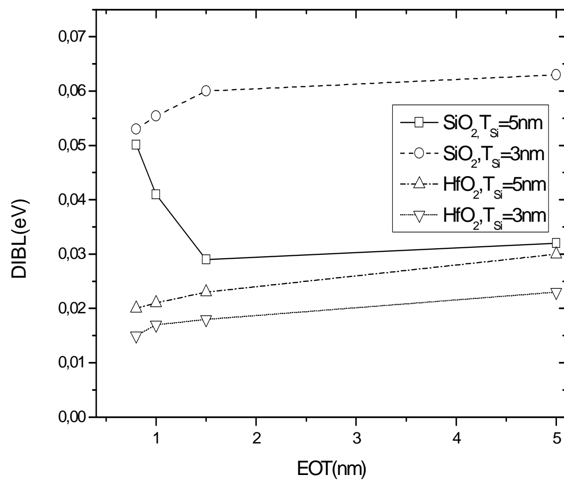

Fig. 2 DIBL as a function of the oxide thikness EOT (nm)

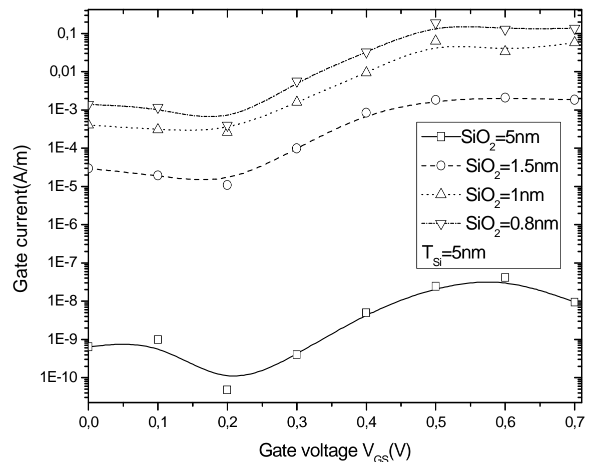

Fig. 4 Gate current as function of gate voltage for SiO_2.

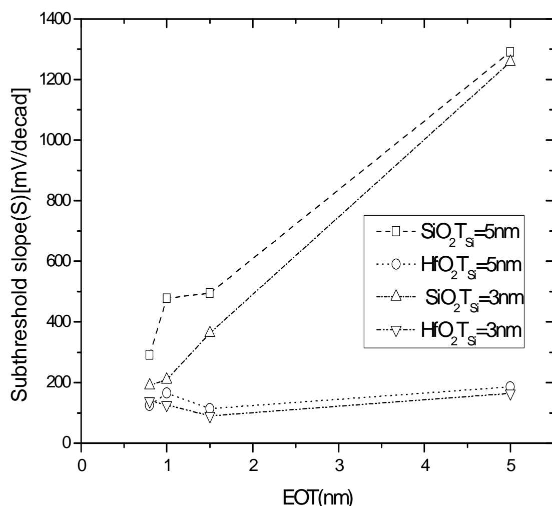

Fig. 3 Subthreshold slope as a function of EOT

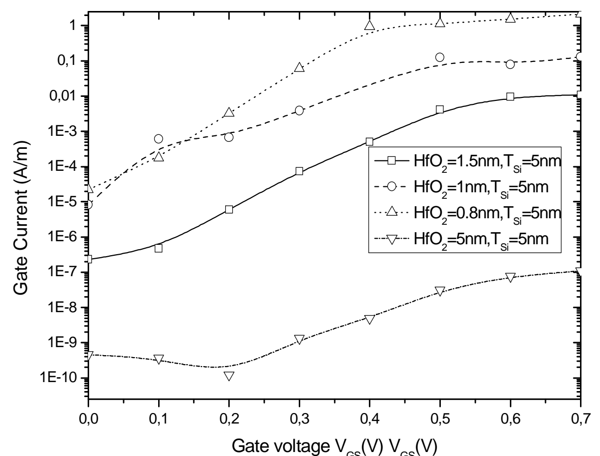

Fig. 5 Gate current as function of gate voltage for HfO_2

Fig. 4 and Fig. 5 show gate direct tunneling current as function of the gate voltage. The gate direct tunneling current becomes an increasingly important such when reducing T_{Si} at 0.8nm physical thickness, and becomes much higher when replacing SiO_2 with HfO_2 thus the gate current at $V_{DS}=V_{DD}=0.7V$, is varied from $9.15 \cdot 10^{-19}$ A/m at EOT=5nm to 0,135A/m at EOT=0.8nm for SiO_2 and from $1.09 \cdot 10^{-7}$ at EOT=5nm to 2,03A/m at EOT=0.8nm.

The I_{on} current versus I_{off} currrent for different EOT and for two channel width is represented in Fig. 6. The high permittivity increases I_{on} and decreases I_{off} for various EOT, for HfO_2 at EOT=0.8nm, I_{on} current value tends towards 1002.02 A/m with I_{off} currrent value equal to 0.15A/m, besides the SiO_2 I_{on} current value which is equal to 717A/m with I_{off} currrent value equal to 35.208A/m but when reducing the Si width channel to 3nm, we obtained a little values for I_{on} current and I_{off} currrent than 5nm width channel, in this case I_{on} current is much weak, which is cannot meet the ITRS predicted value.

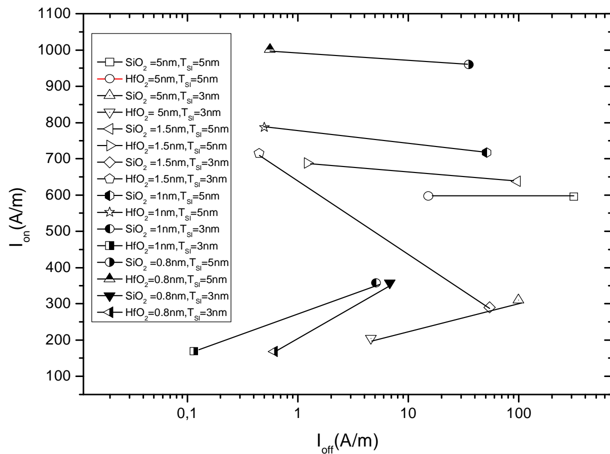

Fig. 6 I_{on} as As a function of I_{off}

V. CONCLUSION

In order to improve subthreshold slope and to suppress drain-induced barrier lowering in SOI MOFET, double gate architecture and high-k dielectric are introduced in this paper. The simulations were conducted using the nextnano code which uses a quantum-drift-diffusion model for carrier transport taking into account quantum confinement effects. It s concluded that hafnium oxide is one of the best candidate to replace SiO_2, due to its extremely high subthreshold slope. Also HfO_2 is effective at reducing I_{off} current and maximizing the ratio of I_{on}/ I_{off}.

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