Design of Reconfigurable Quad-band CMOS Class AB Power Amplifier employing MEMS Variable Capacitors in 0.18µm Technology

Elhadji Mansour Fall, Frederic Domingue
Laboratoire de Microsystèmes et Télécommunication
Université de Québec à Trois-Rivières (UQTR)
Trois-Rivières, QC, Canada
e-mail: mansour.fall@uqtr.ca
frederic.domingue@uqtr.ca

Siamak Fouladi, Raafat R. Mansour
Centre for Integrated RF Engineering (CIRFE)
University of Waterloo
Waterloo, Ontario, Canada
e-mail: siamakf@maxwell.uwaterloo.ca
rrmansour@uwaterloo.ca

***Abstract*— A reconfigurable quad-band CMOS power amplifier suitable for multi-band radiofrequency transceivers is presented. The multi-band power amplifier is a reconfigurable monolithic microwave integrated circuit designed to operate in 1.7, 1.8, 1.9 and 2.1 GHz frequency bands. The structure is a single ended one stage class AB power amplifier with tunable impedance matching network based on high Q micromachined inductors and MEMS tunable capacitors. The reconfigurable power amplifier is fully integrated in 0.18µm CMOS technology and achieves maximum output power with good efficiency over different operating frequencies. The device has a simulated maximum output power of 20 dBm and can achieve a variable gain over than 16 dB in the four operating bands with a power-added efficiency (PAE) better than 50%.**

Keywords- reconfigurable power amplifier; tunable impedance matching; RF microelectromechanical system (MEMS); CMOS-MEMS; variable capacitors

I. INTRODUCTION

As the wireless market continues to grow with the proliferation of wireless communications standards such as GSM, WCDMA, and Wimax, there is increasing demand for reconfigurable multi-band RF front-ends that meet the specifications of various standards.

Considering multi-band operation, designing reconfigurable power amplifier (PA) is required for multi-standard RF transceivers. From the cost point of view, CMOS technology is a breakthrough in competitive RF monolithic integrated circuits, allowing development of cost effective reconfigurable PA.

There are different configurations to achieve multi-band operation and many reconfigurable PAs using different approaches have been reported. The conventional multi-mode implementation consists of a combination of different PA units, designed optimally for each frequency band [1]. Although the PA module presents high performance, it needs complex structure resulting in larger circuit. The second method is a wideband approach with input and output impedance matching in wide range of frequencies [2]. However it is difficult to achieve high efficiency in all bands of interest. Compared to the two first methods, the tunable approach would avoid the use of redundant blocks of single PA and is based on adaptive matching network [3].

The introduction of radio-frequency micro-electro-mechanical systems (RF-MEMS) components have opened new perspectives to implement this ideal solution with enhanced tuning range, low loss and high quality factor Q of passive devices. The reported reconfigurable PAs based on tunable impedance matching network with MEMS switches and/or stubs have demonstrated a high output capability with good efficiency over several bands of operation [4]-[5]. However these devices require the hybrid integration of the MEMS matching network. Thanks to significant advances in CMOS-MEMS integration, reconfigurable PA fully integrated in CMOS process can be achieved.

In this work, the design of a reconfigurable quad-band class AB CMOS power amplifier with the help of MEMS variable capacitors and micromachined inductors is presented. The designed PA is fully integrated in 0.18 CMOS technology and operates in 1.7, 1.8, 1.9 and 2 GHz.

The paper is organized as follow. In next Section, the design of the class AB power amplifier is described. Section 3 presents the tunable approach with MEMS variable capacitors and Section 4 presents the simulation results. Conclusion and future work are summarized in Section 5.

II. CLASS AB POWER AMPLIFIER DESIGN

Power amplifiers have balancing parameters which, often are in conflict; thus a good linearity comes usually at the cost of efficiency. The aim is to achieve 20dBm of output power with good efficiency. A reduced conduction angle configuration is adopted and Figure 1 shows the schematic of the single ended one stage class AB power amplifier.

A. Transistor characterization & circuit design

The first step of the design consists to provide a suitable biasing point for the power amplifier to operate ideally in class AB region. The power amplifier's figure of merit such as maximum output power, gain, efficiency and linearity are related to the bias conditions. Using 0.18µm 1P6M RF-CMOS process available from TSMC, the voltage supply is fixed at 1.8 V for a maximum output voltage swing. The relative low oxide breakdown voltage in bulk CMOS technology limits the maximum drain voltage, hence the

 ISBN: 978-1-61208-150-2

maximum output power. In order to increase the output power, a large transistor size required. The transistor width is chosen according to the maximum driven current capability required for 20 dBm output power. The maximum drain current is derived from [6] with a conduction angle α equals to 3π/2. The corresponding current value is 200mA which in turn leads to a transistor width of 400µm in TSMC 0.18µm RF-CMOS process. To operate in class AB, the gate is biased at 1.05 V corresponding to a DC bias current of 90 mA.

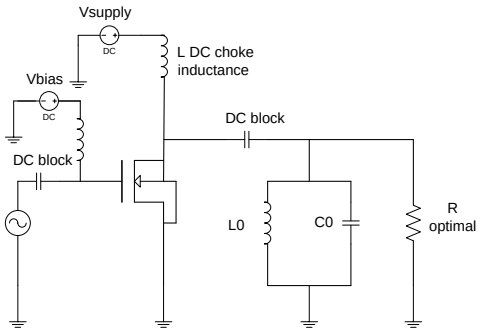

Figure 1. Schematic representation of the power amplifier

The inductor *L* is used as a DC biasing choke to set the DC level of the transistor to the supply voltage. It must have a high reactance at the operating frequency and with the assumption that its value is ten times greater than the load impedance, an inductance of 12 nH will suffice for all frequencies from 1.7 GHz to 2.1 GHz. An integrated capacitor of 10 pF is used as DC blocking capacitor.

The LC tank at the output termination is designed to resonate at $\omega_0^2 = 1/L_0C_0$ and removes higher harmonics.

B. Load pull analysis

For the given transistor size and bias conditions, the load impedance is swept in order to find the optimal load which, enables a maximum output power. To perform the load pull simulation, the input of the power amplifier is conjugately matched to the source for a maximum power transfer. Figure 2 shows the load pull simulation results for 2.1GHz frequency band.

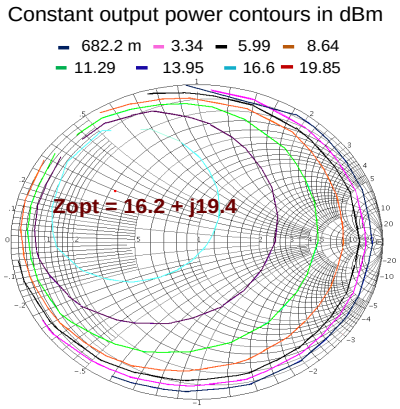

Figure 2. Load pull simulation results for 2.1 GHz.

An optimum power matching point is found after load pull analysis over the different operating bands. The maximum output power is delivered to the load with optimal impedance $Z_{opt} = 16.2 + j19.4\ \Omega$ at all frequencies of interest.

C. Input & Output matching networks

The output matching network is designed to transform the 50 Ω load antenna into optimal load impedance Z_{opt}. The matching network is also implemented in L-sections configuration as shown in Figure 3.

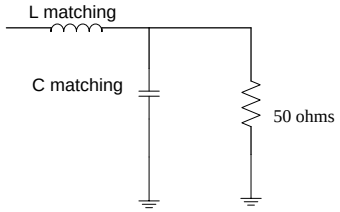

Figure 3. Fixed matching network

The required values for the impedance matching network are listed in Table I.

TABLE I. REQUIRED COMPONENT FOR OUTPUT MATCHING

Frequency	1.7 GHz	1.8 GHz	1.9 GHz	2.1GHz
C matching	2.7 pF	2.6 pF	2.4 pF	2.2 pF
L matching	3.56 nH	3.36 nH	3.25 nH	2.88 nH

The input matching network is designed to match the large signal input impedance of the transistor with the 50 Ω source impedance. The large signal input impedance is extracted at the operating frequency for a given output power such as 1 dB compression point. Table 2 summarizes the input impedance for each frequency and the required reactive components for source matching.

TABLE II. INPUT IMPEDANCE & REQUIRED COMPONENTS FOR INPUT MATCHING

Frequency	1.7 GHz	1.8 GHz	1.9 GHz	2.1GHz
Input Impedance (Ω)	221.5 + j 57.05	229 + j30	203 – j6.5	180 – j 29.8
C matching	869 fF	779 fF	763.3 fF	608 fF
L matching	9 nH	8.4 nH	7.3 nH	6.1 nH

III. TUNABLE AMPLIFIER WITH MEMS VARIABLE CAPACITORS

The reconfigurable amplifier is integrated with micromachined inductors and tunable matching sections based on variable CMOS-MEMS capacitors. The schematic of the designed circuit is presented in Figure 4.

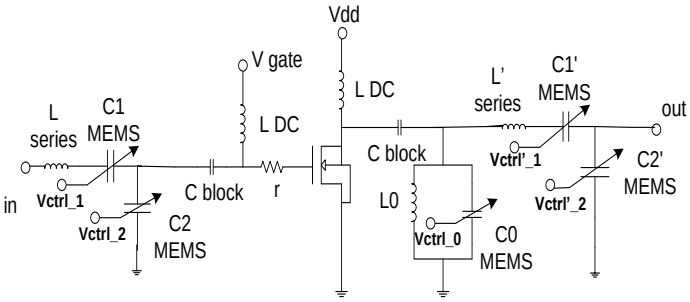

Figure 4. Schematic of the quad band reconfigurable power amplifier

A. *Tunable matching network*

The matching network is based on L-networks configuration for different operating frequencies and variable values for the inductance and capacitance. The concept of the matching network used in this design consists of implementation of the network with a combination of fixed inductors and MEMS variable capacitors as shown in the schematic diagram of the PA circuit in Fig. 4.

To achieve the required impedance both for source and load matching, series inductance of 15 nH and 12 nH are coupled to the source and load respectively with two MEMS variable capacitors actuated by DC voltage between electrodes to insure tunability over the four operating frequencies. In addition, the resonant frequency of the LC tank can be tuned by varying L_0 and C_0. In this case, a MEMS variable capacitor is employed with fixed inductance of 4.5 nH.

The required states of MEMS capacitance for impedance matching and tunable resonance frequency are reported in Table III.

TABLE III. VARIABLE CAPACITANCE FOR SOURCE/LOAD MATCHING & RESONATOR

Frequency	Source matching	Load matching	Resonator
1.7 GHz	C_1= 1.5 pF C_2= 0.9 pF	C_1'= 1 pF C_2'= 2.7 pF	C_0 = 1.95 pF
1.8 GHz	C_1= 1.2 pF C_2= 0.8 pF	C_1'= 0.9 pF C_2'= 2.6 pF	C_0 = 1.7 pF
1.9 GHz	C_1= 0.9 pF C_2= 0.7 pF	C_1'= 0.8 pF C_2'= 2.4 pF	C_0 = 1.56 pF
2.1 GHz	C_1= 0.65 pF C_2= 0.60pF	C_1'= 0.63 pF C_2'= 2.2 pF	C_0 = 1.28 pF

B. *CMOS-MEMS Variable capacitor*

The MEMS variable capacitors proposed in [7] represent a practical configuration for the tunable matching network. The MEMS variable capacitor will be fabricated by the CMOS-MEMS post-processing technique described in Figure 5. The MEMS capacitor is implemented with M3 and M5 metal layers as the bottom and top plates, respectively. An air-gap is created in between by removing interconnect metal layer M4. This CMOS-MEMS post-processing technique is developed at Centre for Integrated RF Engineering (CIRFE) [8].

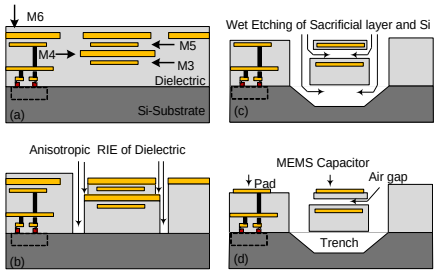

Figure 5. Post-CMOS processing steps required to integrate the MEMS parallel plate capacitors in the 0.18-µm CMOS process. (a) CMOS die after standard processing, (b) 1st RIE of CMOS dielectric layer, (c) wet etching of silicon substrate and the M4 sacrificial layer, (d) critical point drying and 2nd RIE of the CMOS dielectric layer capacitor's top plate and pads [7].

IV. SIMULATIONS RESULTS

The designed circuit was simulated using cadence Spectre. Simulations include components available from 0.18µm TSMC RF-CMOS process and device models for MEMS inductors and variable capacitor. The electrical models for micromachined inductors and MEMS variable capacitor were described in [9] and [10] respectively.

The gain for the tunable PA is over 16 dB in 1.7 GHz, 1.8 GHz, 1.9 GHz, and 2.1 GHz modes, respectively as shown in Figure 6. Figure 7 shows the frequency response of the PA from small signal simulation for the quad band of frequency.

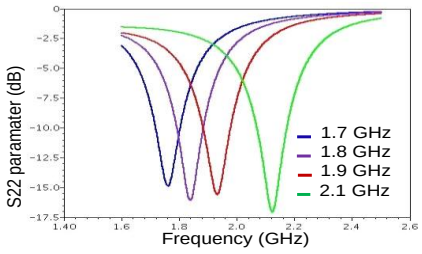

Figure 6. Simulated small signal S21 of the reconfigurable PA

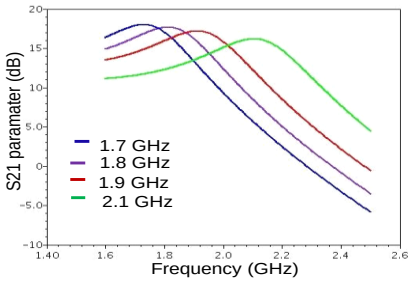

Figure 7. Simulated small signal S22 of the reconfigurable PA

The output matching network was designed to present the optimal load for maximum output power and the output return loss S_{22} of the amplifier is smaller than -10 dB for all frequencies.

Figure 8 shows the output power and PAE at various input power. As presented on plots, the linear output power is over 19 dBm in the four operating bands. The simulated PAE is 41.2%, 42%, and 41.6% in 1.7 GHz, 1.8 GHz, 1.9 GHz, and 2.1 GHz band respectively.

 ISBN: 978-1-61208-150-2

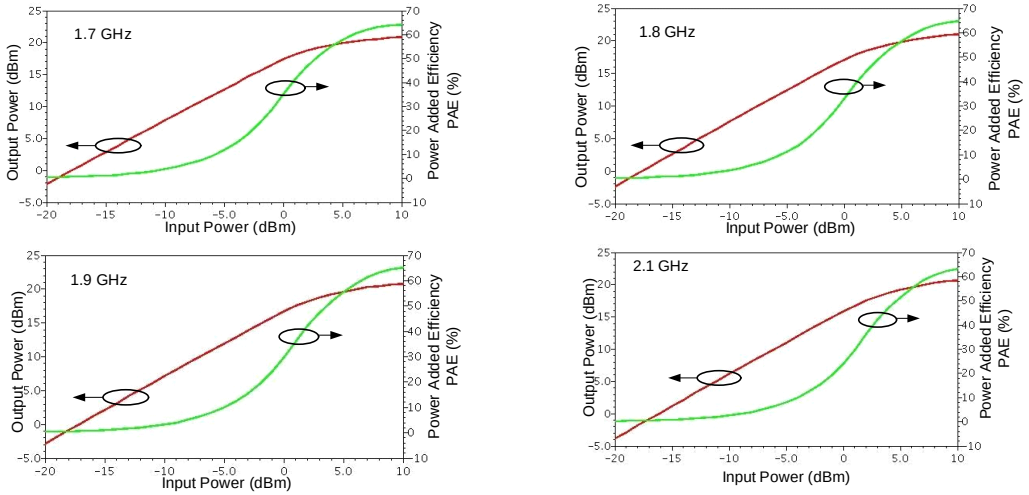

Figure 8. Simulated output power and efficiency PAE of the reconfigurable PA over the four operating band.

The designed tunable PA has been submitted for fabrication and the layout of the circuit is shown in Fig. 9.

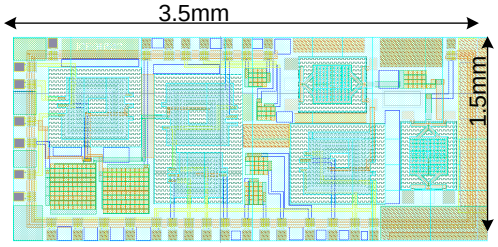

Figure 9. Layout of the proposed reconfigurable quad-band PA

V. CONCLUSION AND FUTURE WORK

In this paper, the design of a reconfigurable quad-band CMOS power amplifier (PA) operating in 1.7, 1.8, 1.9 and 2.1 GHz frequency bands is presented. The PA is fully integrated in 0.18µm CMOS technology and can be used in multi-band environment. Compared to traditional PAs, the designed device has a small circuit and works more effectively. The simulations results show that the PA can achieve a variable gain over than 16 dB with saturated output power of 20 dBm in the four operating bands and a PAE better than 50%. The proposed circuit is based on micromachined inductors and a tunable impedance matching network integrated with CMOS MEMS variable capacitors. The use of the CMOS-MEMS post processing technique allows the development of fully integrated reconfigurable RF circuits for multi-standard applications.

The designed reconfigurable power amplifier is regarded as our first prototype; hence future works will focus on the optimization of the design and the integration of next generation's PA with higher output power and suitable for multi-mode as well as multi-band application. The aim will be to develop a CMOS-MEMS reconfigurable PA according to the specifications for mobile phone standards.

ACKNOWLEDGMENT

The author would like to thank the Canadian Microelectronics Corporation (CMC) for the fabrication, UQTR and CRSNG (Conseil de recherches en sciences naturelles et en génie du Canada) for their financial support.

REFERENCES

[1] S. Zhang, P. Bretchko, J. Mokoro, and R. McMorrow, "On A novel power amplifier module for quad-band wireless handset applications," IEEE Trans. Microwave Theory & Tech., vol. 51, no. 11, pp. 2203-2210, November 2003.

[2] S.K. Wong, S. Maisurah, M.N. Osman, F. Kung and J.H. See, "High efficiency CMOS power amplifier for 3 to 5 GHz ultra-wideband (UWB) application," IEEE Trans. Consumer Electronics., vol. 55, no. 3, pp. 1546-1550, August 2009.

[3] W.C.E Neo, Y. Lin, X. Liu , L.C.N. de Vreede, L.E. Larson, M. Spirito, "Adaptive Multi-Band Multi-Mode Power Amplifier Using Integrated Varactor-Based Tunable Matching Networks," IEEE J. of Solid-States Circuits, vol. 41, no. 9, August 2006, pp. 2166-2176, doi: 10.1109/JSSC.2006.880586.

[4] A. Fukuda, H. Okazaki and S. Narahashi, "A Novel Compact Reconfigurable Quad-band Power Amplifier Employing RF-MEMS Switches," in 36th European Microwave Conference, January 2007, pp. 344-347, doi: 10.1109/EUMC.2006.281327.

[5] L. Larcher, R. Brama, M. Ganzerli, J. Iannacci, B. Margesin, M. Bedani, and A. Gnudi, "A MEMS Reconfigurable Quad-Band Class-E Power Amplifier for GSM Standard," 2009 IEEE 22nd International Conference on Micro. Electro. Mechanical Systems, March 2009, pp. 864-867, doi: 10.1109/MEMSYS.2009.4805520.

[6] S. C. Cripps, RF Power Amplifiers for Wireless Communication, 2nd edition, Norwood, MA 02062,Artech House, 2006.

[7] S. Fouladi and R. R. Mansour, "Reconfigurable amplifier with tunable impedance matching networks based on CMOS-MEMS capacitors in 0.18-µm CMOS technology," 2nd Microsystems and Nanoelectronics research Conference, pp. 33-36, November 2009.

[8] CIRFE, University of Waterloo, http://www.cirfe.uwaterloo.ca/.

[9] G. M. Rebeiz, RF MEMS Theory, Design, and Technology, New York, Wiley, 2003.

[10] J. Reinke, G. K. Fedder and T. Mukherjee "CMOS-MEMS Variable Capacitors Using Electrothermal Actuation," J. of Microelectromechanical Systems, vol. 19, no. 5, septembre 2010, pp. 1105 - 1115, doi: 10.1109/JMEMS.2010.206719.

 ISBN: 978-1-61208-150-2