Comparison of Three Impedance Analysers Implemented on FPGA Circuits

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***Abstract*— In this paper, we present three different methods we have developed for the design of an electrical impedance analyser implemented on an FPGA board. We describe in the first part the general principle of the methods : Ratiometric Measurement, Feedback Voltage Control and Adaptive Parametric Modelisation. In order to test and to compare the performances of each approach, the Hardware In the Loop strategy has been used. We present the steps from the mixed simulation using Matlab DSP Builder, which leads to the FPGA implementation. We investigate the limits and advantages for each method. The impedance analysis results of a model of an audio piezo transducer (7 kHz) are presented. The amplitude accuracy is less than 3 % and the analysis duration from 5 kHz to 10 kHz is about 54.5 ms for the first two methods.**

Keywords - electrical impedance spectroscopy; piezoelectric transducer; FPGA; DDS; Hardware In the Loop.

I. INTRODUCTION

The electrical impedance spectroscopy (EIS) applied to piezoelectric sensors and systems is very often used. It is commonly applied in non-destructive testing (NDT) [1][2]; to perform physical measurements [3]; biological measurements [4] or for the diagnosis of transducers [5]. In practice, the EIS requires heavy, bulky and expensive analyzer, (i.e., Hioki model IM 3570 : 5 MHz, 6 kg, 10 k$, Agilent model 4294A : 110 MHz, 25 kg, 40 k$) . To avoid these disadvantages, several research teams have investigated from 2004 on the design of implementable EIS on a light and low cost embedded system.

Various methods have been proposed. Petersen [6] designed a digital low power EIS device with an accuracy of 0.001%. The system includes an electrical bridge with two arms and a digital synchronous demodulator. One of the arms corresponds to the unknown impedance. The bridge is balanced by a least mean squares (LMS) algorithm. This method is not suitable when the impedance changes fastly and it is not implementable in a portable device.

Lewis et al. [7] have developed a cheap system for impedance spectroscopy with a frequency band between 700 kHz and 20 MHz. The excitation of the piezoelectric transducer is carried out with a pulse generator. The electrical impedance is then determined by a fast Fourier transform performed offline using the Matlab program.

Yang et al. [8] have designed a portable device whose principle is inspired by the traditional ratiometric method. For good accuracy, the device requires three successive algorithms of calibration.

Finally, Hamed et al. [9] have proposed and implemented on an FPGA target an impedance measurement method that does not require current measuring in the tested dipole. This method is based on feedback control of the excitation voltage.

In this paper, we present the implementation of three different EIS methods on an FPGA board. These methods are then applied to the analysis of the complex impedance Z of the same dipole.

In the first part, we present the principle and the equations of each method.

The second part is devoted to the digital architectures. The diagrams are described by the Altera-DSPBuilder tool. This allows the design and the implementation directly on the FPGA target from Matlab-Simulink.

In the last part, the impedance measurements of a Butterworth van Dycke dipole which simulate an audio piezo transducer, are analyzed and compared.

II. THE EIS TESTED METHODS

A. Ratiometric measurement (RM)

The principle of this methode is shown in Fig. 1

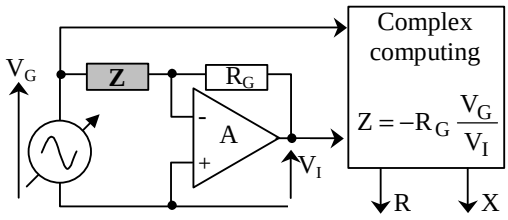

Figure 1. Ratiometric measurement of impedance

In this scheme, Z = R + jX is the unknown impedance, R_G is the reference resistor connected in series with Z.

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The output voltage of the operational amplifier is

$$V_I = -\frac{R_G}{Z} V_G \quad (1)$$

This determines the impedance Z by

$$Z = -R_G \frac{V_G}{V_I} = -R_G \left|\frac{V_G}{V_I}\right| e^{j\varphi} \quad (2)$$

where φ corresponds to the phase shift between the signals V_G and V_I

The computing block has two complex amplitude and phase detectors performed by quadrature demodulation

B. Feedback Voltage Control (FVC) method

In this system (Figure 2), a sinusoidal voltage generator V_G with an output resistance R_G is used to excite the tested dipole. The generator sweeps the desired frequency band. The voltage V_D applied to the dipole is regulated at a constant amplitude whatever the frequency is. For this reason, the variable resistor R_G is controlled in real time by a proportional-integral controller. The value of R_G and the phase φ between V_G and V_D are used to determine the complex value of Z.

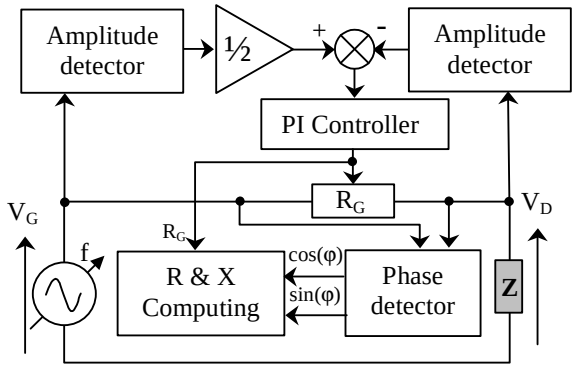

Figure 2. FVC method developed by Hamed and al.

The phase φ between V_D and V_G is determined by synchronous detection.

Real and imaginary parts of Z are determinated from φ and R_G at each frequency by

$$R = \frac{0.5\cos(\varphi) - 0.25}{1.25 - \cos(\varphi)} R_G$$
$$X = \frac{0.5\sin(\varphi)}{1.25 - \cos(\varphi)} R_G \quad (3)$$

C. Adaptive Parametric Modelisation (APM)

1) Principle

This model based method is represented in Figure 3. The dipole is considered as a system whose input is the voltage V and output is the current I. The transfer function of the dipole is then the admittance Y = 1/Z. An adaptive filter models in real time the dipole excited by a white noise. The spectral range is determined by the correlation time T_c of the white noise.

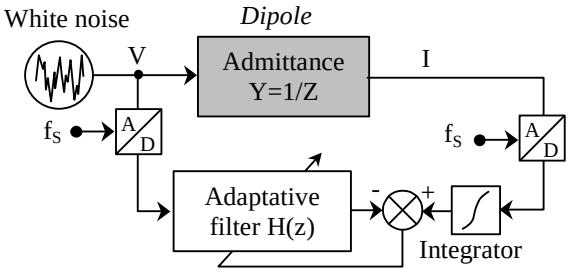

Figure 3. Adapatative parametric modelisation

The filter coefficients are identified with a classical LMS gradient algorithm.

This approach requires the "a priori" knowledge of the function Y(s) where s is the Laplace variable.

In this work, we are interested in the resonant dipole represented by a Butterworth van Dycke (BVD) structure (Figure 4). This structure corresponds to many transducers. It has a resonance frequency for which Z is minimal and a antiresonance frequency for which Z is maximal. So it is well suited to measure the accuracy of n impedanceanalyser.

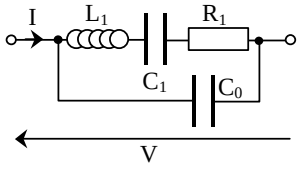

Figure 4. Butterworth van Dyck model

The admittance of this structure is

$$Y(s) = \frac{L_1C_0C_1s^3 + R_1C_0C_1s^2 + (C_0 + C_1)s}{L_1C_1s^2 + R_1C_1s + 1} \quad (4)$$

This admittance has a global capacitive behaviour. To reduce the risk of divergence of the gradient algorithm, Mayer et al. [10] suggest to carry out an integration of Y(s). This way standardizes the admittance modulus outside the resonance zone and reduces the system order.

2) Adaptive filter

It is possible to exploit a model of adaptive finite impulse response filter (FIR). In this case good resonance tracking requires the use of a high order transverse structure. That is why we use a recursive adaptive structure. His general transfer function H(z) is

$$H(z) = \frac{b_N z^{-N} + \cdots + b_1 z^{-1} + b_0}{a_N z^{-N} + \cdots + a_1 z^{-1} + 1} \quad (5)$$

where z is the variable of the Z-transform, N is the order and b_j, a_i are the coefficients of the filter.

III. FPGA IN THE LOOP IMPLEMENTATION

The design and implementation of digital architectures on FPGA target requires specific development tools.

Initially, the complete system is modelled under Matlab/Simulink. Indeed, the Mathworks and Altera companies have developed jointly software tools for fast FPGA prototyping.

- The analogue part is described with the SimPower System toolbox (Simulink).
- The digital part is described with DSPBuilder toolbox (Altera).

In a second step, the tool "Signal Compiler" of DSPBuilder generates the VHDL code of the digital architecture, which is implemented on the FPGA circuit.

Finally, with the hardware in the loop (HIL) simulation, the FPGA architecture is tested in a virtual environment in, which the analogue components are modelled [11].

In Figure 5, we illustrate the design steps of the FPGA in the loop prototyping approach.

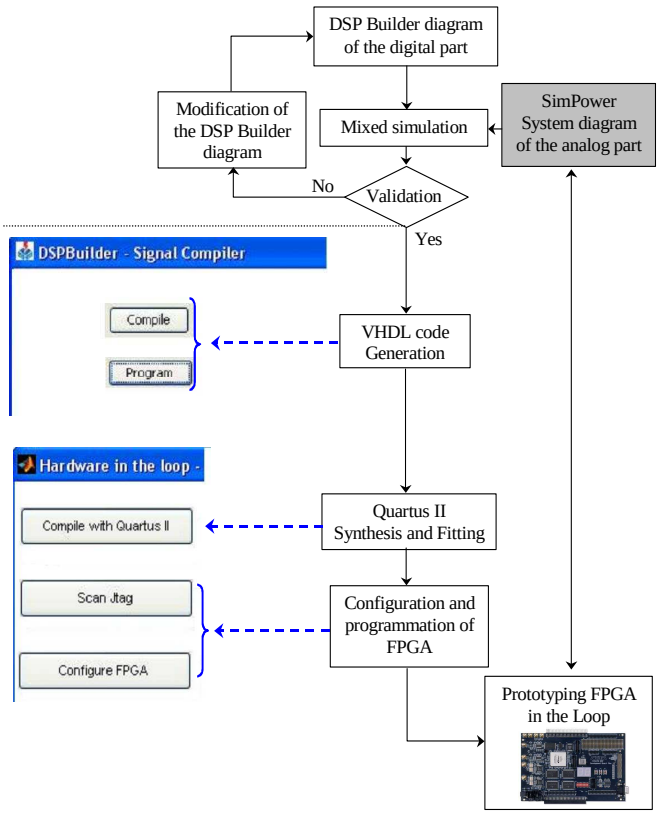

Figure 5. The steps of prototyping an FPGA in the loop

A. FPGA in the loop prototyping for the RM method

For this method of EIS measurement, we have used voltage and current measurement blocks and RLC blocks from the SimPower System library in order to simulate the dipole. These components constitute the analogue part of the system (Figure 6). The digital part contains two rectifiers, two low-pass filters, one divider and one direct digital synthesizer (DDS) to generate the sinusoidal signal with frequency sweeping.

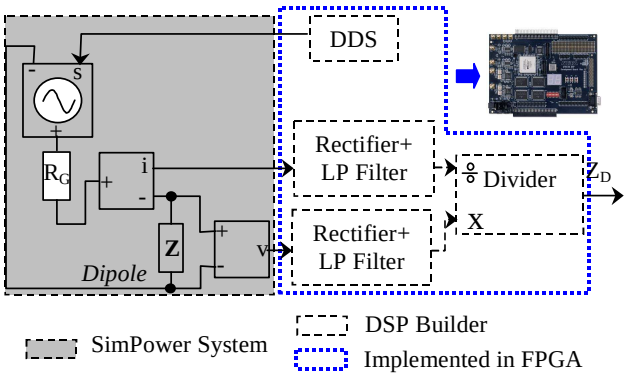

Figure 6. HIL scheme of the radiometric method

B. FPGA in the loop prototyping for the FVC method

Here, we don't need a current measurement, we only use the voltage V_D of the dipole in order to regulate it at $V_G/2$ by feedback control (Figure 7). This choice allows to have the best sensibility $\frac{dV_D}{d|Z|}$.

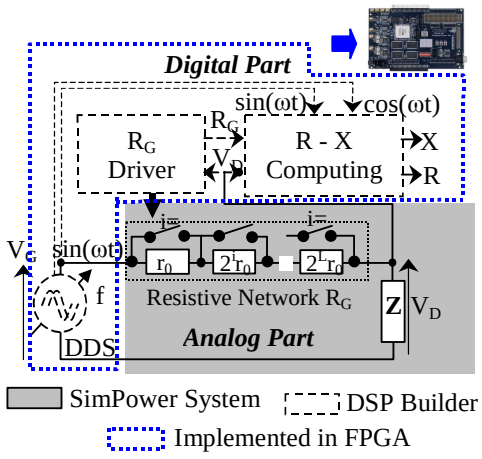

Figure 7. HIL scheme of the FVC method

C. *FPGA in the loop prototyping for the APM method.*

In this method, we must measure the voltage and the current of the tested dipole. The excitation signal is a white noise whose correlation time is T_c (Figure 8).

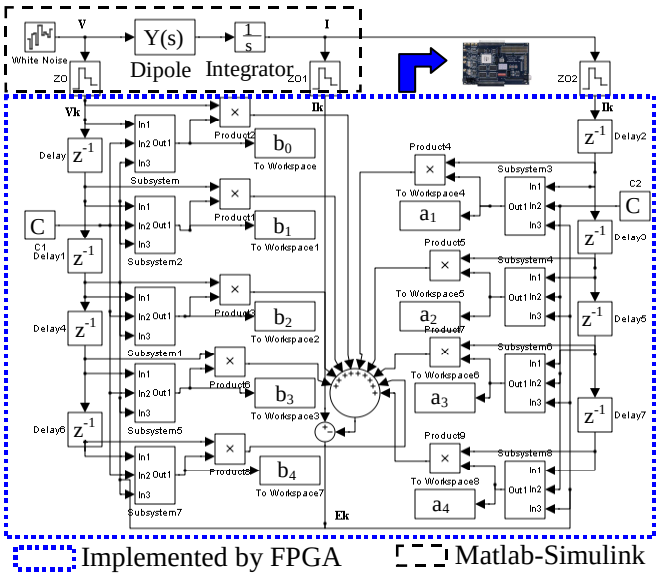

Figure 8. HIL scheme of the adaptive parametric modelisation

The coefficients a_i and b_j are updated using the gradient algorithm

$$b_j(k) = b_j(k-1) + C_1 V_{k-j} E_k \quad \text{for } 0 \le j \le 4 \qquad (6)$$

$$a_i(k) = a_i(k-1) + C_2 I_{k-i} E_k \quad \text{for } 1 \le i \le 4 \qquad (7)$$

where C_1 and C_2 are the adaptation constants
Figure 9 shows the subsystem diagram for the computation of the coefficients.

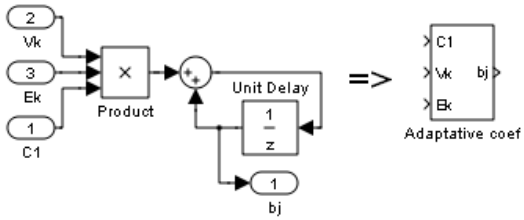

Figure 9. Adaptive coefficient subsystem

IV. RESULTS

A. *Range of frequency analysis*

The Stratix II allows to use a sampling frequency up to 100 MHz. The DDS synthesiser defines the frequency range of analysis. The structure we have adopted, can generate a sine excitation from DC to 5 MHz.

B. *Test of the three methods - Comparison*

The three methods RM, FVC and APM are used to analyse the impedance Z of a BVD structure corresponding to the dipole. The components values are given in Table I.

TABLE I. VALUES OF THE BVD COMPONENTS

L_1 (mH)	C_1 (nF)	R_1 (kΩ)	C_0 (nF)
486.4	1.1	2	4.64

These values correspond to an audio buzzer (7 kHz piezoelectric diaphragm of Murata Company).
The impedance is analysed in the range [5 kHz - 10 kHz], where the electric resonance area of the dipole is located. The RM and FVC methods use a sweeping rate of 91.7 kHz/s. Figures 10 and 11 represent the estimation curves of the real and imaginary parts (R and X) of Z obtained by each method. The curves are compared with the theoretical values R_{TH} and X_{TH} of the BVD impedance.

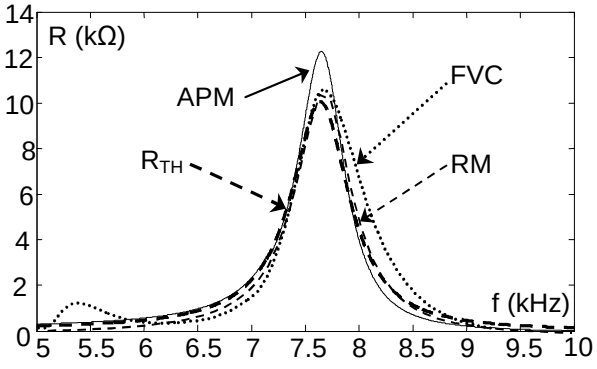

Figure 10. Real part of Z estimated by the three methods

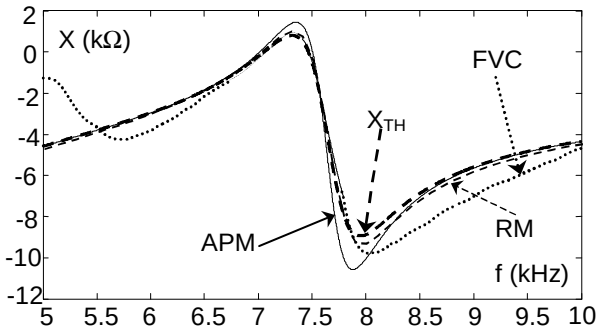

Figure 11. Imaginary part of Z estimated by the three methods

Table II summarizes the main characteristics of these measures. The accuracy is determined by comparison with the theoretical values.

TABLE II. ACCURACY AND DURATION OF THE MEASUREMENT OF Z

	Accuracy (at resonance peak)	Aanlysis duration
RM	99 %	54.5 ms
FVC	97 %	54.5 ms
APM	82 %	200 ms

C. Discussion

In this test, the RM method presents the best results. However, this method has important practical limitations.
A change in the calibre of R_S is necessary if we want to maintain a sufficient signal/noise ratio over a large dynamic range of Z. The dipole should not be grounded, this is not always possible in many situations. The FVC method allows to solve the previous limitations. In addition, the modulus of Z can be estimated from R_G. The feedback control must be stable and the analogue interface (digital resistive network) is more complicated.

The APM method is difficult to be implemented, because a setup phase must be performed. It requires to know " a priori" the dipole model in order to choose correctly the order N of the adaptive filter, the spectral density (1/Tc) of the white noise and the sampling frequency f_S

The convergence of the algorithm is achieved in practice by researching a compromise between these parameters. In our test, the best results are obtained with N = 4, $T_C = 10^{-5}$ s and $f_S = 3.10^5$ Hz.

The analysis time is directly related to the time constant of adaptation, in our case the analysis time is about 0.2 s. The impedance measurement errors are generally low but still significant near the resonance peak. When all adjustments are made, this method becomes very interesting because it provides a reference model for instantly monitoring the changes in characteristics of the tested dipole.

V. CONCLUSION

Three methods for impedance analysis that are implementable on an FPGA target were presented. The traditional ratiometric method is the simplest but requires in practice a change of range for the current measuring shunt and does not allow a grounded transducer. The 2^{th} method is an approach by automatic control of the series resistance to match the one of the transducer. This method allows the connection of the transducer to the ground without using an instrumentation amplifier. The last method is based on the parametric estimation of a model. The order of magnitude of the response time is 0.2. This method allows the determination of the impedance for any real-valued frequency thanks to the analytic model. In addition, the estimated adaptive filter model can be compared to a reference model in order to detect any drift in the transducer. However, this approach requires an "a priori" knowledge of the impedance type and a source of white noise. The presented methods were all implemented in an FPGA and some measurement results are given. A modified parametric estimation method based on the use of a pseudorandom binary sequences is under investigation.

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