



Event-Driven Based CMOS Interface for Magnetic Sensing

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Abstract—An Event-Driven (ED) approach to magnetic sensing is proposed in this paper, utilizing a Selective Change-Driven (SCD) topology and Giant Magnetoresistance (GMR) sensors. The authors developed a 1×8 linear magnetic sensor vector designed for applications such as particle tracking. The system is implemented in standard Complementary Metal-Oxide Semiconductor (CMOS) mixed-signal TSMC 180 nm technology. We are presenting here a preliminary characterization by means of standard Cadence/Virtuoso simulations, including synthetic results from flowing-particle modeling. Unlike conventional frame-based systems, this SCD-based architecture expands the state of the art by performing hardware-level data filtering, drastically reducing data redundancy and power consumption. This makes the system particularly suitable for real-time applications such as high-speed particle sorting or low-latency biomagnetic monitoring, where efficient data throughput is critical.

Keywords—Event-Driven (ED); Resistive Sensors; Giant Magnetoresistance (GMR); Selective-Change-Driven (SCD).

I. INTRODUCTION

In general terms, the neuromorphic approach can be understood as the reformulation of classical computing systems into architectures and topologies that attempt to mimic the behavior of the human brain [1]. It involves mimicking biological neurons with artificial equivalents. Unlike classic sensors that require post-sensing processing, bio-inspired systems respond directly to events, integrating perception and cognition within their topology. The aim of neuromorphic-inspired sensors is to create systems capable of generating a final response to an event by implementing the combined functions of perception and cognition in their topology. In this sense, Event-Driven (ED) sensors, also called Address Event Representation (AER) sensors, show clear advantages when compared with conventional sensors, in those scenarios where high speed or limited bandwidth is a must. This is of particular interest for vision sensors. In these architectures, the basic nodes (or pixels) consist of a photoreceptor (commonly a photodiode) together with the electronics (comparators, amplifiers and addressing management) required for adequately identifying and ‘addressing’ the proper triggered pixels. A particular strategy within AER vision sensors is the Selective Change Driven (SCD) approach [2]. In SCD systems, events are collected at the time they are produced, orderly chosen according to the magnitude of their change. For implementing such a strategy in silicon, some memory elements must be included in each pixel (commonly capacitors), as well as a specific selection circuit (such as Winner-Take-All, WTA, or similar). The use of SCD schemes have traditionally focused

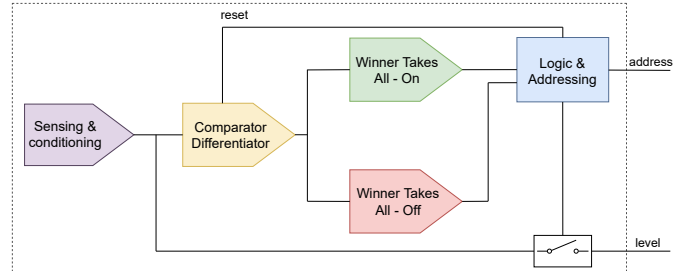


Figure 1. GMR Node scheme.

on movement detection and analysis [3], but the concept can be extended to many vision applications.

The Event-Driven concept is not limited to vision sensors [4], in fact, successful AER approaches have been reported for artificial cochleae [5] and magnetostrictive tactile sensors [6]. In both cases, a unique sensor (a microphone and a mechanical sensor) is considered. In addition, bio-inspiration could also be applied to sensing arrays not having counterparts within the human sensory systems, such as Ion-Sensitive Field Effect Transistors (ISFET) sensors [7], piezoresistive sensors [8], or Giant Magnetoresistance (GMR) sensors [9]. For implementing these proposals, integrable sensing elements should be used, replacing the function of the photodiodes.

We propose to apply a neuromorphic approach to magnetic sensing. As a test bench, we have developed a 1×8 linear magnetic sensor having an SCD topology together with GMR sensors, implemented in standard CMOS mixed-signal TSMC 180 nm technology. While the current version utilizes external GMR connections for initial characterization, the architecture is designed for future monolithic integration where sensors will be deposited directly onto the chip. The rest of the paper is organized as follows: Section II describes the circuit topology and its specific functional blocks; Section III presents the validation results with both electrical pulses and magnetic particle modeling; and Section IV concludes the work and discusses future research directions.

II. CIRCUIT TOPOLOGY

The general scheme of a SCD node [3] is depicted in Figure 1. The current sensor signal level is continuously compared against a sampled and hold value from the last time that sensor in the array was read-out. The difference between the last read-out and current values are rectified and amplified by means of a circuit based on a couple of Operational Transconductance Amplifiers (OTA). The differences I_{diff} of all nodes in the array are compared among them to obtain a set of winners with the

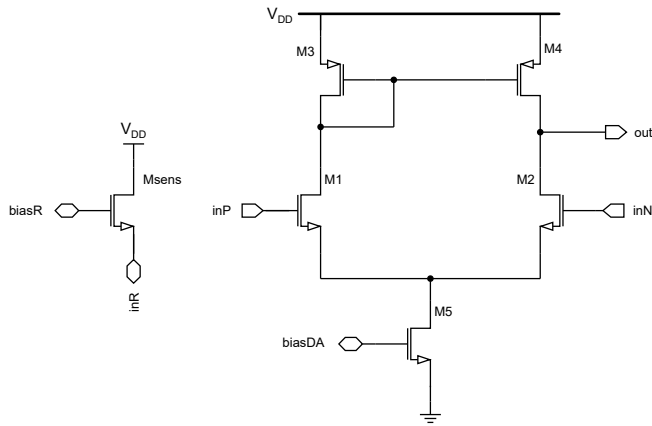


Figure 2. Analog input interface.

larger differences thanks to an analog Winner-Take-All (WTA) circuit. The distributed logic digital circuits take just one single winner from the set of winners. All this process takes place at each read-out clock cycle, ensuring that each access to the chip yields the output of the sensor that have undergone the largest change, since the last time that specific sensor of the array was read out. A detailed description can be found in [3].

A. Sensing and Conditioning

A significant contribution of this work is the sensing and conditioning block. Here, these pixels, commonly based on photodiodes are substituted by magnetic ones, based on GMR sensing elements.

The analog front-end is shown in Figure 2. It is based on a conventional current source and a differential amplifier with adjustable transconductance through the *biasDA* terminal. In this configuration, the architecture implements a reference by performing a global averaging of the sum of all sensors. This generates a dynamic baseline that is compared against the signal of the selected GMR element. This strategy enables the device to amplify local magnetic anomalies relative to the vector's mean, effectively canceling background magnetic fields.

B. Comparator / Differentiator

The identification of a winning resistive sensor within the array is determined by the transition of the *out* node in the capacitive-feedback comparator. In the architecture seen in Figure 3, a winner is defined as a sensor that experiences a magnetic field change significant enough to overcome a predefined threshold. Unlike traditional static comparators, this topology treats the *in* node as a dynamic input, where the capacitors C_1 and C_2 serve to decouple the DC magnetic baseline and focus exclusively on the voltage swing representative of GMR resistance fluctuations.

The operation is divided into a calibration (reset) phase and a sensing (competition) phase. During reset, the *winneg* signal activates the feedback transistor M_1 , biasing the inverter (formed by M_3 and M_2) at its high-gain trip point. This process stores the quiescent environmental magnetic state across the

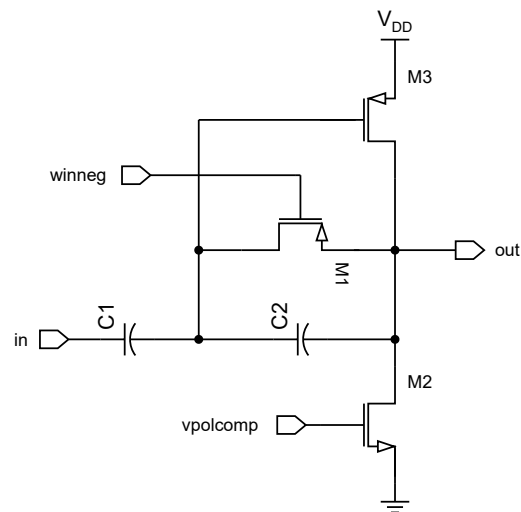


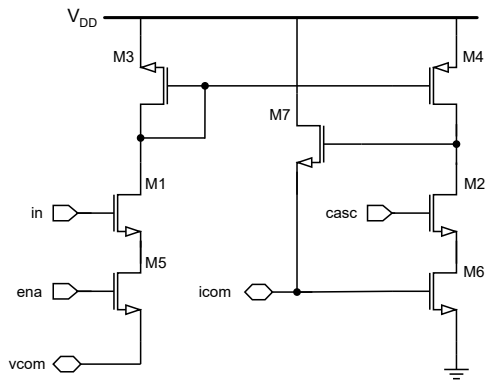
Figure 3. Comparator.

capacitors. When *winneg* is released, the comparator becomes highly sensitive to any local deviation (V_{in}) from this stored baseline. The sensitivity of the "winner" detection is controlled by *vpolcomp*, which regulates the bias current of the inverter stage, determining the speed and the minimum ΔV required to flip the *out* signal.

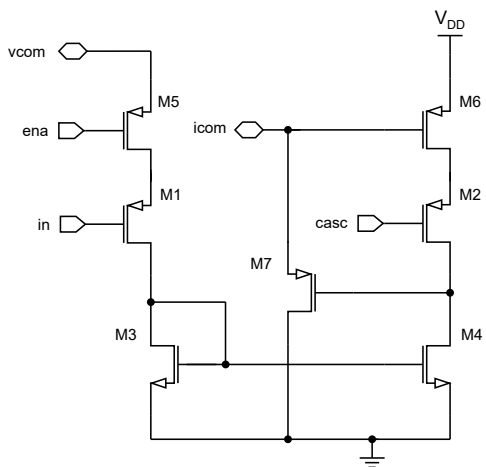
A sensor is identified as a potential winner when its *out* node transitions, signaling that the local magnetic transient has exceeded the threshold. Unlike conventional WTA architectures that employ a master-slave bias scheme to force the selection of at least one winner, this topology leverages the high open-loop gain of the M_3/M_2 stage to amplify small-scale anomalies relative to the global average. By adjusting the *vpolcomp* bias, the system can modify the effective gap required to trigger an event, allowing the sensor to distinguish between localized magnetic field of interest and broad environmental noise.

C. Winner-Take-All ON / Winner-Take-All OFF

The Winner-Take-All (WTA) circuit plays a key role in event-driven applications where a single element must be selected according to its relevance [10]. The signal is processed by two logic blocks: WTA_{on} and WTA_{off} circuits, shown in Figure 4, respectively. These blocks are responsible for the decision-making core of the device. They compare the transient signal against a dynamic global reference, ensuring that only the most significant positive or negative fluctuations result in an event trigger. The decision-making stage identifies significant transients in the magnetic signal by employing two complementary blocks. The WTA_{on} Figure 4 (a) block is responsible for detecting magnetic signal increases. It utilizes an N-channel Metal-Oxide-Semiconductor (NMOS)-core high-gain stage where the input voltage is converted into current. When a local signal experiences a positive excursion that exceeds the global baseline by a predefined threshold, the high open-loop gain of the stage drives the corresponding *win* node high, signaling a positive magnetic event. Conversely, the WTA_{off} block in Figure 4 (b) is designed to monitor



(a) WTA_{on} architecture.



(b) WTA_{off} architecture.

Figure 4. Combined view of the decision-making digital core: (a) ON-event and (b) OFF-event detection.

signal decreases using a P-channel Complementary-Metal-Oxide (PMOS)-core topology. By tracking the lowest signal values relative to the established baseline, the circuit triggers an output event for the specific sensor where the voltage drop is most pronounced. In both blocks, the sensitivity to these subtle anomalies is regulated by the bias current, allowing the system to distinguish localized magnetic signatures from broad environmental noise. This dual-path architecture provides separate channels for ON and OFF events, acting like a filter that ignores the constant background and only reacts when a sensor sees something different from its neighbors. By performing this comparison in the analog domain through current competition, the system avoids the power overhead of high-speed digital sampling, maintaining the energy efficiency required for low-power, high-speed applications.

D. Logic / Addressing

Output management is handled asynchronously, as shown in Figure 5, by asserting column requests (`colRQ`). The single-winner selection circuit grants access via the `colGR` signal, which simultaneously serves as a reset mechanism for the winning channel to initiate a new competition cycle. Once

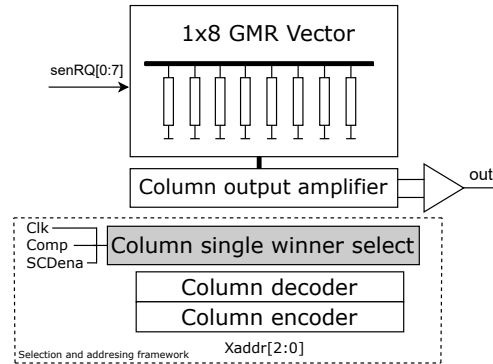


Figure 5. Sensor block with the digital single-winner selection.

arbitration is resolved, an Address Encoder translates the physical sensor position into a 3-bit digital word ($Xaddr[2:0]$). This process is synchronized by the `Clk` and `Comp` signals to prevent digital switching noise from coupling into the sensitive analog front-end. Finally, the infrastructure provides operational versatility through the `SCDena` signal, enabling a standard readout mode where a 3-to-8 decoder allows for individual sensor calibration against the global average.

III. VALIDATION

The validation of the proposed architecture is executed through a two-stage simulation process to verify the overall logic consistency and the system’s response to realistic magnetic stimuli. Initially, the sensing and conditioning blocks are subjected to idealized stimuli, just to characterize the fundamental behavior of the winner selection mechanism. Then, the system is integrated with a behavioral model of a magnetic particle environment, using the Magpylib library to simulate the trajectory of magnetized particles over the 1×8 sensor vector. The developed device has been tested by means of Cadence/Virtuoso/Spectre simulations, the golden standard in microelectronics design.

A. Excitation by Pulses

The first stage of validation focuses on the winner identification logic through a series of controlled transient injections. In this phase, the front-end is subjected to a series of calibrated square pulses applied sequentially to each sensing node. This approach is not intended to emulate the physical behavior of a magnetic particle, which produces a significantly different signal profile in reality. Instead, these square pulses serve as a deterministic electrical stimulus to verify the logic mapping of the competitive core. By triggering the sensors in a discrete, sequential order, the simulation confirms that the WTA_{on} and WTA_{off} architectures can correctly identify the winning channel within the 1×8 vector. Results are collected in Figure 6. These results validate the timing and response of the core, ensuring that no event collisions occur during the sequential identification of the winning channels.

B. Particle Tracking

Then, having in mind the subsequent application of magnetic particle tracking, a specific simulation experiment was designed.

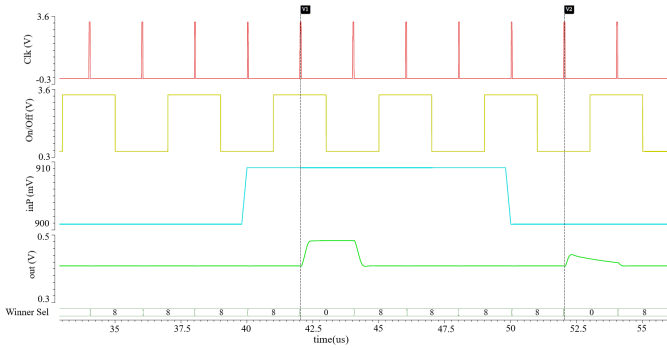


Figure 6. Excitation by pulses: System Clock ; WTA_{on} / WTA_{off} ; Input square stimuli ($V_{peak} = 10\text{ mV}$); Output response; Winner selection logic.

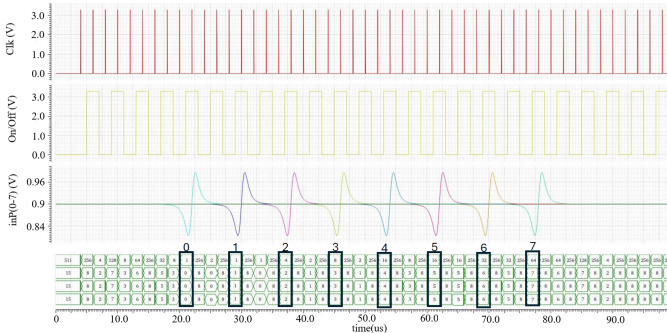


Figure 7. Response to a flowing particle through the 8 sensing elements.

Synthetic responses of magnetic microparticles flowing through a microfluidic channel were obtained using MagPyLib modeling. These data were used as excitation signals for the circuit. The results are collected in Figure 7. As observed, the system tracks the flow of the particles, identifying them individually.

IV. CONCLUSION AND FUTURE WORK

A neuromorphic interface for resistive sensors has been developed and validated. Cadence/Virtuoso/Spectre demonstrated both the proper function of the system and its capability of tracking and identifying individual magnetic microparticles. Future research directions will focus on the transition from simulation to physical prototyping. A primary objective is the execution of a tape-out in 180 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology to characterize the impact of thermal noise and substrate coupling on the sensitivity of the analog core under real operating conditions. Furthermore, we intend to quantify the system’s common-mode rejection capabilities; while GMR elements are naturally sensitive to ambient fields, the architecture uses the global average of the sensor vector as a dynamic reference; this allows the system to cancel out widespread environmental noise while detecting only the localized magnetic changes caused by a passing particle. Looking ahead, the architecture is intended to be scaled into two-dimensional ($N \times M$) arrays, which will necessitate the exploration of hierarchical Winner-Take-All (WTA) structures to manage higher event densities without compromising power efficiency. Finally, the integrated system will be validated within a microfluidic setup to assess its performance in

high-throughput particle sorting and biomagnetic monitoring applications.

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