Design of a High-speed CMOS Image Sensor with an Intelligent Digital Correlated Double Sampling and a Symmetrical 3-Input Comparator

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Abstract— **In order to improve the frame rate of a CMOS image sensor (CIS), a novel technique of correlated double sampling (CDS) and a symmetrical 3-input comparator are discussed. In the conventional digital CDS, a subtraction algorithm between the reset digital code and the pixel digital code has been normally adopted. Thus, it needs two ramps and takes a much more operating time, compared to that of analog CDS. In this paper, an intelligent digital CDS is proposed drastically to reduce the operating time. Further, a symmetrical 3-input comparator to implement the intelligent digital CDS is also described. A high speed CIS with the proposed CDS and a symmetrical 3-input comparator has been fabricated with Samsung 0.13um CIS technology. A high frame rate of 240fps is achieved at the VGA resolution of 640x480 with 39mW power consumption.**

Keywords—CMOS image sensor(CIS); one-ramp digital correlated double sampling; symmetrical 3-input comparator; subtraction algorithm.

I. INTRODUCTION

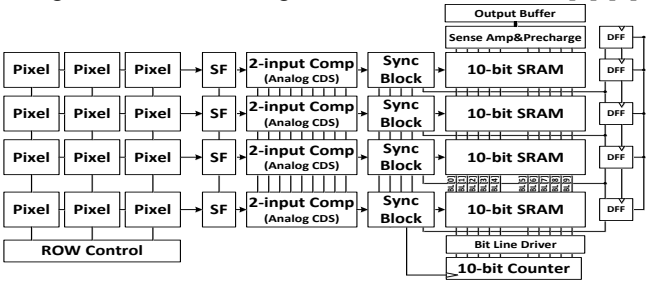
CMOS Image Sensors (CIS) are now widely used in many kinds of areas including digital cameras, camcorders, CCTV cameras, medical equipment, etc. In order to improve the image quality of CIS, research has focused on developing methods to reduce noise. In CIS, Fixed Pattern Noise (FPN) is a major factor causing the degradation of image quality. FPN is normally generated from the device mismatching errors of pixel circuits, such as threshold voltage variations of source follower, fluctuations of MOS transistor size, etc. To remove the errors, a few techniques of analog Correlated Double Sampling (CDS) have been reported [1][2]. However, it requires a large size of capacitor to enhance the accuracy. Further, it is difficult to have a high resolution image beyond 8-bit. Therefore, many CISs with a single-slope ADC use a digital CDS to reduce FPN [3]-[10]. In the digital CDS, FPN is normally eliminated by comparing the reset signal and the pixel signal through the two ramp signals. Generally, the length of the reset ramp signal is at least about a quarter of the pixel ramp signal. In other words, the A/D conversion time of digital CDS is much longer than that of analog CDS only. Even though the digital CDS has a high quality image, the operating speed is much lower than that of analog CDS. In this paper, to improve the speed of CIS, a single ramp signal is used. The contents of the papers are as follows. In Section II, the conventional CDS and a new CDS are discussed. The implementation of CIS and experimental results are described in Section III. Finally, the conclusions are summarized in Section IV.

II. CORRELATED DOUBLE SAMPLING (CDS)

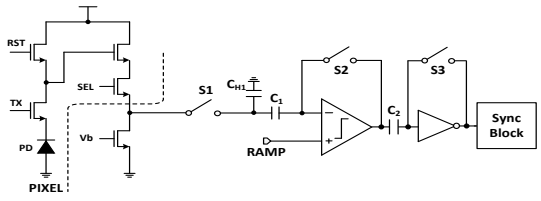
In order to understand the main idea of this paper, the principle of CDS is essential. After a conventional CDS is described, the proposed CDS technique will be discussed.

A. Conventional Two-ramps Digital CDS

Fig. 1 shows a conventional CIS with a single-slope ADC (SS-ADC). Fig. 1(a) shows the block diagram of a CIS with a column parallel ADC. Since it consists of many pixels, the pixel FPN can occur due to device mismatching errors. The pixel FPN conveys each output from the same light to the ADC in the form of another voltage. Moreover, the ADC in each column can also generate imbalance features, column FPN. Therefore, both the pixel FPN and the column FPN must be reduced and properly calibrated. In order to reduce the FPN, an SS-ADC with an analog CDS shown in Fig. 1(b) is widely used. The difference between the pixel signal voltage and the reset voltage is transferred into ADC [3]-[6].



(a)



(b)

Figure 1. Principle of a Conventional CMOS Image Sensor (CIS)
(a) Block Diagram (b) Circuit Diagram for a CDS

 ISBN: 978-1-61208-543-2

The analog CDS requires a large size of the capacitor to enhance the accuracy. Thus, a digital CDS is generally used with an analog CDS in order to reduce FPN. Fig. 2 shows the timing diagram of the conventional SS-ADC with a digital CDS. It compares the reset signal with the first ramp and the pixel signal with the second ramp. When comparing the reset signal, the counter executes a down count mode. When comparing pixel signal, the counter operates in the up count mode. In this case, the digital CDS can remove the FPN that cannot be removed with the analog CDS. However, the conversion time of digital CDS is increased because an additional ramp is needed at the SS-ADC, compared to that of analog CDS. Generally, the operation time to compare the reset signal with the ramp is about a quarter of the time to compare the pixel signal with the ramp. Therefore, the A/D conversion time of digital CDS is much longer than that of analog CDS only.

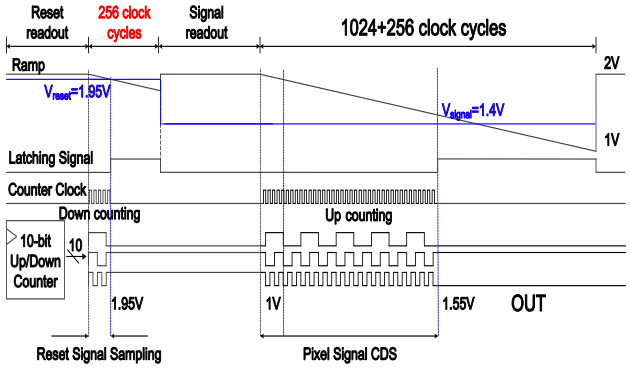


Figure 2. Timing Diagram of a Conventional Two-ramps Digital CDS

B. *Intelligent CDS*

Fig. 3 shows the principle of a SS-ADC with the proposed intelligent digital CDS. Fig. 3(a) shows the circuit diagram of a SS-ADC with the intelligent CDS. Instead of a conventional comparator, a symmetrical 3-input comparator performs an A/D conversion. In order to separate the voltage coming from the reset signal and the pixel signal, a holding capacitor and a DC blocking capacitor are used at each node, respectively. Fig. 3(b) shows the circuit diagram of 3-input comparator, and Fig. 3(c) shows the timing diagram of a SS-ADC. Since the reset signal and the pixel signal are stored separately through the operation of the intelligent CDS, only one ramp signal is enough to obtain a digital code even in a digital CDS. The procedure of Fig. 3(c) is as follows. In the region of A, the reset signal is stored at C_{H1} when S1 and S3 are ON, then the pixel signal is stored at C_{H2} when S2 and S4 are ON. Further, in Fig. 3(b), when S6 and S8 are ON, S7 and S9 are OFF, the 3-input comparator is now ready to start.

In the region of B, all the switches of Fig. 3(a), S1,S2,S3, and S4 are OFF. Then, the ramp is now starting down when S6 and S9 are ON, S7 and S8 are OFF in Fig. 3(b). Thus, the right side of 3-input comparator is at the state of equilibrium, and the left side of 3-input comparator amplifies the voltage difference between the ramp and the reset signal. The output voltage of 3-input comparator is easily obtained from the simple equation of a differential amplifier as follows.

$$V_{\text{out}} = G_m \; R_{out} \; \{(V_{RAMP} - V_{rst}) + (V_{sig} - V_{sig})\} \qquad (1)$$

where G_m is the input transconductance of 3-input comparator, R_{out} is the output impedance, respectively. At the end of region B, when the ramp signal and the reset signal are the same, the sync block becomes HIGH.

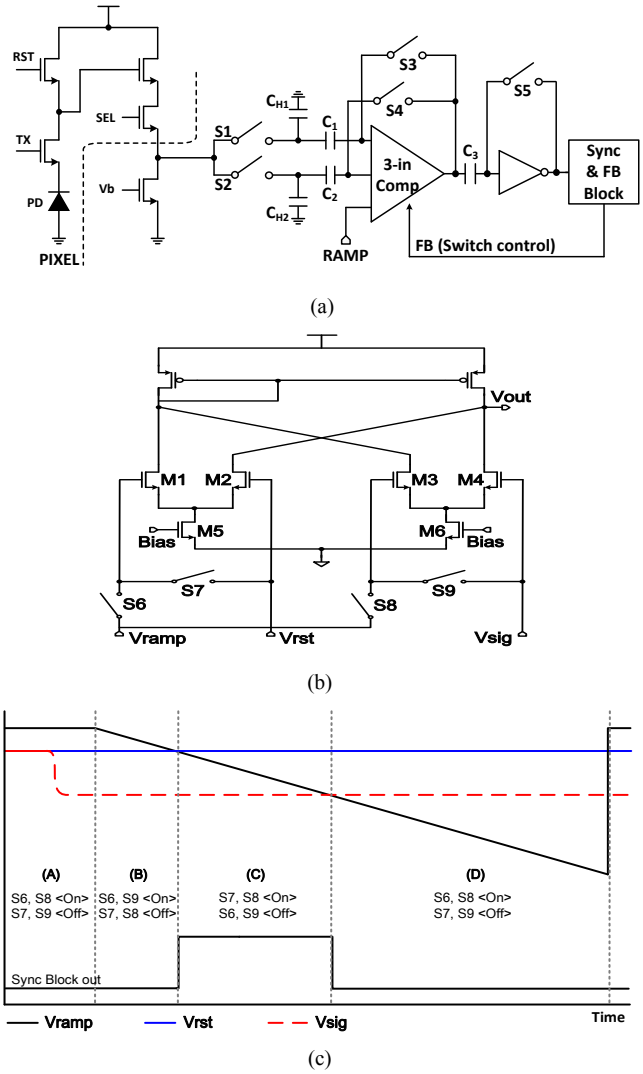


Figure 3. Principle of the Proposed CDS
(a) Circuit Diagram for an Intelligent one-ramp CDS
(b) Circuit Diagram for a Symmetrical 3-input Comparator
(c) Timing Diagram for the Switch Operation Procedure

In the region of C, the counter is starting to count, when S7 and S8 are ON, S6 and S9 are OFF, in Fig. 3(b). Thus, the left side of 3-input comparator is at the state of equilibrium, and

the right side of 3-input comparator amplifies the voltage difference between the ramp and the pixel signal. At this time, the output voltage of 3-input comparator is also easily obtained as follows.

$$V_{out} = G_m \; R_{out} \; \{(V_{rst} - V_{rst}) + (V_{RAMP} - V_{sig})\} \qquad (2)$$

At the end of region C, when the ramp signal and the pixel signal are the same, the sync block becomes LOW and the counter stops. Therefore, the digital code which corresponds to the difference of reset signal and pixel signal can be calculated. The operating time of the intelligent CDS technique can be reduced drastically compared to that of a conventional CDS, because only one ramp is used. In the region of D, all the functions of 3-input comparator stop and it returns to the initial state, when S6 and S8 are ON, S7 and S9 are OFF. Thus, the 3-input comparator is like a symmetrical amplifier.

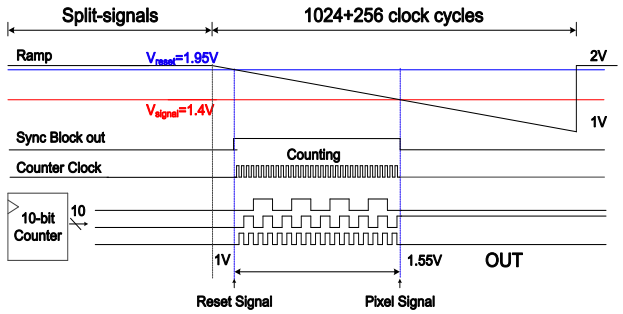


Figure 4. Timing Diagram of the Proposed Intelligent One-ramp CDS

Fig. 4 shows the timing diagram of a SS-ADC with the proposed intelligent digital CDS. Compared to those of Fig. 2, it does not need the section that compares the reset signal with the ramp. In case of 10-bit SS-ADC, at least, the time of 256 cycles is saved. Therefore, the operating time of the proposed technique is much faster than that of the conventional one.

III. Experimental Results

Fig. 5 shows the block diagram of a CIS with a 10-bit SS-ADC and the intelligent digital CDS. The CIS is based on a column-parallel ADC structure with a VGA resolution of 640x480, and each pixel uses a 4-TR APS with a size of 5.6 µm x 5.6 µm. As mentioned above, the CIS uses the intelligent digital CDS, which compares the reset signal and the pixel signal with only one ramp signal. Thereby, this new method facilitates the digital block with a simple counter. Because of a simple counter, the chip area of digital block is drastically reduced, compared to that of the conventional one.

Table I shows the comparison of chip size per one column. With 0.13µm Samsung CIS technology, the total layout size of the proposed one per one column is 470 µm, while that of a conventional one is 450 µm. Thus, the total chip area of the proposed CIS is not so much bigger than that of the conventional one, even though the intelligent digital CDS technique uses the large size of capacitors and differential mode at the analog block.

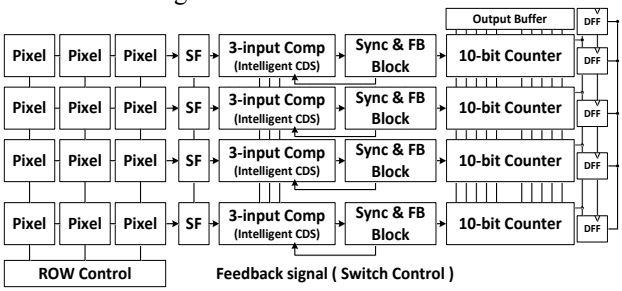
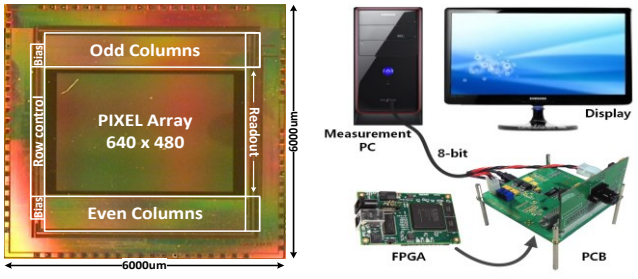


Figure 5. Block Diagram of the CIS with an Intelligent CDS

TABLE I. CHIP SIZE COMPARISON PER ONE COLUMN

	Counter	Capacitor	total
Conventional one (10-bit)	330 µm (up-down)	120 µm (1.5pF)	450 µm
This work (10-bit)	230 µm (normal)	240 µm (3pF)	470 µm
Column pitch = 11.2 µm C1, C2 = 500fF CH1, CH2 = 1pF Unit capacitor = 50fF (L=7 µm, W=4 µm)			

Fig. 6(a) shows the chip microphotograph of the CIS fabricated with Samsung 0.13 µm 1P4M CIS technology. The chip size is 6 mm x 6 mm, and the pixel array conforms to the VGA resolution (640x480). Fig. 6(b) shows the configuration of the measurement system which is comprised of a board that contains the Xilinx-XEM 3050 FPGA and a test board of the prototype CIS chip with a chip-on-board (COB). The prototype of CIS chip shown in Fig. 6(a) is controlled by the control signals through an external FPGA. Using such a configuration allows us to establish various test environments for the image sensor, to verify the performance of the CIS and to check the results of various features. The FPGA plays a role in generating the control signal for the measurements, receiving the output data from the image sensor, and delivering the results to the PC through the USB interface. The transmitted data are handled in the PC, where the real image is processed.



(a) (b)

Figure 6. Chip Photo and Measurement (a)Chip Microphotograph of the CIS with Samsung 0.13µm CIS (b) Configuration of the Measurement Systems

Figure 7. Measured VGA Sample Image

Fig. 7 shows the VGA sample image with the condition of 10-bit resolution. The method achieves frame rates of 240 fps at a main clock speed of 100MHz. The image shows high quality.

IV. CONCLUSION

A high speed CMOS image sensor with an intelligent digital CDS technique was discussed. In order to raise the operating speed of the conventional CIS, we described a new symmetrical 3-input comparator and an intelligent digital CDS that compares the reset signal and the pixel signal using only one ramp. With the technique, the operating speed of the proposed CIS was much faster than that of the conventional one, because only one ramp was adopted. The prototype chip has been fabricated with the Samsung 0.13 μm 1P4M CIS technology. The resolution of the CMOS image sensor was the VGA specifications of 640x480, and the pixel size was 5.6 μm with the 4-TR APS. The conversion time of the designed 10-bit SS-ADC using the intelligent digital CDS satisfied the 16-μs at a main clock speed of 100MHz. The frame rate of the CIS was of 240 fps at the main clock speed of 100MSPS. Table II shows the comparison results of the proposed CDS with the previously published works. The proposed CIS has the advantage of high speed frame rate, compared to other ones at the same condition.

TABLE II PERFORMANCE COMPARISON

Reference	[7]	[8]	[9]	[10]	This work
Technology	0.13um	0.18um	0.13um	0.18um	0.13um
CDS	Analog	Digital	Digital	Analog	Digital
ADC Type	Sigma-delta	Single-slope	Single-slope	TS Cyclic	Single-slope
ADC Bit	11-bit	10&12-bit,	12&14-bit	12-bit	10-bit
Pixel Array	1600x1300	1920 x 1440	8192 x 2160	76804320	640 x 480
Frame Rate	120	180 (10-bit)	120 (12-bit)	120	240
Power [mW]	44.1	580	3000	2500	39.2

In the future, we have a plan to raise the pixel array up to UHD resolution (3840 x 2160), the frame rate up to 360, and the ADC resolution up to 14-bit. Further, a two-step single-slope ADC with the proposed CDS technique will also be studied.

ACKNOWLEDGMENT

This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education, Science and Technology(2015R1A1A2001455).

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 ISBN: 978-1-61208-543-2