Multi-Stage Threshold Decoding of High Rate Convolutional Codes for Optical Communications

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***Abstract*— For 100 Gb/s optical transport network, researchers are searching a suitable error correction coding scheme that can provide coding gain more than 10 dB at the bit error rate less than 10^{-12}, provided that the redundancy does not exceed 20 percent. This paper presents a least complex error correction coding scheme based on iterative threshold decoding called multi-stage threshold decoding with difference register (MTD) for the 100 Gb/s optical transport network. High rate (code rate 0.8) self-orthogonal convolutional codes are considered. The MTD achieves lower bound error performance of maximum likelihood decoding at higher bit energy to noise density ratio. The codes with orthogonal checking 10 and larger satisfy the requirements of 100 Gb/s optical transport network. The bit error rate of MTD with parity check decoding becomes less than 1/100 times in the error floor region compared to ordinary MTD. The MTD based decoding with parity check decoding for the code with orthogonal checking 12 produces 10.60 dB coding gain at the bit error rate 10^{-15}. The coding gain further improves 0.25 dB in the waterfall region by using 2-step decoding.**

***Keywords*- threshold decoding, convolutional codes, self-orthogonal codes, optical transport network.**

I. Introduction

Forward error correction codes (FECs) play an important role in the newly considered optical transport network (OTN) with network capacity 100 Gb/s. International telecommunications union (ITU–T) primarily consider the Reed–Solomon (RS) codes as FEC [1] in the G.975 recommendation. It considers RS(255,239) code with 7% redundancy. The expected coding gain is 4 to 5 dB per fibre span, but it is not sufficient for 100 Gb/s OTN operation.

There have been a number of proposals for higher gain FECs; one is iterated code based on (1023,992,8) BCH code claimed as the best choice as FEC for 100 Gb/s OTN system that produced the coding gain around 9.3 dB at the output bit error rate 10^{-15} [2]. However, more than 10 dB coding gain is required for the 100 Gb/s OTN system at the output bit error rate less than 10^{-12} with the maximum allowable redundancy 20% [3].

Most of the codes proposed as FECs for the 100 Gb/s OTN system are block codes and their hard decoding technique is considered. The low density parity check (LDPC) codes with soft decoding have been adopted for the 10 Gb/s Ethernet (IEEE 803.3an), WiFi (IEEE 802.11n), WiMAX (IEEE 802.16e) wireless LAN standards and are being considered for a range of application areas, from optical transport network to digital storage [3][4]. An LDPC code concatenated with RS code may be the main candidate as FEC for the 100 Gb/s.

However, the convolutional codes for optical communications are rarely shown as FEC due to their latency and error floor [3]. This paper presents a least complex decoding method for self-orthogonal convolutional codes that can reduce the decoding latency by parallel processing and improves the error floor performance with concatenation of parity check (PC) decoding that fulfills the requirements of 100 Gb/s optical transport network. Moreover, implementation of convolutional encoding is simpler than the encoding of block codes. In addition, the proposed decoding is mainly based on the several shift registers and high speed decoding is expected.

The proposed decoding method is an iterative bit flipping decoding based on the threshold decoding [5] called multi-stage threshold decoding with difference register (MTD) which, is treated as MTD-DR in [6]. Similar decoding idea, called multi threshold decoding, is shown in [7][8]. They did not show why and how the threshold value changes in each iterations. Moreover, necessary information to rebuild the system is absent.

The iterative decoding based on min-sum decoding, instead of bit flipping, for the self-doubly orthogonal codes is shown in [9]. The decoding decision depends on the log likelihood ratio (LLR) of a posteriori probability and updates it after decoding each information bit. Moreover, the LLR increases the decoding complexity. Instead of LLR value, MTD uses a set of magnitude of the received signals for decoding an information bit and updates the binary value of the related signals by the flipping decision. The decoding latency, however, depends on the span of information shift register in the encoder and the average number of iterations.

The lower bound of maximum likelihood (ML) decoding has been presented in [10] and it is seen that, MTD achieves lower bound of ML decoding performance at higher bit energy to noise density ratio, E_b/N_0. That means, MTD gives optimum decoding performance of a given code and the error floor experiences due to the number of orthogonal checking of the code. Moreover, if we allow maximum 1.5% more redundancy by concatenating parity check code, the bit error performance in the error floor becomes less than 1/100 times

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compared to conventional MTD.

Lower the orthogonal checking of a code gives better error performance in the waterfall region. In this context, the 2-step decoding, 1st decoding step uses a part of parity bit sequences (lower number of orthogonal checking) and 2nd decoding step uses all the parity sequences (all the orthogonal checking of the code), has been presented for rate 1/2 codes and the decoding scheme produces more coding gain in the waterfall region [10].

Rest of the paper is arranged as follows. Section II gives the concepts of iterative threshold decoding with difference register. In this section, we give soft decoding algorithms. Section III gives high rate self orthogonal convolutional codes. Section IV discusses about 2-step decoding that produces additional coding gain in the waterfall region. Section V gives an idea for high speed decoding that reduces total decoding latency. Section VI gives the bit error performance of decoding schemes. Section VII gives the decoding complexity in terms of basic operations (e.g., modulo 2 summation, real number summation, minimum value searching etc.) and compared with the complexity of min-sum based decoding scheme and Section VIII concludes this paper.

II. Decoding Concept

This section provides decoding algorithms of self-orthogonal convolutional codes (SOCCs) on the basis of threshold decoding. Soft decoding algorithms are also given.

A. Multi-Stage Threshold Decoding

A systematic SOCC with the rate R=1/2, shift register length M and the number of orthogonal checking J is considered. The orthogonal checking is denoted by the tap connection in the shift register of the encoder and the code is determined by its connection positions. Let g_a, a=1, 2, ..., J, be a tap connection position in the shift register involving to generate a parity bit sequence. The minimum Hamming distance (d_{min}=J + 1) depends on the orthogonal checking of the codes [11]. The dotted section in Figure 1 shows an encoder of the SOCC with R=1/2, M=8, J=3, d_{min}=J+1=4. The information bit sequence $\mathbf{u}$=$\{u_0, u_1, \ldots\}$ is fed to the encoder and generates a parity bit sequence $\mathbf{v}$=$\{v_0, v_1, \ldots\}$. The i-th parity bit is determined by

$$v_i = \sum_{a=1}^{J} \oplus\, u_{i-g_a},\ \ i = 0, 1, \ldots \tag{1}$$

where $\oplus$ is the modulo-2 addition operator in this paper. The information and the parity bit sequences make a systematic codeword and is transmitted through the additive white Gaussian noise (AWGN) channel as BPSK signals. The tail biting termination is used.

Let $\mathbf{y}_u \triangleq \{y_0^u, y_1^u, \ldots\}$ be received information signals, $\mathbf{y}_v \triangleq \{y_0^v, y_1^v, \ldots\}$ be received parity signals, $\tilde{\mathbf{u}} \triangleq \{\tilde{u}_0, \tilde{u}_1, \ldots\}$ be hard decision information bits and $\tilde{\mathbf{v}} \triangleq \{\tilde{v}_0, \tilde{v}_1, \ldots\}$ be hard decision parity bits. The threshold decoding generates a syndrome bit sequence by the help of received information and parity bit sequences. The i-th syndrome bit is given by

$$s_i = \tilde{v}_i \oplus \sum_{a=1}^{J} \oplus\, \tilde{u}_{i-g_a} \tag{2}$$

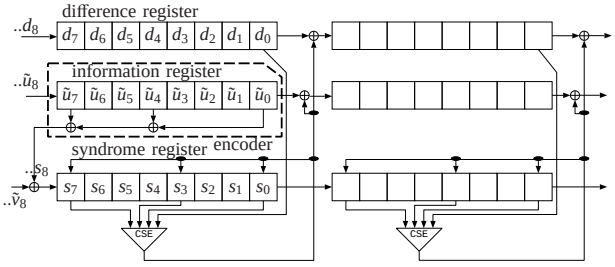

Fig. 1. Multi-stage threshold decoder for the Self-orthogonal convolutional code with m=n=1, J=3, M=8 and R=1/2. CSE means checksum-threshold element.

Figure 1 shows a hard decision multi-stage threshold decoding scheme. The decoder contains an extra shift register against an information shift register called difference register (DR). The DR holds pairwise difference between the received and decoded information bits. At the initial stage, DR contains all zero bits.

The soft decoding MTD (SMTD) calculates the checksum value from a set of the magnitude of parity signals related to the information signal under decoding and the magnitude of the information signal itself [6]. In this case, the checksum value L_j is calculates by

$$L_j = \sum_{a=1}^{J} w_{j+g_a} \tilde{x}_{j+g_a}^v + w_{d_j} \tilde{x}_j^u \tag{3}$$

where w_k represents the magnitude of the signal y_k^v and w_{d_k} represents the magnitude of the signal y_k^u and the value $\tilde{x}_k^u \triangleq (1\text{-}2d_k)$ and the value $\tilde{x}_k^v \triangleq (1\text{-}2s_k)$. If the checksum value becomes negative, i.e., $L_j < 0$, the decoding is done by flipping the information bit. At the same time, related DR and syndrome bits are inverted. After flipping each information bit, the Euclidean distance between the received signals and the decoded codeword, where bits are represented by +1 or -1, becomes shorter [6].

B. Weighted Bit Flipping Multi-Stage Threshold Decoding

The weighted bit flipping (WBF) algorithm is proposed for decoding low density parity check (LDPC) codes [12]. By the similar way, the weighted bit flipping MTD (WMTD) explores the value w_k as the minimum magnitude among the received signals related to the syndrome bit s_k. Then, the checksum value is calculated by using (3) and the decoding decision is made accordingly.

C. Combined Soft Decoding Multi-Stage Threshold Decoding with Feedback

The individual error performance of SMTD and WMTD is not attractive. The concatenation of WMTD and SMTD called combined soft decoding MTD with feedback (CMTDF) produces attractive error performance. Figure 2 shows the schematic diagram of CMTDF where weighted bit flipping MTD works first and terminates its decoding when no information bit is flipped or by the maximum number of iterations. Then SMTD works by the same manner and feedback again.

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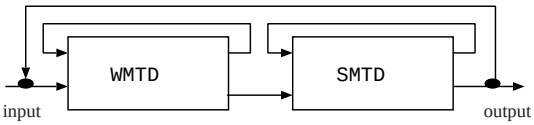

Fig. 2. Schematic diagram of combined soft decoding multi-stage threshold decoding.

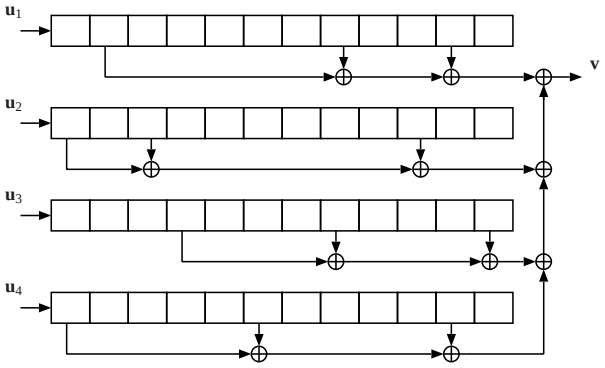

Fig. 3. Self-orthogonal convolutional code type 1 with m=4, J=3, M=12 and code rate R=4/5=80%.

If no information bit is flipped in both component decoders or completed maximum number of iterations, final output is made.

D. Combined Soft Decoding Multi-Stage Threshold Decoding with Parity Check Decoding

A parity check decoding is serially concatenated with CMTDF. The CMTDF with parity check (PC) decoding achieves attractive bit error performance in the error floor region [6]. The PC encoder adds a parity check bit in the information bit stream after each n_1 bits. When parity check is not satisfied, the PC decoder searches the minimum absolute checksum value, provided by the CMTDF after the final iteration, related to each n_1 information bits. The decoding is done by flipping the information bit related to the minimum absolute checksum value. In this paper n_1 is set to 50 bits.

III. High Rate Self-Orthogonal Convolutional codes

This section gives high rate (code rate 80%) SOCCs that can produce redundancy around 20%. The SOCC is categorized into two types: 1) the self-orthogonal convolutional codes type 1 and 2) the self-orthogonal convolutional codes type 2 [6].

A. Self-Orthogonal Convolutional Code Type 1

The self-orthogonal convolutional code type 1 (SOCC:TP1) generates only one parity bit sequence by using $m \geq 1$ information bit sequences. That means, the encoder of SOCC:TP1 has m information shift registers and each shift register contains one set of tap connection with J_k $(k = 1, 2, ..., m)$ elements and the m tap connection sets make a SOCC. The orthogonal checking distribution of this code is defined by $\{J_1; J_2; \ldots; J_m\}$. Figure 3 shows an encoder of such code with m=4, $J = J_1 = J_2 = J_3 = J_4 = 3$ and the shift register length M=12. The code rate of this code is R=$m/(m+1)$ and the code length becomes N=$K(m+1)$, where K is the number of information bits in each sequence. The orthogonal checking distribution of this code is $\{3; 3; 3; 3\}$. Unfortunately, MTD makes an unavoidable error grouping in the decoded information bit sequences for this type of code and degrades the error performance [6].

B. Self-Orthogonal Convolutional Code Type 2

The self-orthogonal convolutional code type 2 (SOCC:TP2) generates $n \geq 2$ parity bit sequences by using $m \geq 1$ information bit sequences. i.e., an encoder of SOCC:TP2 has m information shift registers and each shift register contains n tap connection sets with $J_p^{(k)}$ $(k = 1, 2, ..., m,\ p = 1, 2, ..., n)$ elements and the $m \times n$ tap connection sets make the SOCC. The orthogonal checking distribution of the code is defined by $\{J_1^{(1)}, J_2^{(1)}, ..., J_n^{(1)}; J_1^{(2)}, J_2^{(2)}, ..., J_n^{(2)}; ...; J_1^{(m)}, J_2^{(m)}, ..., J_n^{(m)}\}$. Figure 4 shows an encoder of SOCC:TP2 with m=12, $n = 3$, $J = \sum_{p=1}^{3} J_p^{(k)} = 2 + 2 + 2 = 6$ and the shift register length M=12. The code rate of this code is R=$m/(m+n)$= 12/15. The orthogonal checking distribution of this code is $\{2, 2, 2; 2, 2, 2; 2, 2, 2; 2, 2, 2; 2, 2, 2; 2, 2, 2; 2, 2, 2; 2, 2, 2; 2, 2, 2;$- $2, 2, 2; 2, 2, 2; 2, 2, 2\}$. The SOCC:TP2 successfully breaks down the error groping and produces better error performance by the MTD compared to the SOCC:TP1 [6]. Therefore, this paper only consider the SOCC:TP2 for the encoding schemes.

IV. 2-Step Decoding

As is described in Section VI, MTD based decoding achieves lower bound of ML decoding performance at higher E_b/N_0. That means, error floor is realized due to the minimum Hamming distance $(J + 1)$ of the code. On the other hand, larger the J of a code shifts the waterfall error performance to higher E_b/N_0 and opposite situation is occurred due to smaller J value [6]. In this context, a 2-step decoding (2SD) has been proposed [10]. At the 1st decoding step, MTD uses a part of parity check bits so that decoding is done by approximately 50% of J of the code and the 2nd decoding step works just like an MTD. The code is constructed such a way that, one parity sequence is to be generated by approximately $J_s \approx J/2$ orthogonal checking. Other $J - J_s$ orthogonal checking are distributed evenly for generating rest of the parity sequences. The 1st decoding does not use a parity sequence which, is generated by the J_s orthogonal checking. MTD works with the orthogonal checking $J - J_s$ in the 1st decoding step and produces additional coding gain in the waterfall region. The 2nd decoding step then works by the all parity sequences. In this case, decoding is done by the J orthogonal checking. By this way of decoding, 0.55 dB additional coding gain is observed for the code with rate 1/2 [10]. In this paper we apply this idea for the codes with rate around 80%.

V. High Speed Decoding

This section gives an idea of parallel processing that speeds up the decoding process. Since, tail biting termination is used, the decoding can start from any position of the received

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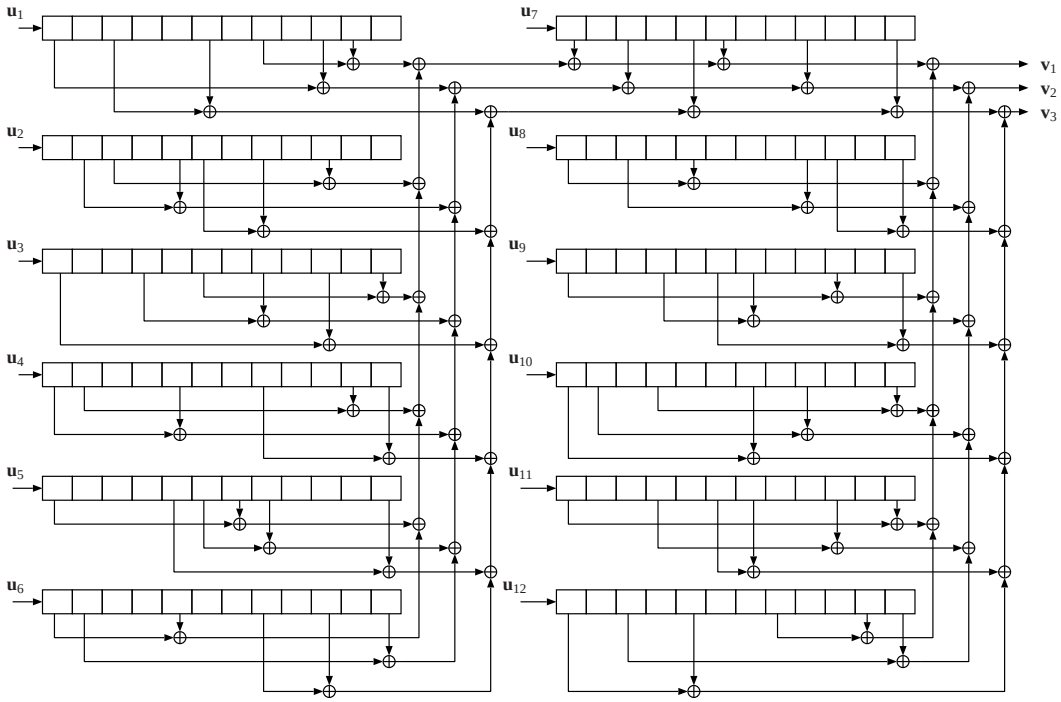

Fig. 4. Self-orthogonal convolutional code type 2 with m=12, n=3, J=6, M=12 and code rate R=12/15=80%.

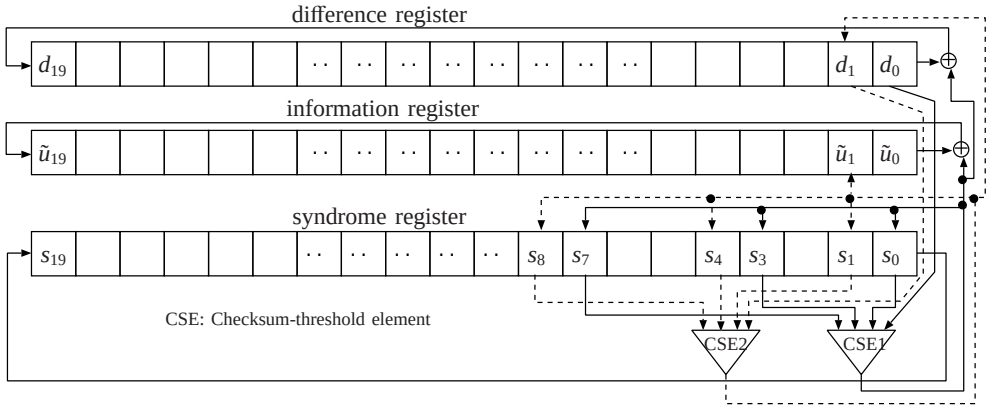

Fig. 5. Parallel processing of MTD with two checksum-threshold elements. The code with m=n=1, J=3, M=8, R=1/2 and code length N=40.

information sequence. If any syndrome is not commonly shared to decode other information bit, decoding can take place in parallel. Among the M positions in the shift register, only J points are involved to decode an information bit. When the minimum tap spacing (tap position difference in the syndrome register) is more than one, MTD can add more than one checksum-threshold elements (CSEs) where different CSE decodes different information bit at the same time. Figure 5 shows a simple example of such decoding scheme for a code with the minimum spacing 3 and two CSEs are shown. For this code, total 3 bits are decoded by the single period of shift register clock. In addition, to reduce the error propagation effect, it is necessary to use information bit length around twice of shift register length [13]. The length of the information bit stream is more than two times (20 bits in this example) of M = 8 value. Therefore, we have possibility to use another set of CSE with 3 elements in the decoding circuit and the decoding is done 6 times faster compared to the single CSE decoding scheme.

VI. Performance of Combined Soft Decoding Multi-Stage Threshold Decoding and 2-Step Decoding

Simulation results and ML decoding performance of the codes are presented in this section. In this case, channel is considered as AWGN and the data modulation is considered as BPSK. Before going to show the error performance, CMTDF with parity check (PC) decoding performance is estimated by using the lower bound of ML decoding of SOCCs and the simulation results of them with PC decoding.

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TABLE I
SELF-ORTHOGONAL CONVOLUTIONAL CODES TYPE 2 WITH CODE RATE R=1/2.

Code parameter	# of shift register		orthogonal checking distribution
	m	n	
J=10 $M = 10^4$	2	2	{5, 5; 5, 5}
J=10 M = 1000	5	5	{2, 1, 1, 1, 5; 1, 2, 1, 1, 5; 1, 1, 2, 1, 5; 1, 1, 1, 2, 5; 2, 1, 1, 1, 5}
J=12 M = 1000	6	6	{1, 1, 1, 1, 2, 6; 1, 1, 1, 2, 1, 6; 1, 1, 1, 2, 1, 1, 6; 1, 2, 1, 1, 1, 6; 2, 1, 1, 1, 1, 6; 1, 1, 1, 1, 2, 6}

TABLE II
SELF-ORTHOGONAL CONVOLUTIONAL CODES TYPE 2 WITH CODE RATE R=4/5.

Code parameter	# of shift register		orthogonal checking distribution
	m	n	
J=8 M = 5000	8	2	{4, 4; 4, 4; 4, 4; 4, 4; 4, 4; 4, 4; 4, 4; 4, 4}
J=10 M = 5000	8	2	{5, 5; 5, 5; 5, 5; 5, 5; 5, 5; 5, 5; 5, 5; 5, 5; 5, 5; 5, 5}
J=12 M = 5000	8	2	{6, 6; 6, 6; 6, 6; 6, 6; 6, 6; 6, 6; 6, 6; 6, 6; 6, 6; 6, 6}
J=10 M=4000	12	3	{2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6; 2, 2, 6}

The lower bound of bit error rate of ML decoding is calculated for the self-orthogonal convolutional code with the orthogonal checking J by [10]

$$P_b \gtrapprox Q\left(\sqrt{\frac{2R(J+1)E_b}{N_0}}\right) \quad (4)$$

where $Q(x) \triangleq \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-\frac{y^2}{2}}dy$ and P_b is the bit error rate of the ML decoding scheme.

Figure 6 shows simulation results of CMTDF for the code with J=10, m=n=2, M=10000, R=1/2, the code length N=81600 and the minimum tap spacing 35 bits. The orthogonal checking distribution of the code is shown in Table I. The dashed line represents the lower bound of ML decoding result of the code. The error performance of CMTDF coincides with the lower bound of ML decoding performance in the error floor region. The CMTDF concatenated with PC decoding makes the BER less than 1/100 times of the lower bound of ML decoding of the SOCC without PC decoding in the error floor region. Simulation results of the 2SD are shown in Figure 7 for the codes with J=10 and 12, M=1000, R=5/10=6/12=1/2, the code length N=81600. The orthogonal checking distribution of codes are shown in Table I. The minimum tap spacing are 4 and 2 for the codes with J=10 and 12, respectively. The 2SD decoding also achieves lower bound of ML decoding performance for the codes. The 2SD with parity check decoding makes also the BER less than 1/100 times of the lower bound of ML decoding for the code without parity check decoding in the error floor region. From these observations, we expect that, the MTD based decoding with parity check decoding can achieve 1/100 times bit error rate of lower bound of ML decoding (without PC decoding) in the error floor region. This result will be applied for estimating the bit error rate of MTD based decoding with PC decoding at the BER below 10^{-12}.

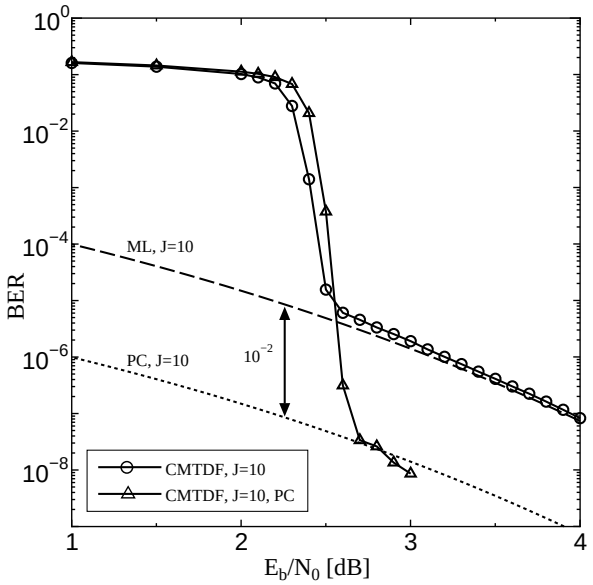

Fig. 6. Bit error performance of CMTDF for the SOCC type 2 with m=2, n=2, J=10, M=10000, R=2/4 and code length N=81600. Code is in Table I.

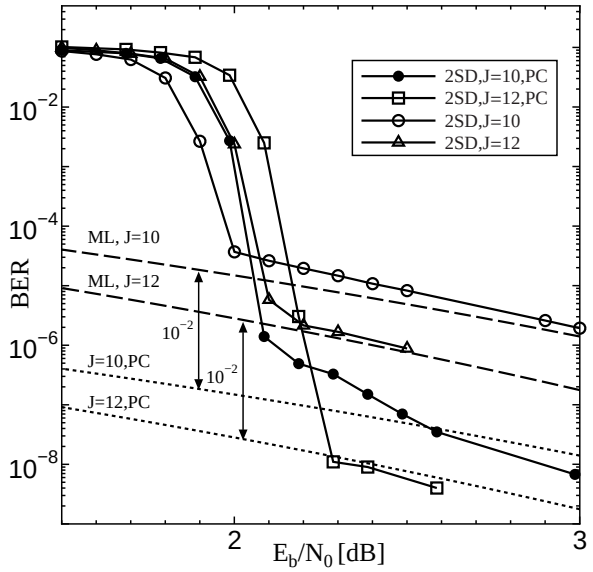

Fig. 7. Bit error performance of 2SD for the SOCC type 2 with m=n=5 for J=10 and m=n=6 for J=12, M=1000, R=5/10=6/12=1/2 and code length N=81600. Code is in Table I.

Figure 8 shows the bit error performance of CMTDF for the SOCC:TP2 with the code rate R=8/10=4/5, m=8 and n=2. The shift register length is M=5000 each. The figure shows the bit error performance for the codes with J=8, 10 and 12 and the minimum tap spacing are 2, 5 and 5, respectively. CMTDF for the codes with rate 80% also achieves the lower bound of ML decoding performance at higher E_b/N_0. The dotted line connected to the simulation result is the extrapolation of

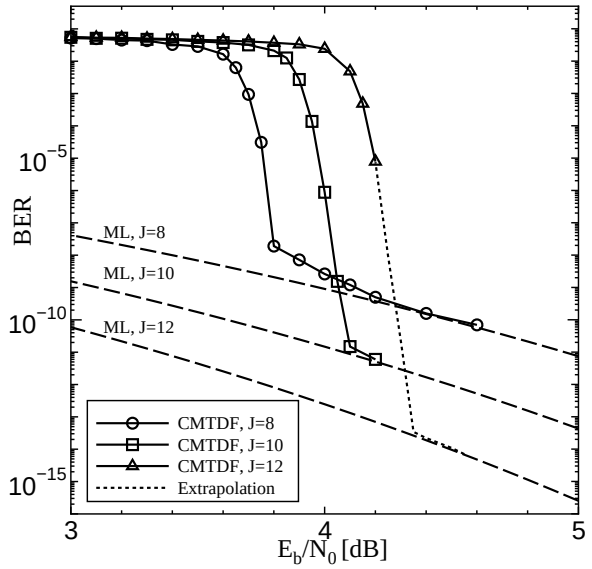

Fig. 8. Bit error performance of CMTDF for the SOCC type 2 with m=8, n=2, M=5000, R=4/5 and code length N=105060. Codes are in Table II.

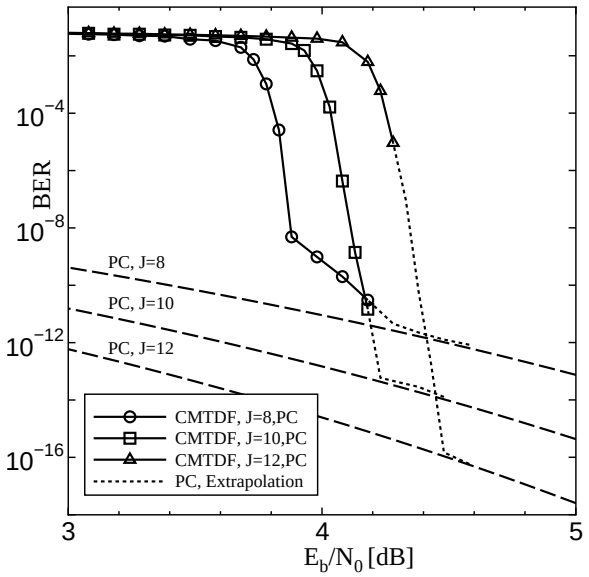

Fig. 9. Bit error performance of CMTDF with PC decoding for the SOCC type 2 of m=8, n=2, M=5000, R=4/5 and code length N=105060. Codes are in Table II.

the error performance up to lower bound line, because this performance is expected. The codes with J=8 gives better performance in the waterfall compared to the other codes, but the error floor is degraded. The 100 Gb/s OTN system demands at least 10 dB coding gain at the bit error rate less than 10^{-12}. The CMTDF for the code with J=10 achieves coding gain 9.0 dB at the BER 10^{-10}. For the code with J=12, CMTDF produces the coding gain 9.96 dB at the BER 10^{-13} and 10.20 dB at the BER 10^{-15}. In this point, the CMTDF for the SOCC:TP2 with J=12 is effective for 100 Gb/s OTN system. The decoding scheme uses average number of iterations (summation of the average iterations uses by the WMTD and by the SMTD) 23 at E_b/N_0=4.8 dB for the code with J=12.

Figure 9 shows the bit error performance of CMTDF with parity check decoding for the same codes mentioned in the Figure 8. The estimated error performance of CMTDF with PC decoding is shown by the dashed line with mark 'PC' in the figure. With the PC decoding, CMTDF for the codes with J=10 produces the bit error rate 10^{-13} and achieves the coding gain 10.10 dB. In this case, average number of iterations is 19.6 at E_b/N_0=4.8 dB. The code with J=10 with parity check decoding satisfies the requirement of 100 Gb/s OTN system. The overall code rate, in this case, is 78.43%. The same decoding scheme is used for the code with J=12. The decoding scheme achieves coding gain 10.60 dB at the BER 10^{-15} and 23 average number of iterations is used at E_b/N_0=4.8 dB.

Although CMTDF already realizes the lower bound of ML decoding performance in the error floor, we have opportunity to improve error performance in the waterfall region. The 2SD can produce some extra coding gain in the waterfall region. Figure 10 shows the bit error performance of 2SD for the codes with m=12, n=3, J=10 and shift register length M=4000. The

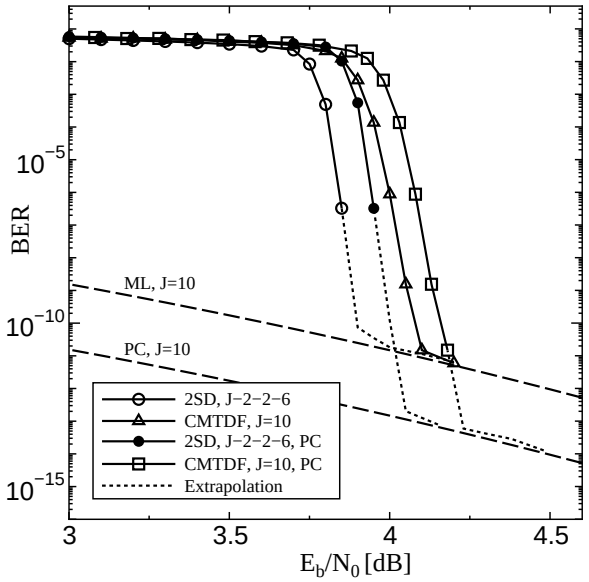

Fig. 10. Bit error performance of CMTDF and 2SD with and without PC decoding for the SOCC type 2 (m=12, n=3) in Table II. The code length is 130050.

code parameters are shown in Table II. This code provides the code rate R=12/15=4/5 and the minimum tap spacing is 4. Figure 10 also shows the comparison of the error performance between CMTDF and 2SD. Their performance with PC decoding is also given. The 2SD for the SOCC:TP2 with the code rate 80% produces additional coding gain 0.25 dB compared to CMTDF. The 2SD with PC decoding for the code achieves coding gain 10 dB at the BER 10^{-12} and 10.20 dB at the BER 10^{-13}. The 2SD uses 90 average number of iterations at E_b/N_0=4.2 dB and it is expected to decrease at

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larger E_b/N_0. The 2SD with parity check for the code with J=10 satisfy the demands of 100 Gb/s OTN system. Moreover, the high speed decoding scheme can reduce the total decoding delay.

The Viterbi and the forward-backward (Bahl, Cocke, Jelinek, Raviv) algorithms gives the ML decoding of convolutional codes. They use trellis states of the code. The algorithms are suitable for the code with constraint length less than 20. The proposed decoding scheme handles a large constraint length (more than 1000) code. Thats why it is not comparable with them. However, min-sum decoding based iterative decoding has been shown in [9]. The CMTDF for the SOCC with rate 1/2 gives the similar decoding performance [6] of min-sum based decoding. So, it is expected that the proposed decoding scheme with high rate code also achieves similar performance with the min-sum decoding.

VII. Decoding Complexity

Table III shows the decoding complexity in terms of basic operations, e.g., modulo 2 summation, real number summation, etc. Decoding complexity is defined by the total number of operations necessary to decode an information bit. The decoding complexity of min-sum based decoding is calculated in terms of add-min operations [9] which, can be broken down to $J+1$ modulo 2 summation and J minimum weight search operations for decoding each information bit. Let, the 2SD uses (I_1, I_2) and the min-sum based decoding uses I_{tr} average number of iterations, respectively, then Table III summarizes the decoding complexity of 2SD and min-sum based decoding. Here I_1 is the average number of iterations used in 1st decoding step and I_2 is the average number of iterations used in final step of decoding for 2SD.

TABLE III
Decoding complexity of 2-step decoding and min-sum based Decoding.

Name of operations	Number of operations necessary for decoding each information bit	
	2-step decoding	min-sum based decoding [9]
Modulo 2 summation	$\leq J^2 + (I_1 + I_2)(J+2)$	$\geq I_{tr}(J^3 + 2J^2 - J - 2)/2$
Min. weight search	$J(J+1)$	$I_{tr}(J^3 + J^2 - 2J)/2$
Real number summation	$I_1(J - J_s) + I_2 J$	$I_{tr} J$

The complexity of the proposed decoding scheme depends on the J^2 operations of modulo 2 summation and minimum weight searching where the min-sum based decoding consumes J^3 operations in the same domain. Therefore, the proposed decoding method uses less number of basic operations than the decoding method given in [9].

VIII. Conclusion

This paper focuses on the forward error correction coding for the 100 Gb/s optical transport network. The optical transport network demands more than 10 dB coding gain at the BER less than 10^{-12} by allowable coding rate more than 80%. Most of the FECs proposed for the network are hard decoding based block code. This paper has presented a kind of soft decision bit flipping decoding using self-orthogonal convolutional codes. The decoding scheme is iterative threshold decoding called MTD that uses the magnitudes of received signals for making decoding decision. The combined soft decoding MTD with feedback (CMTDF) produces lower bound error performance of ML decoding. The CMTDF for the code with J=12 produces the coding gain 10.20 dB with rate R=0.8 at the BER 10^{-15}. It is effective for 100 Gb/s OTN system. When the code contains extra redundancy (not more than 1.5%) due to parity check bits, the 2SD with PC decoding makes the bit error rate 1/100 times compared to the bit error rate of 2SD for the code without extra redundancy. In this case, the code with J=12 be the best choice for the OTN, because it achieves 10.60 dB coding gain at the BER 10^{-15}. Although CMTDF already produces the lower bound of ML decoding error performance, we have possibility to acquire more coding gain in the waterfall region. The 2SD decoding can do this. The 2SD produces 0.25 dB more coding gain compared to CMTDF for the codes with rate 0.8. The 2SD with parity check decoding for the SOCC with J = 10 achieves 10 dB coding gain at the BER 10^{-12} and 10.20 dB at the BER 10^{-13}. The SOCC of J=10 concatenated with parity check code will be another candidate of FECs for the 100 Gb/s OTN system. Moreover, the proposed decoding scheme is less complex than the min-sum based decoding scheme. However, it is expected that, the 2SD for the code with larger orthogonal number produces more coding gain at the bit error rate less than 10^{-15}. Unfortunately, finding such codes with limited span of shift register is an open problem.

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