Low Power Tristate Buffer for Mobile Applications

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***Abstract*—The adaptiveness of integrated electronics is a key feature in current and future mobile applications. Despite the continuous improvement of battery capacity, reconfiguration capabilities of integrated electronics are an inevitable step to cover the rising demand for processing power. Without any further adjustments for efficiency, power consumption becomes a limiting factor for runtime performance. Field Programmable Gate Arrays (FPGA) provide suitable configuration capabilities, but lack of efficient power saving design measures. To overcome this challenge, different approaches were proposed in recent research activities. A substantial contributor to battery load are General Purpose Input Output (GPIO) circuits, which serve the purpose of connectivity. In this paper, we present a modified tristate buffer, which is a key component in a typical GPIO design. Modifications for active power reduction and standby leakage current suppression are applied at circuit level to achieve a better energy efficiency. This new tristate buffer design is compared to already existing designs.**

Keywords–Tristate buffer; GPIO; Power reduction; Leakage suppression; Energy efficiency.

I. INTRODUCTION

Mobile computing is the driving factor for innovations on the field of instant availability of information. It is expected to have the same computing performance in mobile devices like smartphones, tablets and even sometimes in vehicles, as known from high performance computers in very demandable applications. Vehicles approach a rising degree of functions supporting autonomous driving which require fast evaluation of different driving situations in real time. This comes along with a urgent demand for continuously rising computing power, whilst batteries do not experience comparable proceedings in terms of higher capacities. Field Programmable Gate Arrays (FPGAs) offer vast reconfiguration capabilities way beyond their earlier use case as glue logic [3]. Depending on the size of the FPGA in terms of number of Configurable Logic Blocks (CLBs), different designs can be loaded into the FPGA and therefore synthesized by an intelligent routing of CLBs. However, in most cases implemented designs do not use all resources of reconfigurability, leading to a waste of energy due to leakage currents flowing through blocks in standby mode. Unused blocks inside an integrated circuit, which is intended to be used in mobile applications, should be switched off and only turned on again, if more resources are needed. Different design methodologies can be used on different hierarchical levels to realize a fine-grain and coarse-grain approach for reduction of consumed power. This can be achieved by an efficient combination of design decisions at circuit level, e.g., power gating, clock gating, dynamic voltage scaling, etc [4]. A breakdown of a CLB into its single blocks reveals further possibilities to modify the schematics towards the intended low power purpose, e.g., optimization of configuration random access memory (CRAM) [1] and data flip-flops (D-FFs) [2]. In addition to that, investigations have shown that a noticeable amount of power is dissipated by the General Purpose Input Outputs (GPIOs), which serve as a generic input / output device for integrated circuits [5]. As the number of reconfigurable / adaptive electronics in mobile applications is expected to grow continuously, we beliebe that special attention in terms of improvements or redesign should be allocated to these special circuitry, which can not be neglected for the sake of well interconnectivity in integrated circuits.

In this paper, we investigate a standard tristate buffer design on its most significant characteristics, which are dynamic power consumption, standby leakage current and high Z capabilities. In Section II, we give an overview about related work and key aspects of dependencies between performance and power consumption. In Section III, we introduce a reference design of a tristate buffer and discuss typical characteristics in operation and standy. In Section IV, a newly implemented tristate buffer is presented and its benefits for energy sensitive usage are introduced. In Section V, we compare the simulation results of the different investigated designs. In Section VI, all previous discussions are summarized and concluded.

II. RELATED WORK

GPIOs are used in almost every integrated circuit as an interface to communicate with peripheral circuitry. These elements are designed for receiving data as inputs and to transmit data as output to other connected devices. Therefore tristate buffers are bidirectional circuits with the ability to receive and to transmit logic signals by the same input/output pin. Due to this important functions, GPIO play a major role in consumed area of a chip and power consumption in each complex design [6]. Figure 1 illustrates a simplified block diagram of a FPGA without any additional hard processing cores.

As illustrated in Figure 1, all CLBs of this simplified internal hierarchy are surrounded by GPIO blocks. For the sake of simplicity, all further blocks, e.g., switching matrices, are not displayed there. In complex systems, several FPGAs may drive an internal bus for different purposes, e.g., data exchange, leading to potential conflicts when different circuits try to write different logic values to the same bus line.

Figure 2 highlights the described conflict and depicts a situation, in which two different FPGAs, connected to the same 4 bit data bus, drive the same line with different values: whilst FPGA1 drives one signal line of the bus with a logic 1 or V_{dd}, FPGA2 tries to do same but with a logic 0. The consequence is a floating voltage on the interconnection signal line, which is difficult to predict and an undefined state. For this reason tristate buffers play an important role inside each GPIO, since they offer one special output state beside their functionality to pass a logic value from the input to the output node: $highZ$, also called high impedance. By enabling this state, a tristate

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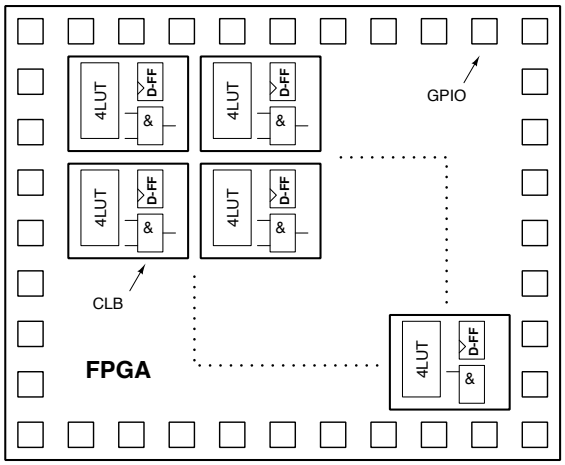

Figure 1. Simplified FPGA structure

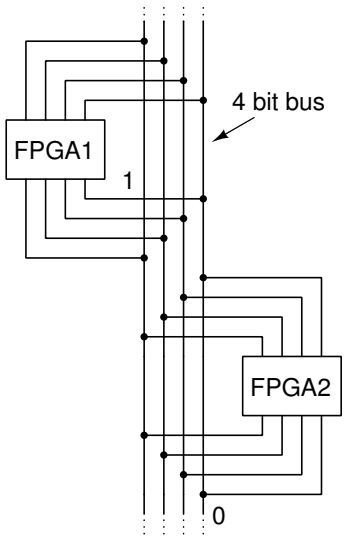

Figure 2. Interconnection bus

buffer cuts off the connection between its input and output node and therefore prevents an undesired throughput from the inputs of the GPIO inside an FPGA to the interconnection bus. So in general, we can identify three aspects to be of relevance for optimization in terms of energy efficiency:

- Subthreshold / standby leakage
- Active power consumption
- $highZ$ behavior

Each of these bullet points has to be adressed by a careful analysis of parameters which are responsible for different behaviour and therefore also different results or performance of the circuit in scope. Subthreshold leakeage current can be characterized by the following equations [7][8]:

$$J_{DT} \propto A(\frac{V_{ox}}{T_{ox}})^2 \tag{1}$$

$$I_{leak} \propto \frac{W}{L_{eff}} e^{(V_{GS}-V_{t0}-\gamma V_{SB}+\eta V_{DS})/nV_t)(1-e^{-\frac{V_{DS}}{V_t}})} \tag{2}$$

Equation (1) explains that a higher oxide thickness T_{ox} will subsequently lead to a lower current density J_{DT}, which is a favored effect for our purposes as we intent to limit undesired current flows as good as possible. On the other hand, (2) highlights the dependency of a subthreshold current I_{leak} to different factors, e.g., the transistor length L_{eff}, the gate-source voltage V_{GS} and the source-body voltage V_{SB}. On the other hand, active power consumption P_{dyn} depends on various factors showed in the following equation:

$$P_{dyn} = \alpha C_{load} V_{dd}^2 f_{Clk} \tag{3}$$

Equation (3) [9] shows that for significant reduction of consumed battery power several factors, e.g., the switching activity α, the load capacitance C_{load}, the supply voltage V_{dd} and the operating frequency f_{Clk} have to be designed in a way to keep P_{dyn} as low as possible. Some factors like C_{load} can not be easily controlled, however other factors can be adapted in a better way directly at circuit level. Last but not least, the $highZ$ attributes of a tristate buffer play an important role due to their ability to decouple this buffer from the remaining signal chain. A careful design of the output transistors inside a tristate buffer offers heavy impact on this ability. Nevertheless it should be stated here, that priority was put on low power characteristics of our newly implemented design. Measurement of the $highZ$ state with different output voltages was done after evaluating power consumption of all investigated designs. Furthermore, all measurements were compared against each other to figure out which design performs best in general.

III. TRISTATE BUFFER CELL DESIGN

The basic purpose of a buffer circuit is to forward the input value with a certain delay to the output node. Some applications might require the addition of a delay time for synchronizing different data paths. The easiest way to understand the basic function of a buffer is to imagine the logic function of two inverter in series. A tristate buffer adds a third, important feature to this functionality: the $highZ$ state. For a better understanding of the circuit's function, a tristate inverter is shown in Figure 3.

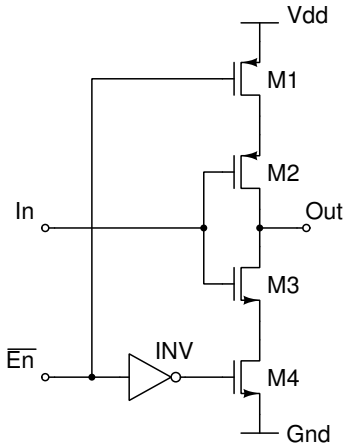

Figure 3. Tristate buffer

As long as $\overline{En}$ provides a logic *LOW* at the respective input node, the transistors *M1* and *M4* are turned on and

subsequently provide a direct path to the voltage source V_{dd} and Gnd. As a consequence, the transistors *M2* and *M3* work as an inverter and therefore invert all signals applied to In. On the other hand, if $\overline{En}$ turns to *HIGH*, *M1* and *M4* are turned off and cut-off the internal transistors *M2* and *M3* from the supply voltage and ground path. In this special case, the voltage at the output node *Out* is floating and undefined. This means that in dependence of this floating voltage, only a very small current will flow either as leakage current from the tristate inverter into the circuitry connected to *Out* or from the load into the tristate inverter to Gnd. By adding one additional *nMOS* and *pMOS* transistor, the discussed tristate inverter can be modified to a tristate buffer, which is shown in Figure 4.

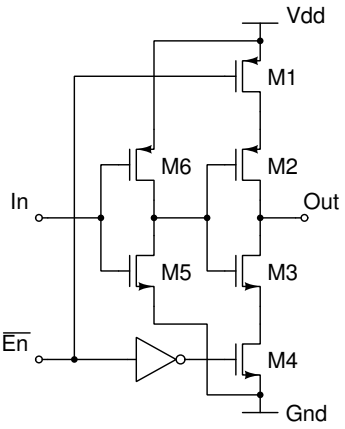

Figure 4. Standard design of a tristate buffer

Different aspects of this tristate buffer's behavior have been investigated during simulations by a $90nm$ TSMC (Taiwan Semiconductor Manufacturing Company) technology and a Cadence toolchain (INCISIVE 6.1.5). All simulations, serving the purpose investigating the circuit's dynamic performance, were done at an operating frequency of $200MHz$ and with standard settings for all transistors' dimensions ($120nm$). Since all analyzed designs are not dynamic logic inheriting a dedicated Clk input, the operating frequency was modulated into the switching events of $\overline{En}$. The results of the first simulation run with active inputs are shown in Figure 5 and also displayed in Table I and Table II . This simulation was followed by further tests for alternative circuit states with the intention to build up a baseline database for further comparisons.

TABLE I. SIMULATION RESULTS (PWR)

Design type	*Average Power nW*	*Max. Power uW*	*Min. Power pW*
Reference	245	56.75	103.8

TABLE II. SIMULATION RESULTS I_{Vdd}

Design type	*Avg. Current nA*	*Max. Current uA*	*Min. Current nA*
Reference	215.2	230.5	261.4

The simulation results display the correct function of this tristate buffer, which directly passes the input value to *Out* whenever $\overline{En}$ is set to *LOW*. Once $\overline{En}$ applies a logic *HIGH* to the cutoff transistors, the voltage level at *Out* starts to float and

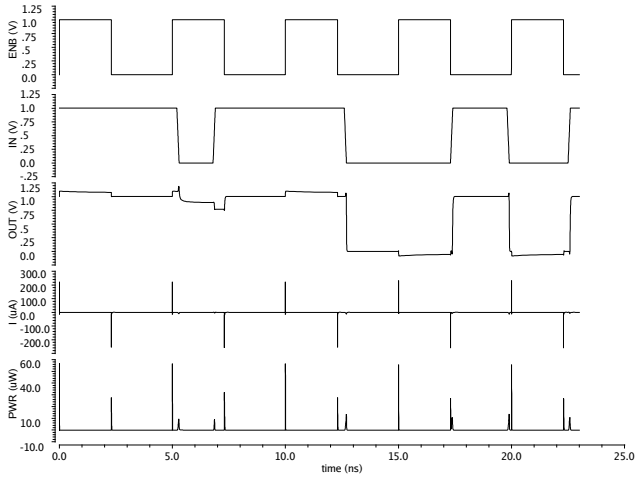

Figure 5. Simulation results of dynamic behavior of a standard tristate buffer

swings between voltage levels above V_{dd} and below $0V$ (Gnd). These floating voltages are not defined and also indicate that the whole circuit is in *highZ* mode. Active power dissipation is of high importance for the estimation of required energy resources, but regardless of these results it is also obligatory to have a closer look on the standby power characteristics when the circuit is lead into an idle phase or put completely into standby mode. This means that the data input is inactive and $\overline{En}$ active. The simulation results are shown in Figure 6.

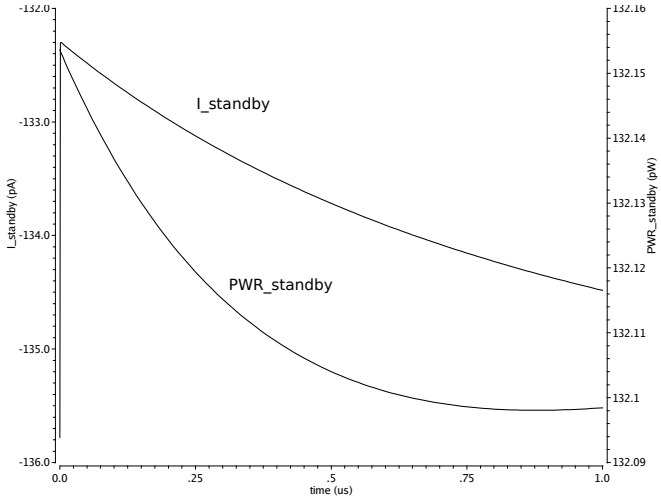

Figure 6. Simulation results of idle standby results

For this analysis and for a better observation of the standby current, the simulation runtime was set to $1\mu s$. The simulation curves of both, standby current and standby power dissipation, show the discharging process of all internal parasitic capacitances after powering on the circuit at the very beginning of the simulation process. Both, standby current and the allocated dissipated power, continuously decrease over time, resulting in an average leakage current I_{leak} of $133.6pA$ and a related average power dissipation of $132.1pW$.

The remaining aspect to be considered at this point is the behavior of the reference tristate buffer in *highZ* mode after setting $\overline{En}$ to *HIGH*. First of all, it should be stated here that

there is no unambiguous answer on this question, since this depends on the voltage which will be applied by the load to the output node *Out* of the tristate buffer. In addition to that, there is always a small throughput from the input node on the output in case that the tristate buffer in *highZ* is still stimulated with input date, which might be a realistic situation when the related control logic fails. Thus, two different situations, active and inactive inputs, must be considered. Based on the assumption that the voltage applied to *Out* may vary from $0V$ to$1V$, a dc sweep simulation was done. The results of both test runs are displayed in Figure 7.

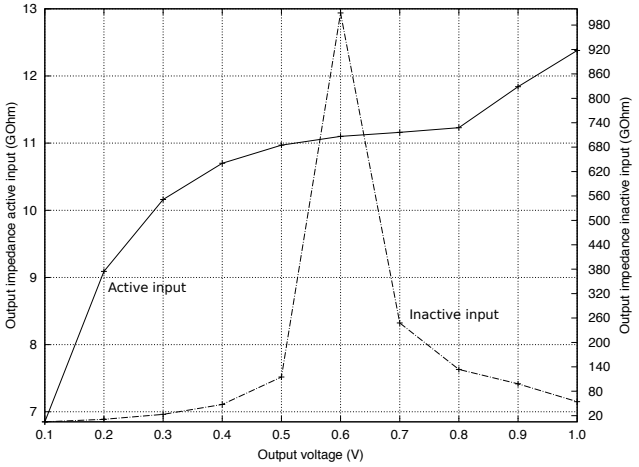

Figure 7. Simulation results of output impedance in *highZ* state

Active input data has a remarkable influence on the circuit's capabilities to decouple its internal switching events to the output node. In case of setting the input node to a $0V$ and therefore making it 'inactive', Figure 7 reveals a sweetspot in terms of output impedance and which is closely allocated to almost $V_{dd}/2$. Having this striking high output impedance ($\approx 1.01T\Omega$) at this voltage range is a desirable situation, since this implements an almost perfect balance between current source and current sink. If input data are applied to *In*, a drop the output impedance can be observed after simulation. Even with turned of decoupling transistors *M1* and *M4*, the throughput originating from the buffer's input is strong enough to lower the impedance at *Out*. Therefore, a stronger decoupling mechanism would probably lead to better results.

IV. Modifications

A careful analysis of the reference tristate buffer pointed out that there is still room left for different improvements. Thus, a noticeable adaption of circuits for sensitive low-power application can only be achieved by a synergy of different power savings measures for imaginable operating states.

A. Power Gating

On our way to develop a low-power tristate buffer, the implementation of a *'hold'*-mechanism for standby-phases was an inevitable step. The difficulty here was the fact, that this design does not imply clocked inputs which could have been gated. Instead of this, a more stringent design technique was applied: power-gating. This modification can be applied in different ways, by adding a gating transistor between the supply voltage and the circuit or by inserting a transistor between *Gnd* and all internal nodes. A third alternative comes along with a combination of both design modifications and can be found in Figure 8 (transistors *M5* and *M10*).

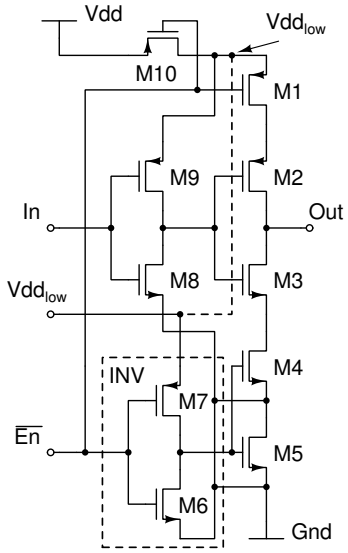

Figure 8. Low-power tristate buffer

The addition of two transistors to a design with a total number of eight transistors before this modification means an increase 20% and a high probability for penalty in terms of area consumption. Regardless of the chosen technology for synthesis and allocated continuous proceedings in technology node shrinking, a higher number of transistors is always considered as a drawback. On the other hand, this modification is responsible for a noteworthy limitation of leakage current running through the design under test (DUT), since we achieve a complete decoupling of the tristate buffer vor V_{dd} and *Gnd* respectively.

B. Leakage Current Reduction

A reasonable extension of power gating is the use of special transistors with a higher oxide thickness T_{ox} which can be also seen in (1), where T_{ox} is in the denominator and therefore has the ability to limit the electrons tunneling through the transistor's gate connector. This results in a reduction of the leakage current in idle / standby state. Despite these benefits it should be mentioned that high T_{ox} transistors have a slower switching frequency than standard T_{ox} do. Hence, adding these transistors should be carefully waived taking a decision upon it. In our case, *M5* and *M10* have an increased T_{ox} than the remaining transistors have for keeping the penalty in performance degradation as low as possible.

C. Subthreshold Current Reduction

Whilst power gating is an effective method for a total shutdown of a circuit, there should be an alternative for measurable reduction of a current flowing through a transistor with an applied gate-source voltage V_{gs} below the threshold. voltage V_{th}. This led to the decision to apply high V_{th} transistors, which have the ability to cut off subthreshold electron tunneling. This method might have a negative impact on the maximum operating frequency and should be carefully applied.

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Nevertheless, these special transistors can not be neglected during the design of low power designs. All internal transistors, except the gating transistors, have been replaced by their hight V_{th} counterparts and simulated.

D. Multi Supply Voltage

An operating circuit in low power applications should not only be optimized for static power reduction but also for energy efficiency in active mode. As shown in equation 3, the supply voltage has a vast influence on the overall dissipated power. It's obvious that the best approach would be to decrease the global supply voltage V_{dd}, but might lead to the necessity of additional level restorers for a smooth signal transmission to other circuitry. An alternative is the careful partial supply voltage reduction within a design after analyzing certain parts of a design, which could be powered by a lower V_{dd}. On the other hand, lowering V_{dd} comes along with a slower computation time of the input values, therefore a smaller supply voltage V_{ddlow} was only applied to the internal inverter *M6* and *M7*. In principle, there are two different ways how to generate V_{ddlow}: this can be realized by an external voltage source (illustraed by the additional voltage source V_{ddlow} in Figure 8) or by exploiting internal voltage nodes (illustrated by the dashed line in Figure 8). The second option shows its beauty by an inherent voltage reduction automatism. Once $\overline{En}$ goes *HIGH M10* is turned off and therefore cutting off *M7* from V_{dd}, but keeps the internal inverter still working. Minor adaptions to the width of *M7* have to made due to the decreased internal supply voltage. Nevertheless, both options work well with the low power tristate buffer.

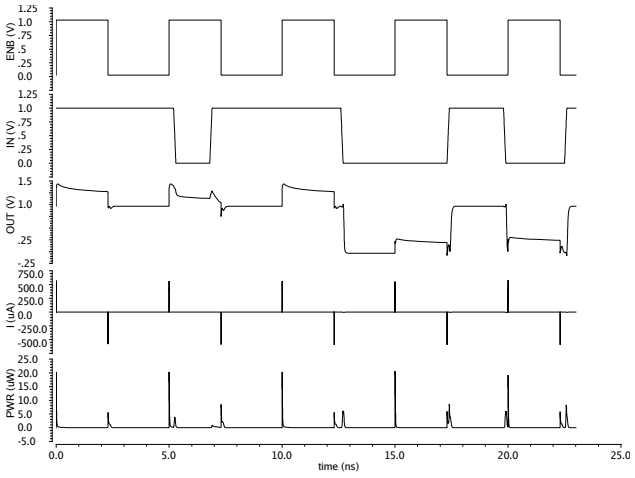

Figure 9. Simulation results of dynamic behavior of the low-power tristate buffer

Figure 9 shows the dynamic behavior of the low power tristate buffer. Compared to the simulation curves shown in Figure 5, it can be seen that the low power tristate buffer is superior in terms of dissipated power during active runtime. The related simulation results are summarized in Table III and Table IV.

Furthermore, an analysis of the standby behavior revealed an improved average leakage current I_{leak} of $24.1pA$ and a related average power dissipation of $22.04pW$. As a final step, the *highZ* characteristic was investigated for having a better

TABLE III. SIMULATION RESULTS (PWR)

Design type	*Average Power nW*	*Max. Power uW*	*Min. Power pW*
LP tristate	191.3	29.72	22.36

TABLE IV. SIMULATION RESULTS I_{Vdd}

Design type	*Avg. Current nA*	*Max. Current uA*	*Min. Current nA*
LP tristate	225.8	194.8	206.9

comparison to the reference design. The simulation results are displayed in Figure 10.

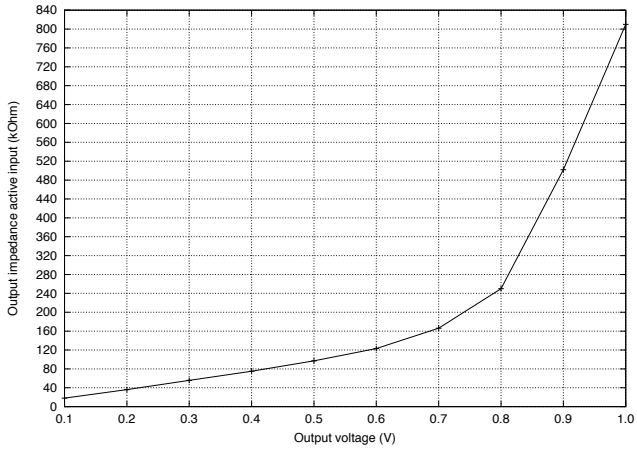

Figure 10. Output impedance in *highZ* state (low power tristate buffer)

In contrast to the reference tristate buffer, the newly implemented tristate buffer shows a different behavior. First of all, the output impedance shows a smaller order of magnitude ($G\Omega \rightarrow k\Omega$) and in addition to this, the output curve strongly depends on the voltage at the output node and reveals a proportional dependency. The higher the voltage at *Out* is, the higher the output impedance will be. Despite the fact that the low power tristate buffer's active *highZ* curve has a smaller order of magnitude, the evaluated results are still acceptable and give an evidence about the appropriateness for the usage as an connecting element in complex designs. These results could be improved by modifying the gate lengths of the output transistors *M2* and *M3*. The downside of this modification would lead to necessary modifications of the manufacturing process, but which can be easily handled by modern technology nodes.

V. RESULTS COMPARISON

For a better comparison of the investigations which have been done, all results were summarized in Table V. The low power tristate buffer outperforms in almost each aspect the reference design, which highlights its appropriateness for use in applications with limited energy resources. Results of dynamic behavior show that power dissipation is reduced significantly, no matter whether the average, maximum or minimum power consumption is in focus of discussion. The most remarkable reduction is allocated to static behavior of both circuits. Here, the standby leakage current and the dissipated power in idle mode are lowered by over 80%, which emphasizes the effect of implemented low power measures.

TABLE V. SIMULATION RESULTS I_{Vdd}

Design type	*Reference buffer*	*Low power buffer*	$\Delta\%$
Av. PWR (nW)	245	191.3	22 $\downarrow$
Max. PWR (uW)	56.75	29.72	47.63 $\downarrow$
Min. PWR (pW)	103.8	22.36	78.46 $\downarrow$
Av. Current (nA)	215.2	225.8	5 $\uparrow$
Max. Current (uA)	230.5	194.8	15.49 $\downarrow$
Av. Leak. Current (pA)	133.6	24.1	82 $\downarrow$
Av. Standby PWR (pW)	132.1	22.04	83.32 $\downarrow$
highZ max.	12.38 $G\Omega$	81 $G\Omega$	$\uparrow\uparrow$
highZ min.	6.85 $G\Omega$	18 $k\Omega$	$\uparrow\uparrow$

The appropriate choice of process technology due to the multi-oxide requirements as well as careful layout of transistor parameters requires special attention and allows additional improvements. However, the low power tristate buffer delivers remarkable out of the box performance without further detailed optimization. These adaptions are achieved with a small penalty in terms of transistor count and area. Xilinx provides 372 *Maximum User I/O* and 165 *Maximum Differential I/O Pairs* [6], which could be realized in 537 GPIOs. Implementing a new FPGA design by usage of the low power tristate buffer requires 1074 additional transistors. Here it comes to the point where an efficient layout of the overall chip could be a measures to catch up this drawback. In addition to that, the achieved minimum *highZ* state of the new design of about $14k\Omega$ does not perform as good as the result of the reference tristate buffer ($6.85G\Omega$). This could be improved by a further optimization of the transistor parameters in terms of length and width. However, this might lead to a higher energy consumption and should be carefully decided case by case, depending on which characteristic is of higher importance for the respective application. Despite the additional parasitic capacitances which come along by adding transistors, nearly all measured insights does not weaken the positive overall print.

VI. CONCLUSION

We analyzed an existing design of a tristate buffer, which was baselined as a reference design serving for further comparisons. During the analysis we did a deep dive into the characteristics of this design for the evaluation of its active and standby performance in terms of dissipated power, average current consumption and the special ability to enter a *highZ* mode. The outcome of these activities was that we wanted to develop a tristate buffer which is superior in terms of energy savings during runtime and idle state. Due to the lack of a clock signal and therefore the impossibility to apply clock gating, we implemented power gating by choosing special high T_{ox} transistors. These transistors have the ability to decouple the tristate buffer from V_{dd} and *Gnd* as well as the function of gate tunneling mitigation. For subthreshold current reduction we decided to use high V_{th} transistors, being aware of accepting a penalty in the maximum operating frequency, which was not in the focus of our work though. Simulations have shown that the low power tristate buffer delivers outstanding performance in terms of, e.g., average power consumption in active mode, which is decreased by 22% compared to the reference design. This is a noticeable improvement, since it shrinks the losses of energy in active mode of almost a quarter compared to the reference design. In standby mode, our design outperforms the legacy design by 82% related to average I_{leak}, which is a remarkable result. This low power design features the ability to provide the generation of an internal, smaller supply voltage without any extra *enable* signal from external circuitry. The *highZ* mode abilities of the legacy design are better by a higher order of magnitude, nevertheless we consider the achieved results of the new tristate buffer as acceptable. These results come at the cost of a higher transistor count and an additional input for an internal, decreased supply voltage I_{Vddlow} as an option. Several possibilities exist for future investigations and improvements. A very simple but effective method for achieving remarkable power savings would be the choice of a technology library with shorter channel lengths, e.g., $28nm$. A technology shrink usually leads to a measurable reduction of consumed power, however, this comes along with some drawbacks like the short-channel effect. Applying negative V_{GS} voltages is an effective way to suppress subthreshold leakage currents after turning a transistor off. Of course, this requires auxiliary logic for generation of negative V_{GS} gate voltages, but this should be a small amount of additional transistors. Further supporting measures can be applied at a higher hierarchical layer, e.g., at architectural level. Controlled dynamic voltage scaling offers the potential to drive the whole. circuit into a deep sleep mode if a standby mode is not crucial for operation of the whole logic. These suggested measures will be starting points for further elaboration of enhanced energy balance with strong focus on a extended battery lifetime in mobile applications.

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