Designing Towards A Fully Monolithic Envelope-Tracking SiGe Power Amplifier for Broadband Wireless Applications

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Abstract— **This paper presents an overall design path towards our fully monolithic envelope-tracking (ET) power amplifier (PA) in a 0.35 µm SiGe BiCMOS technology. First, a discrete hybrid switching supply modulator (SM) is designed to study the effects of its switching frequency and bandwidth limitation to the linearity and efficiency of an overall ET-PA. Next, the same circuit configuration is used for our CMOS SM which modulates our self-biased cascode SiGe PA with the proposed envelope shaping function. By analyzing the power losses of the CMSO SM under our special ET operation, we show the SM can still achieve high efficiency with a relatively low switching frequency, which helps to improve the system linearity. At 1.9 GHz, our BiCMOS cascode ET-PA delivers the maximum linear output power (P_{out}) of 24/23.4 dBm with the overall power-added-efficiency (PAE) of 41%/38% for the long-term evolution (LTE) 16QAM 5/10 MHz signals, respectively. Meanwhile, good linearity and low spurious emission are achieved without the need of digital predistortion (DPD).**

Keywords- Broadband; envelope-tracking (ET); hybrid switching supply modulator (SM); long-term evolution (LTE); SiGe; power amplifier (PA); WiMAX

I. INTRODUCTION

Broadband 3G/4G/WLAN wireless standards utilize highly spectral-efficient modulation schemes with inherent non-constant envelope signals having high peak-to-average power ratios (PARs). In a typical mobile transmitter (TX), the radio frequency (RF) power amplifier (PA) tends to be the most power-hungry block. Although high efficiency can be achieved by the PA at the saturated output power (P_{sat}) for GSM handset systems, its high distortion at P_{sat} violates the linearity specs for non-constant envelope signals (e.g., in the case of long-term evolution (LTE)). Therefore, the PA is usually required to be backed off from its P_{sat} for non-constant envelope signals, resulting in poor efficiency.

The envelope tracking (ET) technique is a promising solution to improve the PA efficiency for broadband applications [1]-[12]. In ET-PA systems, the envelope signal from a supply modulator (SM) dynamically modulates the PA collector or drain voltage in response to the instantaneous output power (P_{out}). In practical implementation, a hybrid switching SM (also called as a linear-assisted switching SM) is often used to achieve a good balance between the efficiency and the wideband envelope tracking [1]-[16]. Although many articles have reported excellent efficiency by using this hybrid switching SM, its design details still need to be studied and optimized with a specific PA to achieve the best trade-off between the efficiency and linearity for the overall ET-PA. In ET systems, both the PA and SM are the distortion sources, thus if the SM can be tuned for better linearity without suffering a great efficiency reduction, the PA can be pushed into deeper compression, leading to higher overall efficiency. Moreover, a hybrid switching SM is typically designed with a high average switching frequency (e.g., ≥ 2 MHz in [9]-[11]), creating out-of-band spurs which may violate the spectral mask of interest and spurious emission specs. To sufficiently suppress the high frequency switching ripples, the linear stage of the hybrid switching SM must have an ultra-wide bandwidth, inevitably increasing the design complexity [17]. Therefore, it becomes necessary to understand how much the average switching frequency can be lowered without hurting much on the SM efficiency. To address the concerns mentioned above, in this paper, we will present our complete design path towards a fully monolithic ET-PA in a silicon based technology.

In Section II, a discrete hybrid switching SM is designed to study the effects of the bandwidth limitation and switching frequency to the linearity and efficiency of the overall ET-PA system. The discrete SM is paired with a SiGe PA in Section III to compare the performances between the stand-alone PA (i.e., the fixed supply PA) and the ET-PA. The measurement data verifies that our design approach of the SM is suitable for high PAR wideband applications.

As the expansion to the work [1], we will present our fully monolithic BiCMOS ET-PA in Section IV. A CMOS SM will be integrated with the cascode SiGe PA in a 0.35 µm SiGe BiCMOS technology to form a fully monolithic ET-PA system. In contrast to the discrete solution described in Section II, the single-chip ET-PA integration solution has several benefits: (1) it reduces cost; (2) it has an integrated signal path providing better signal integrity [11], and (3) from the design perspective, the PA and the SM can be optimized together to achieve better linearity and overall efficiency. Unlike common emitter PAs, our cascode PA structure relieves the voltage stress on the power transistor, while also requires some special envelope shaping function to improve its linearity at the ET operation. In Section IV, we will first highlight the self-biasing structure of our cascode PA design and our proposed envelope shaping method based on [3]. Moreover, we will analyze the power

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losses of the CMOS SM in details in responding to our special cascode ET-PA operation. Although the same SM was presented in [3], [4], this paper further demonstrates how our SM can achieve high efficiency with a relatively low average switching frequency, which helps to improve the overall ET linearity. Based on the measurement data in Section V, our BiCMOS cascode ET-PA achieves state-of-the-art overall efficiency with good linearity performance for LTE 16QAM 5/10 MHz signals. No digital predistortion (DPD) technique will be used in our measurement.

II. Design Insights for Envelope Tracking

A. Design of Common-Emitter SiGe Power Amplifier

A monolithic 1-stage common-emitter SiGe PA is used here as an example to form an ET-PA system to study the trade-offs for the hybrid switching SM design. This PA was designed and fabricated in the IBM 7HP 0.18µm SiGe BiCMOS technology [5], [6]. The simplified schematic and die picture of the PA are shown in Fig. 1. The high-breakdown heterojunction bipolar transistor (HBT) option is used for the PA design with a total emitter-area of 220 µm^2 (typical BV_{CEO}= 4.2 V, BV_{CBO}= 12.5 V). This monolithic SiGe PA was tested on an FR4 PCB. To achieve high power-added-efficiency (PAE), the RF choke (RFC) inductor was left off-chip for high Q at 2.4 GHz. Additionally, the output tank inductor was realized by a bondwire, and more than 4 downbonds (i.e., bondwires at the emitter node) are used to reduce the grounding parasitic inductance [5]. No other off-chip elements are needed for the input and output matching.

It is important to characterize the PA thoroughly before designing the SM for optimal ET-PA performances, as the collector impedance presented by the PA (R_{load}) will affect the efficiency and linearity performance of the SM. Fig. 2 shows the measured PAE vs. output power (P_{out}) at different supply voltage V_{CC} in the continuous wave (CW) mode. For the fixed-supply PA, its PAE reduces rapidly when P_{out} drops, while the PAE at low P_{out} can be greatly enhanced by varying V_{CC} as shown by the dash curve. The dash curve is the ideal operating trajectory of an ET-PA by tracking the peak PAE points at different P_{out} levels. Fig. 2 also plots the R_{load} presented by the PA to the SM, which is calculated from the DC supply voltage and the measured DC supply current of the PA at each peak PAE point. The R_{load} changes roughly from 70 Ω to 10 Ω at P_{out} from 8 dBm to 20 dBm.

B. Hybrid Switching Supply Modulator

A proper SM design is critical to achieve the best overall efficiency and linearity performances for an ET-PA. As reported in [2], the finite bandwidth and the associated group delay of the SM are large contributors of nonlinearity in an ET-PA. In addition, to take advantage of the efficiency enhancement provided by the ET technique, the SM needs to maintain high efficiency throughout the ET-PA operation. The overall efficiency of an ET-PA system ($\eta_{ET\text{-}PA}$) is the product of the SM efficiency (η_{SM}) and the PA collector efficiency ($\eta_{PA,CE}$), which is expressed as:

$$\eta_{ET-PA} = \eta_{SM} \cdot \eta_{PA,CE} \quad (1)$$

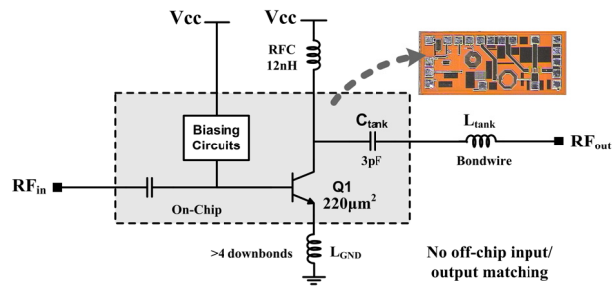

Fig. 1. Simplified schematic and die picture of the 1-stage PA designed and fabricated in IBM 7HP 0.18 µm SiGe BiCMOS technology

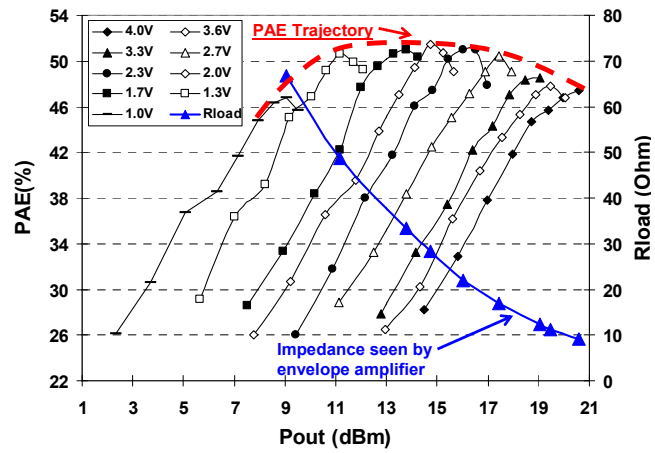

Fig. 2. Measured PAE vs. P_{out} of the SiGe PA in the CW mode, and the R_{load} presented by the PA to the SM

Therefore, the design goals of an SM are high efficiency and wide bandwidth to track the instantaneous input envelope.

1) Hybrid Switching Structure

The envelope signal is extracted from the modulated I/Q (i.e., in-phase/quad-phase) signals from the LTE/WiMAX baseband and then feed into the SM. Such nonlinear transformation will expand the bandwidth of the envelope by a factor of 5-10 compared with the original signal bandwidth [2], [7]. Conventionally, the SM can be implemented in the form of a linear regulator (e.g., a low dropout regulator (LDO) as in [18]), as the linear topology offers wide bandwidth and can reduce much of the output ripples. Nonetheless, the power efficiency of linear regulator is very poor when the output voltage level is low [18], making it unsuitable for high PAR signals for 3G/4G applications. On the other hand, a switching regulator has high efficiency across a broad range of output voltage, but it produces significant output ripples and its bandwidth is constrained to be a fraction of the switching frequency [19], making it suitable only for narrowband applications such as the North American Digital Cellular (NADC) in [19]. With a rather high switching frequency, switching regulators could be pushed into high data-rate systems, but inevitably causing high switching loss that limits the efficiency (e.g., ~76% maximum efficiency for WCDMA in [20]). A high switching frequency may also degrade the ET-PA linearity

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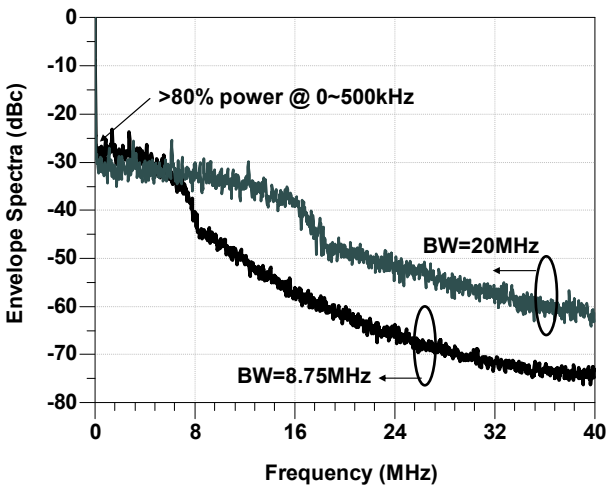

Fig. 3. Simulated envelope spectra of WiMAX 8.75/20 MHz signals

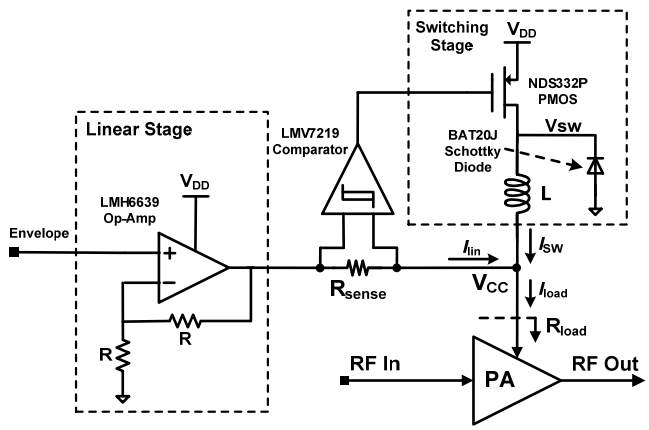

Fig. 4. Schematic of the discrete hybrid switching SM designed by using COTS components

considerably, which often defeats the purpose of using switching regulators for any supply-modulated PAs.

Many recent reports on the wideband SM design for ET-PA have combined the advantages of a wideband linear regulator and a high efficiency switching converter in various ways [1]-[17]. Fig. 3 shows the simulated envelope spectra of WiMAX 8.75 MHz and 20 MHz signals (PAR of ~10.2 dB). An important characteristic of the envelope spectrum is that ~80% of envelope power resides from DC to several kHz, while over 99% of the envelope power resides within DC to 8MHz for the 8.75 MHz signal, and within DC to 20 MHz for the 20 MHz signal, respectively. Such a characteristic of the envelope spectrum implies that a hybrid switching structure can achieve a good balance between efficiency and bandwidth tracking for an ET-PA system. The hybrid switching SM consists of a wideband but low efficiency linear stage and a high efficiency narrowband switching stage. The hybrid structure lessens the requirements of the switching stage, since the fast transients of the envelope signal are taken care of by the wideband linear stage, while the switching stage handles the DC and slow moving signals with high efficiency. The overall efficiency of the entire SM (η_{SM}) is a combination of the switching stage efficiency (η_{SW}) and the linear stage efficiency (η_{lin}), as expressed by:

$$\frac{1}{\eta_{SM}} = \frac{\alpha}{\eta_{SW}} + \frac{1-\alpha}{\eta_{lin}} , \qquad (2)$$

where α is the ratio of the output power from the switching stage to the total output power of the SM [7], [16].

2) Discrete Supply Modulator Design

The hybrid switching SM is implemented by using commercial-of-the-shelf (COTS) components to investigate the overall efficiency and linearity trade-off for an ET-PA system. Fig. 4 shows the circuit implementation of the discrete SM using an operational amplifier (Op-Amp) as the linear stage, and a buck converter as the switching stage. The buck converter supplies the slow slew-rate load current (I_{SW}) that contributes to the majority of the load current (I_{load}) to ensure high efficiency, while the wideband linear Op-Amp stage operates in a feedback mode to track the high slew-rate current (I_{lin}). Additionally, the ripples caused by the buck converter will be attenuated and/or filtered by the linear Op-Amp. The smooth transition between the linear stage and the switching stage is realized by a hysteretic current feedback control. The hysteretic current feedback control consists of a current sensing resistor R_{sense} that senses the output current of the linear stage and a hysteresis comparator to control the buck converter. The value of the sensing resistor R_{sense} is chosen to be 1 Ω in this case, as it needs to be much smaller than R_{load} (i.e., the load impedance presented by the PA) to achieve high efficiency.

C. Efficient and Linearity of the Hybrid Switching SM

Although there are many reports on the efficiency of the SM in the literature [7]-[13], the effects of its bandwidth and switching frequency have not been studied as rigorously. Since the switching ripples (generated by high switching frequencies) and the bandwidth limitation are two major factors that cause distortions at the SM output, understanding their effects helps to optimize both efficiency and linearity of an overall ET-PA system. In this section, the nonlinearities of a discrete hybrid switching SM will be discussed.

1) Bandwidth of the Hybrid Switching SM

The linear stage (i.e., the Op-Amp) should have sufficient bandwidth not only to track the high frequency contents of the envelope signal with high fidelity as suggested by previous works [7]-[13], but also to suppress the switching ripples/noise generated from the switch converter. The switching ripples beyond the bandwidth of the linear stage can distort the envelope signal, and also be mixed with the modulated carrier in the PA to cause large spurious noise at the PA output, potentially degrading the system linearity.

To investigate the effect of the bandwidth, an Op-Amp behavior model provided by Agilent's ADS is used to replace the realistic Op-Amp model in the simulation, so that its bandwidth can be changed manually. The realistic SPICE models are still used for other blocks of the SM. Fig. 5 shows

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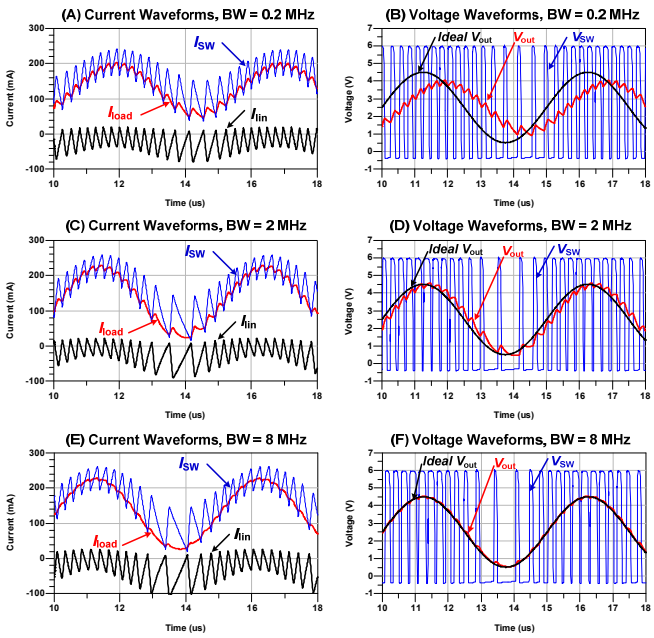

Fig. 5. Simulated (A, C, E) current and (B, D, F) voltage waveforms of the SM; the behavior model is used for the Op-Amp with different 1-dB bandwidths, while realistic SPICE models are used for other blocks of the SM. Input voltage = $1.25+sin(2\pi\cdot 200\text{kHz}\cdot t)$ V, L = 4.7 µH, R_{load} = 20 Ω

the simulated current and voltage waveforms of the SM using different 1-dB bandwidths of the Op-Amp at an input wave of $1.25+sin(2\pi\cdot 200\text{kHz}\cdot t)$ V. Note we found the *1-dB bandwidth* of the Op-Amp is more sensitive and correlates considerably better to the output signal fidelity of the ET-PA than the more conventional 3-dB bandwidth. As shown in Fig. 5(A), (C) and (E), the output current of the switching stage (I_{SW}) has large ripples on the waveforms, which need to be suppressed or cancelled by the output current of the linear stage (I_{lin}) to reproduce an accurate load current waveform (I_{load}). When the 1-dB bandwidth of the Op-Amp is set as 0.2 MHz, the output voltage (V_{out}) of the SM exhibits not only the switching ripples but also with some attenuation (Fig. 5(B)). When the 1-dB bandwidth is increased to 2 MHz, the V_{out} follows the input voltage (V_{in}) without attenuation, but the switching ripples still cannot be effectively suppressed (Fig. 5(D)). Furthermore, once the 1-dB bandwidth is increased to 8 MHz, the V_{out} follows the V_{in} with high fidelity and negligible ripples (Fig. 5(F)).

To further demonstrate the importance of having a wideband linear stage in the SM to meet the stringent linearity specs, the entire ET-PA using the monolithic SiGe PA is simulated with the RF/analog/digital co-simulation bench in ADS. The behavior model is used for the Op-Amp, while the realistic SPICE models are used for the PA and the other blocks of the SM. The inductor (L) of the buck converter is chosen around 40 µH here. The effect of the value of L on the SM design will be discussed in the next section. The simulated output error-vector-magnitude (EVM) of the ET-PA against different 1-dB bandwidths of the Op-Amp are plotted in Fig. 6 for the WiMAX 64QAM 8.75

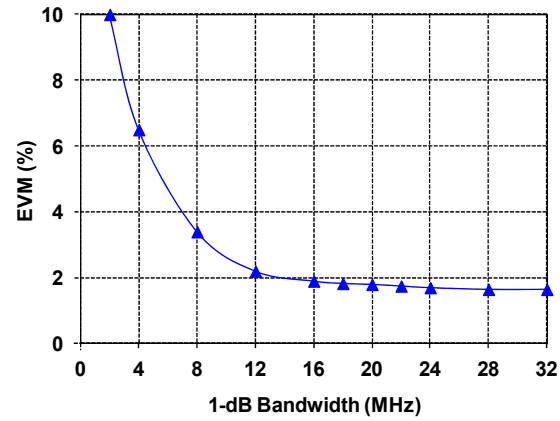

Fig. 6. Simulated output EVM of the ET-PA vs. 1-dB bandwidth of the Op-Amp for the WiMAX 64QAM 8.75 MHz signal. The behavior model is used for the Op-Amp, while realistic SPICE models are used for the SiGe PA and other blocks of the SM, P_{in} = 6 dBm, P_{out} = 16 dBm.

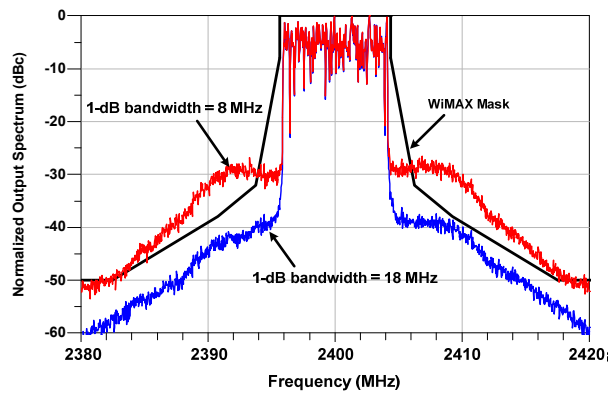

Fig. 7. Simulated output spectra of the ET-PA using different bandwidths of Op-Amp for the WiMAX 64QAM 8.75 MHz signal. The behavior model is used for the Op-Amp, while realistic SPICE models are used for the SiGe PA and other blocks of the SM. P_{in} = 6 dBm, P_{out} = 16 dBm.

MHz. As shown in Fig. 6, the EVM values of the ET-PA decrease as the *1-dB bandwidth* of the Op-Amp increases, and become saturated to ~1.8% after the 1-dB bandwidth of the Op-Amp becomes larger than 18 MHz. Fig. 7 shows the simulated output spectra of the ET-PA with different bandwidths of the Op-Amp. There is a large improvement on the adjacent channel power ratio (ACPR) when the 1-dB bandwidth of the Op-Amp increases from 8 MHz to 18 MHz, enabling the output spectrum passing the stringent WiMAX spectral mask specs. As indicated by Figs. 6-7, the required bandwidth of the SM needs to be at least 2x of the original signal bandwidth, while sufficiently suppressing the switching ripples.

2) *Switching Frequency of the Supply Modulator*

The average switching frequency of the SM shown in Fig. 4 is well analyzed in [7] and can be expressed as [6]:

$$f_{SW} = \frac{R_{sense}}{L} \cdot \frac{V_{dc}}{2h}\left(1 - \frac{V_{rms}^2}{V_{DD} \cdot V_{dc}}\right), \quad (3)$$

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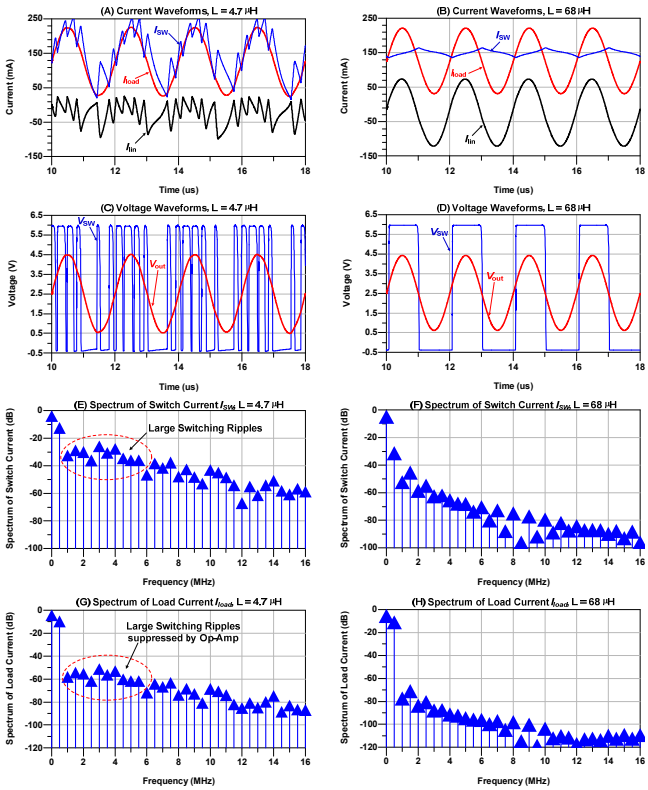

Fig. 8. SPICE simulated (A, B) current waveforms, (C, D) voltage waveforms, (E, F) spectra of the switching current I_{SW}, and (G, H) spectra of the output load current I_{load} of the SM using two different values of L (4.7 μH vs. 68 μH). The realistic SPICE models are used for the supply modulator. R_{load} = 22 Ω, the input voltage = 1.25+$sin(2\pi \cdot 500\text{kHz} \cdot t)$ V.

where V_{dc} and V_{rms} are the average and root-mean-square voltages of the output envelope signal, respectively; h is the hysteresis voltage of the comparator. In this design, the comparator LMV7219 has a pre-determined internal hysteresis h of 7-10 mV according to the data sheet and the SPICE simulations. Therefore, according to (3) the average switching frequency can now be mainly controlled by the value of L. The drawback of using a rather small L is that it usually generates more switching ripples at high frequencies, making the design of the linear stage more challenging [17].

Fig. 8 shows the SPICE simulated waveforms and spectra of the SM designed using two different values of L with an input waveform of 1.25+ $sin(2\pi \cdot 500\text{kHz} \cdot t)$ V. This time, the realistic SPICE models are used for all blocks of the SM simulations. The switching current I_{sw} supplies both DC and AC components of the load current (I_{load}) by using an L of 4.7 μH; a higher switching frequency and large switching ripples on the waveform of I_{sw} can be observed from Fig. 8(A). Such large switching ripples need to be largely suppressed or cancelled by the output current of the linear Op-Amp (I_{lin}), which can be clearly shown by the spectra of I_{sw} and I_{load} in Figs. 8(E) and (G). On the other hand, for the case of L= 68 μH, I_{sw} supplies only the DC component of I_{load}, while the AC component is taken care of by the linear Op-Amp, as shown in Fig. 8(B). Also, the spectra of I_{sw} and I_{load} for the case of L= 68 μH have smaller harmonics than those using L= 4.7 μH. These simulation

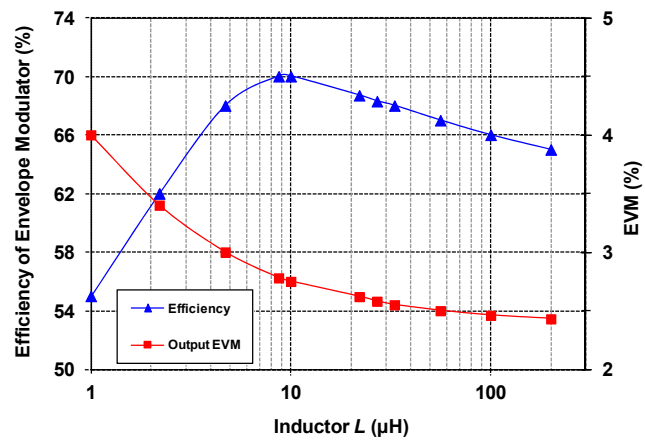

Fig. 9. Simulated efficiency of the SM and output EVM of the ET-PA using different values of L for WiMAX 64QAM 8.75MHz signal. Realistic SPICE models were used for the PA and SM. V_{DD}= 4.2 V, P_{out} = 17 dBm.

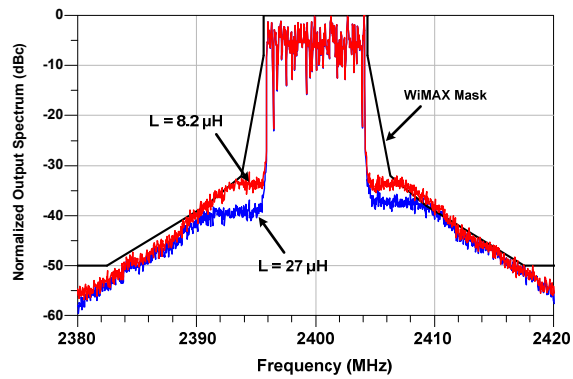

Fig. 10. Simulated output spectra of the ET-PA using different values of L for the WiMAX 64QAM 8.75 MHz signal. Realistic SPICE models were used for the SiGe PA and the EM. V_{DD}= 4.2 V, P_{out} = 17 dBm.

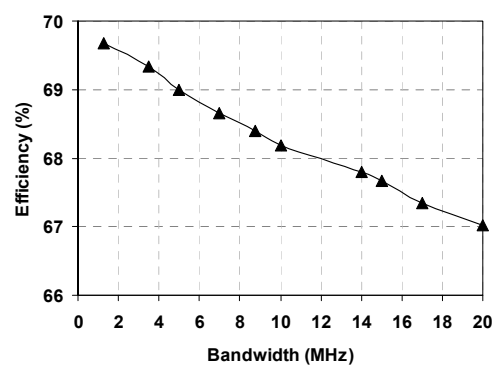

Fig. 11. Measured SM efficiency for different bandwidths of WiMAX 64QAM signals; V_{DD}= 4.2V, R_{load}= 22Ω, average output voltage = 2.3V

results indicate that the optimal L should be selected for not purely the highest efficiency, but also for the sufficient ripple suppression based on the limited bandwidth of the Op-Amp.

Fig. 9 shows the SPICE simulated efficiency of the SM and the EVM of the ET-PA using the SiGe PA (see Fig. 1). The realistic SPICE models are used for the SiGe PA and all blocks of the SM. From the pure view point of efficiency, the optimal L is 8.2 μH for the best efficiency. Smaller L results

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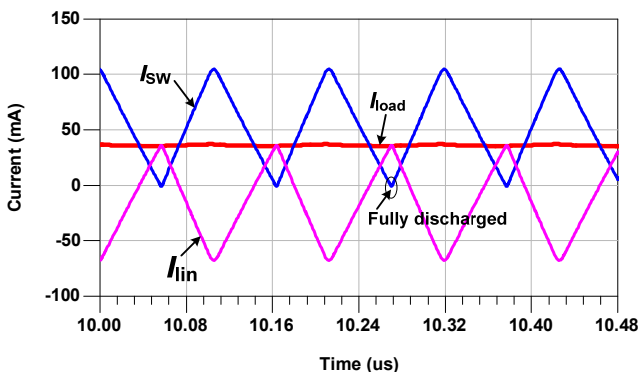

Fig. 12. SPICE simulated current waveforms of the discrete hybrid switching SM at the boundary of the discontinuous mode (L = 1.2 µH)

in higher switching frequency and significant switching loss. In addition, the EVM degrades with smaller L due to higher switching ripples. On the other hand, larger L makes the buck converter only able to supply the DC component of the load current, and in such a case the lower efficiency Op-Amp has to deliver the remaining AC contents (as illustrated in Fig. 8 (B)), leading to lower SM efficiency and thus lower overall efficiency of the ET-PA. A rather large L also causes high parasitic resistance to decrease its efficiency. Fig. 10 shows the SPICE simulated output spectra of the ET-PA using L of 8.2 µH and L of 27 µH, respectively. When the larger L (27 µH) is chosen, the ACPR is 4-6 dB better at the offset of 5-8 MHz from the center frequency with only ~2% lower efficiency (see Fig. 9).

Figs. 9-10 indicate that a small efficiency improvement may not be worthwhile if the linearity of the overall ET-PA has to be sacrificed. Therefore, the L of 27 µH is chosen in the design for our SM to achieve the best trade-off between efficiency and linearity. Fig. 11 shows the measured SM efficiency for different bandwidths of the WiMAX 64QAM signals. The SM efficiency only reduces by 2.5% when the signal bandwidth is increased from 1.5 MHz to 20 MHz.

When the output current is low, the inductor may be completely discharged at the "OFF" state of the buck converter before the switcher is turned on again, which is often called as the "discontinuous mode" for DC-DC converter design [25]. Therefore, another concern in the selection of the inductor value is to ensure the buck converter does not go into the discontinuous mode operation [25]. The boundary of the discontinuous mode occurs at where the output DC current (I_o) equals to one half of the peak-to-peak inductor ramp current ΔI (i.e., $0.5\Delta I = I_o$). For the stand-alone buck converter controlled by the conventional pulse-width modulation (PWM) scheme, the minimal L should be determined to avoid the discontinuous mode at the minimum DC output current ($I_{o,min}$) as [25].

$$L_{min} = \frac{(V_{DD}-V_{out,DC})\cdot D}{\Delta I\cdot f_{SW}} = \frac{(V_{DD}-V_{out,DC})\cdot V_{out,DC}}{2\Delta I_{o,min}\cdot f_{SW}\cdot V_{DD}}, \quad (4)$$

where $V_{out,DC}$ is the output DC voltage, D is the duty cycle, and f_{SW} is the switching frequency determined by the PWM

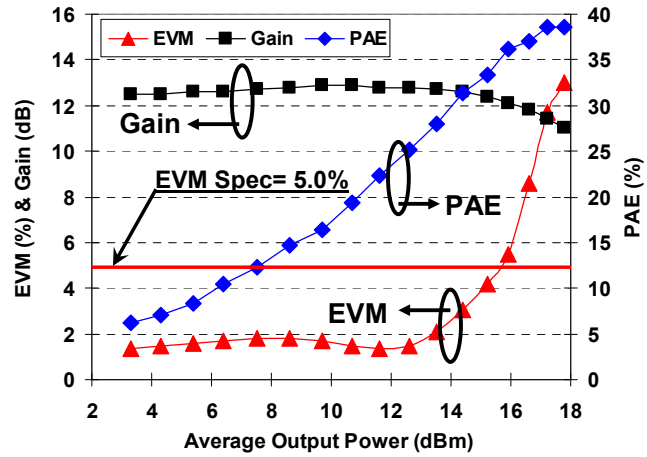

Fig. 13. Measured EVM, gain and PAE vs. average P_{out} of the stand-alone SiGe PA at V_{CC} of 3.6 V for WiMAX 64QAM 8.75MHz signal at 2.3 GHz

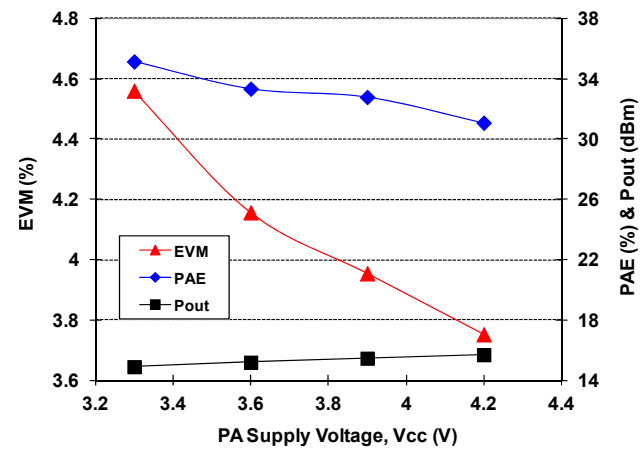

Fig. 14. Measured EVM, PAE and P_{out} vs. V_{CC} of the stand-alone PA for the WiMAX 64QAM 8.75 MHz signal at 2.3 GHz. P_{in} = 3 dBm

control scheme. For example, if the SM were to be implemented using the conventional PWM control scheme for this ET-PA, one could obtain the $V_{out,DC}$ = 2.3 V, $I_{o,min}$ = 33 mA (i.e., at R_{load} = 70 Ω presented by the SiGe PA as shown in Fig. 2). Therefore, the minimal inductor value calculated based on (4) would be ~16 µH for a PWM-controlled buck-converter, assuming f_{SW} =1 MHz.

For the hybrid switching SM in this work, the peak-to-peak inductor ramp current ΔI is limited under $2h/R_{sense}$, which is not related with the inductor value [7]. This is because once the switching current I_{SW} is h/R_{sense} lower than the load current I_{load}, the hysteresis comparator will immediately sense the current difference and turn on the switcher again, assuming the switcher can response fast enough [7]. In the practical SM design, however, the switcher is not ideal due to its intrinsic gate capacitance and resistance, therefore it may not respond fast enough with a high switching frequency, and this frequency is directly determined by the inductor value. In addition, the hysteresis window h increases with higher input slew rate [26]. The SPICE simulations show that h is ~ 7 mV with the input voltage ramp below 0.2 V/µs, but increases to ~ 43 mV with

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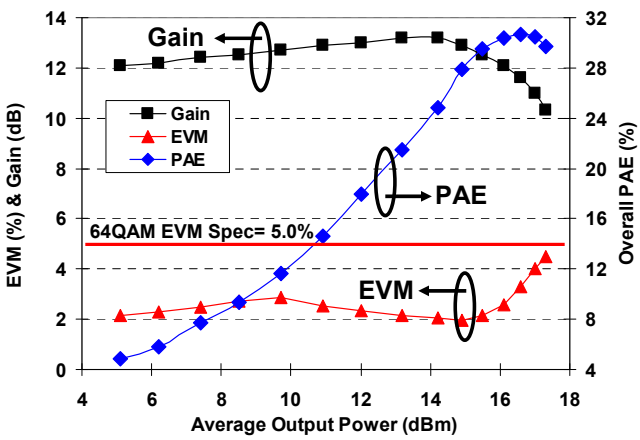

Fig. 15. Measured EVM, gain and overall PAE vs. P_{out} of the ET-PA system for the WiMAX 64QAM 8.75 MHz signal at 2.3 GHz; V_{DD} = 4.2 V

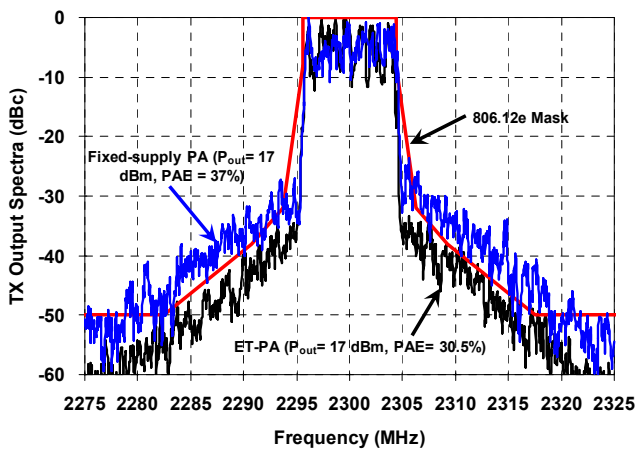

Fig. 16. Measured output spectra of the ET-PA and fixed-supply PA at P_{out} of 17 dBm for WiMAX 64QAM 8.75 MHz at 2.3 GHz

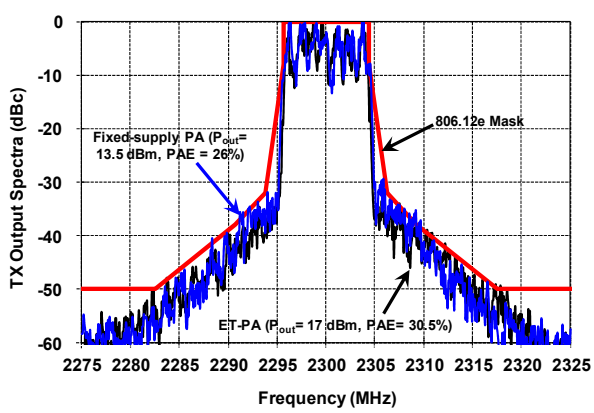

Fig. 17. Measured output spectra of the ET-PA (P_{out}=17 dBm) and fixed-supply PA (P_{out}=13.5 dBm) for WiMAX 64QAM 8.75 MHz at 2.3 GHz

the input voltage ramp of 4 V/µs. According to the simulation, the minimal L is 1.2 µH to avoid the discontinuous mode operation for our SM. Fig. 12 shows the SPICE simulated current waveforms of the hybrid SM at the boundary of the discontinuous mode.

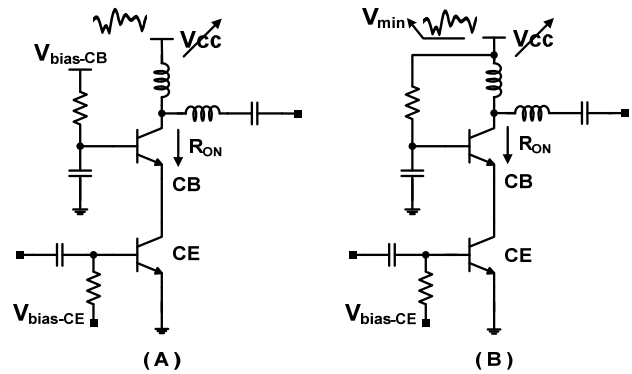

Fig. 18. Simplified schematics: (A) the conventional constant biased cascode SiGe PA; (B) the proposed self-biased cascode SiGe PA

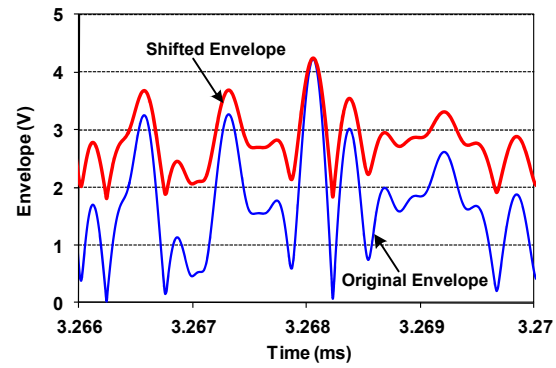

Fig. 19. Simulated envelope waveforms of the WiMAX 64QAM 5 MHz signal before and after using the proposed envelope shifting method

III. Comparison of ET-PA and Stand-Alone PA

A. *Efficiency and Linearity of the Stand-Alone PA*

First, the stand-alone SiGe PA with fixed-supply voltage is tested to serve as a reference for the comparison with the ET-PA. Fig. 13 shows the measured gain, PAE and EVM vs. P_{out} for the WiMAX 64QAM 8.75 MHz signal (PAR = 10.5 dB) at 2.3 GHz. The PAE of the SiGe PA reached 39% at the P_{out} of 17.8 dBm, but with a rather high output EVM of 11.7% (the EVM spec of WiMAX 64QAM is 5.0% or -26 dB). At P_{out} of 16 dBm, the stand-alone PA already violates the lenient EVM spec. Increasing V_{CC} could reduce the EVM as shown in Fig. 14, but at the cost of lower efficiency.

B. *Efficiency and Linearity of the ET-PA*

The discrete SM discussed earlier is used to modulate the supply voltage (V_{CC}) of the PA to form an ET-PA. No DPD is used in the measurement. The ET-PA operates at V_{DD} of 4.2 V. Fig. 15 shows the measured EVM, gain and overall PAE of the ET-PA. The overall PAE (or the composite PAE) of the ET-PA includes the power consumption of the SM. The overall PAE of the ET-PA is 30.5% at P_{out} of 17 dBm with an EVM of 4.4%. Fig. 16 shows the output spectra of the ET-PA and the stand-alone PA with a fixed supply. At P_{out} of 17 dBm, the ET-PA passes the stringent WiMAX 64QAM mask, while the fixed-supply PA fails the spectral

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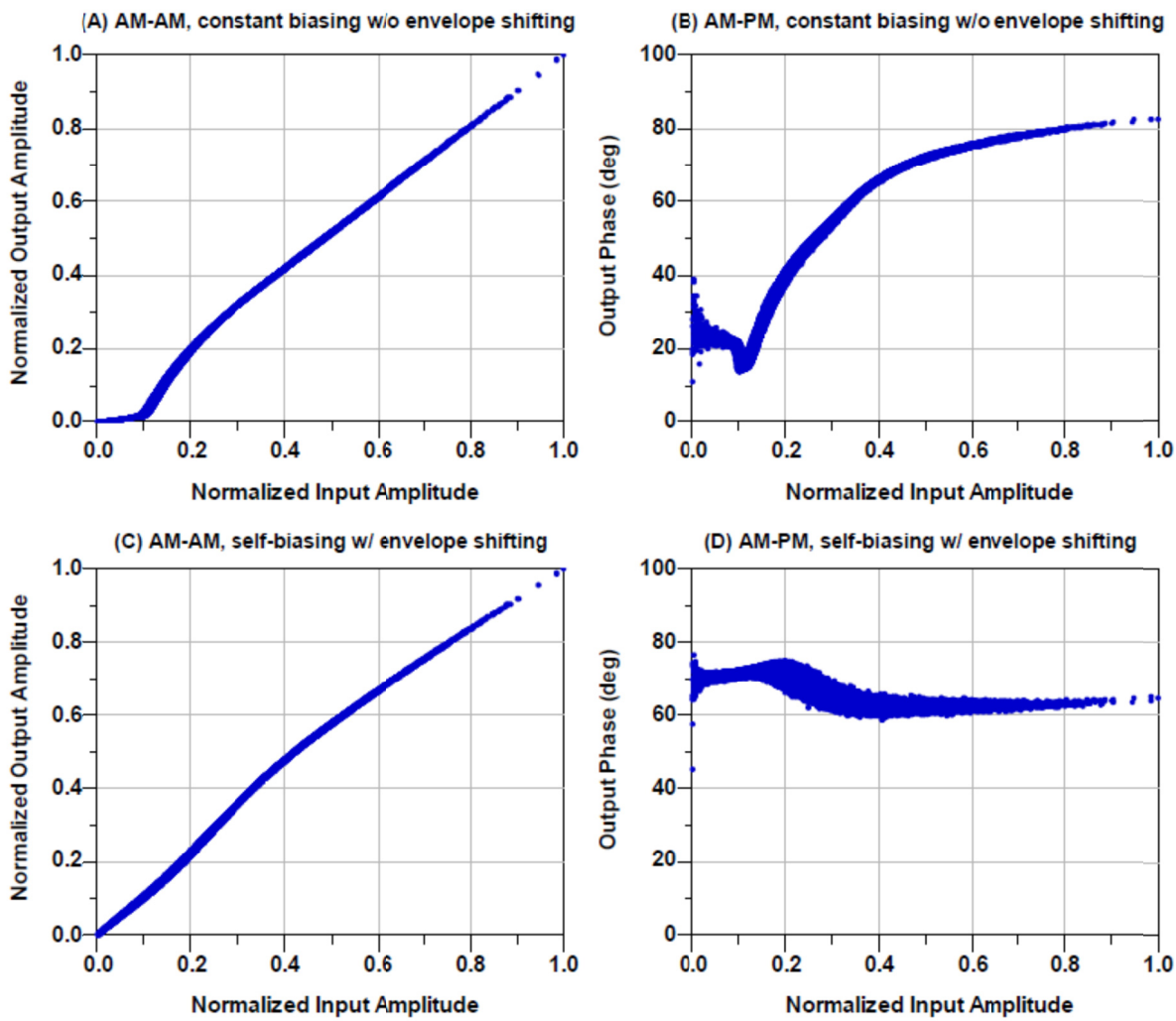

Fig. 20. Simulated AM-AM and AM-PM characteristics of the cascode ET-PA for the WiMAX 64QAM 5 MHz signal: (A, B) conventional constant biased cascode PA without the envelope shifting, (C, D) proposed self-biased cascode PA with the envelope shifting

mask badly. Note that the ET-PA operates at its P_{2dB} point at P_{out} of 17 dBm. Fig. 17 shows that the maximum linear P_{out} of the fixed-supply PA is only ~13.5 dBm in order to pass the WiMAX spectral mask, leading to a PAE of only ~26%.

IV. Fully Monolithic BiCMOS ET-PA

The ET-PA using a SiGe PA and a discrete SM has achieved the promising performances, which prompts us to integrate the SM into the PA to form a low cost solution for handset applications. In this section, a monolithic ET-PA in a 0.35 µm SiGe BiCMOS technology will be presented.

A. Differential Cascode SiGe PA Design

To improve the reliability for Si-based PAs, the cascode topology was used for our PA to relieve the voltage stress on the power devices. In addition, the differential structure is used to reduce the grounding parasitic inductance for higher gain and P_{out}. Although this differential cascode SiGe PA has been presented in [3], here we still highlight its self-biasing structure and our proposed envelope shaping function (i.e., envelope shifting in [3]), since both affect the design of the CMOS SM discussed in the next section.

Fig. 18 shows the simplified schematics of the constant biased cascode PA and the proposed self-biased cascode PA. The envelope waveforms of the WiMAX 64QAM 5 MHz signal before and after the envelope shifting are shown in Fig. 19. Fig. 20 shows the simulated AM-AM and AM-PM characteristics of the ET-PA using the conventional constant biased cascode PA and the proposed self-biased cascode PA with the envelope shifting. In the simulation, the SPICE models provided by the design kit were used for the cascode PA. To only focus on the PA structure and envelope shaping function, an ideal SM (i.e., a gain block without any distortion) is used in this particular simulation to eliminate any distortion from the SM. As shown in Fig. 20, the AM-AM characteristic of the conventional cascode PA under the ET operation has a large distortion at the low instantaneous input amplitude due to the knee effect [10], [27], and its AM-PM characteristic has a large phase difference of ~65°. Both

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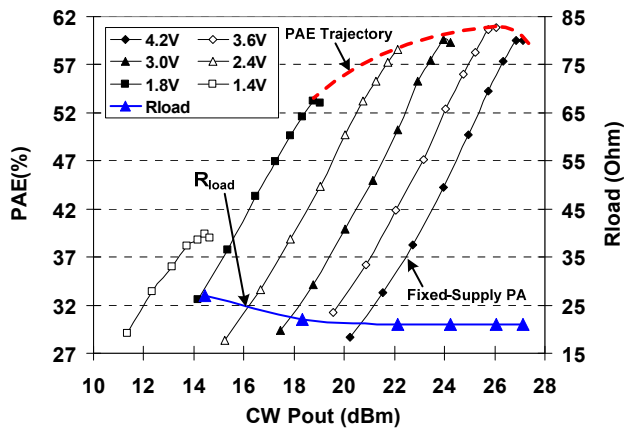

Fig. 21. The PAE vs. P_{out} of the self-biased cascode SiGe PA (measured at different V_{CC} at the CW mode) and the R_{load} seen by the SM

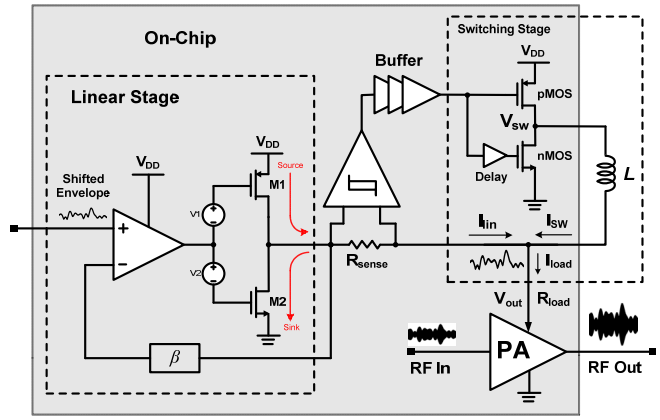

Fig. 22. Simplified block diagram of the CMOS SM integrated with the differential cascode SiGe PA on the same die

AM-AM and AM-PM distortions can be diminished by using the proposed self-biased PA with the envelope shifting.

Following the same procedure as Section II, Fig. 21 shows the measured PAE against P_{out} of the self-biased cascode PA at various V_{CC} in the CW mode. As the V_{CC} is modulated from 1.8 V to 4.2 V, the PAE of the ET-PA varies between 53% and 61%. The R_{load} presented by the self-biased cascode PA stays constantly at ~20 Ω, when V_{CC} is swept from 1.8 V to 4.2 V. The value of R_{load} is important for the analysis of the power losses for the SM.

B. Integrated CMOS Supply Modulator

Fig. 22 shows the simplified block diagram of the CMOS SM integrated with the cascode SiGe PA. The SM was designed in the TSMC 0.35 µm BiCMOS process, but no bipolar devices were used. The SM utilizes the same hybrid switching structure as described in Section II. Although the same SM was presented in [3], [4], its power dissipation has not been discussed in details. In this paper, with our special envelope shaping function and cascode self-biasing PA, we will discuss how our SM can achieve high efficiency with a relatively low average switching frequency.

1) Linear Stage of the Supply Modulator

The linear stage uses a folded cascode amplifier with gain-boosting to meet the slew-rate requirement of the LTE and WiMAX envelope signals [3]. The output stage of the Op-Amp has a common source structure biased at the class-AB mode for a good compromise between distortion and quiescent power dissipation [3]. The efficiency of the class-AB output stage is the key for achieving high efficiency of the linear stage. Since all the DC current is supplied by the switching stage, the loss of the class-AB stage is almost zero at the DC level of the output signal. When the output transistors (M1 and M2) begin to source or sink current, the voltage across them will cause power loss, expressed as:

$$P_{pMOS} = (I_{load} - I_{SW}) \cdot (V_{DD} - V_{out}) \quad (5)$$

$$P_{nMOS} = (I_{SW} - I_{load}) \cdot V_{out} \quad (6)$$

Fig. 23 (A-D) shows the current and voltage waveforms of the supply modulator with and without the envelope shifting for the LTE 16QAM 5 MHz signal. When the load current (I_{load}) is higher than I_{SW}, the pMOS device (M1) of the class-AB stage sources the current; and when I_{load} is lower than I_{SW}, the nMOS device (M2) of the class-AB stage sinks the current. The instantaneous power losses from M1 and M2 against the output voltage (V_{out}) can be clearly seen from Fig. 23 (E) and (F). The average power loss from M1 is reduced from 38 mW to 17 mW by using the envelope shifting technique, while the average power losses from M2 are very close in both cases. According to (5), the envelope shifting mainly reduces the power loss from M1 for the class-AB stage, because it pushes V_{out} closer to V_{DD} (i.e., V_{DD}–V_{out} becomes smaller as shown in Fig. 23 (B)). On the other hand, even though V_{out} becomes higher with the envelope shifting method, the linear stage sinks less current than the case without envelope shifting (see the comparison between Fig. 23 (C) and (D)). This helps to maintain the power loss from M2 roughly the same as the case without using envelope shifting.

2) Switching Stage of the Supply modulator

In this cascode ET-PA system, the envelope shifting method reduces the AC magnitude of the envelope signal, while raising its DC content (see Fig. 19). Therefore, the switching stage supplies more current to the load than the case without envelope shifting, and its efficiency becomes more dominant to the overall efficiency of the supply modulator. It is well-known that there are at least two main mechanisms of power loss in the switching stage: (1) conduction loss; and (2) switching loss. The MOSFET switchers need to be sized for the minimal total power loss (i.e., the conduction loss plus the switching loss). The conduction loss is caused by the on-resistance of the switching FETs when they are conducting, expressed as [11]

$$P_{cond_loss} = D \cdot \overline{I_{SW}}^2 \cdot R_{on,p} + (1 - D) \cdot \overline{I_{SW}}^2 \cdot R_{on,n}, \quad (7)$$

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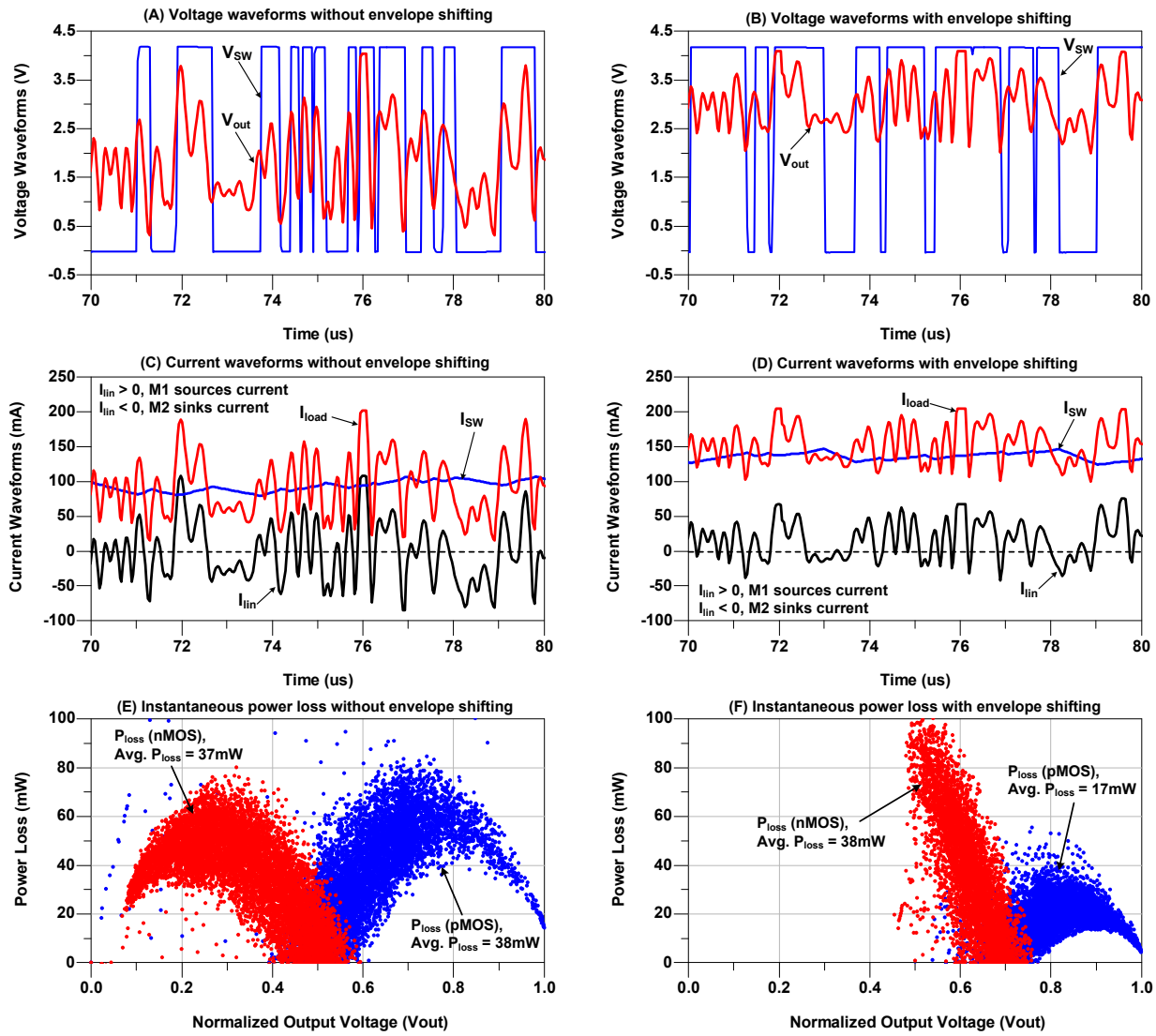

Fig. 23. SPICE simulated waveforms and power losses of the CMOS SM for the LTE 16QAM 5 MHz signal before and after using the envelope shifting method: (A, B) voltage waveforms, (C, D) current waveforms, and (E, F) instantaneous power losses from the class-AB output stage of the Op-Amp. R_{load} = 20 Ω

where D is the average duty cycle of the switching pulses, I_{SW} is the average output current of the buck converter, $R_{on,p}$ is the on-resistance of the pMOS switcher, and $R_{on,n}$ is the on-resistance of the nMOS switcher. The conduction loss is not dependent on the switching frequency and is inversely proportional to the device width. In the design of this integrated CMOS supply modulator, the sizes of pMOS and nMOS of the buck converter are chosen as 20 mm × 0.4 µm and 7 mm × 0.4 µm, respectively. According to the SPICE simulation, $R_{on,p}$ and $R_{on,n}$ are ~0.26 Ω and ~0.27 Ω, respectively. The I_{SW} is 140 mA when driving the R_{load} of 20 Ω presented by the PA. Therefore, the conduction loss of the buck converter is ~10.5 mW according to (7).

The switching loss is caused from the simultaneous current and voltage overlap during the device on/off time (i.e., called crossover loss in [11]), as well as the loss due to its input and output capacitances during switching [7], [9], [11]. The crossover loss can be minimized by adding a delay at the gate of the nMOS as the work in [9] (see Fig. 22). Once the crossover loss is minimized, the switching loss can be expressed as [11]:

$$P_{sw_loss} = \left(C_d V_{dmax}^2 + C_g V_g^2\right) \cdot f_{SW}, \qquad (8)$$

where C_d is the total drain capacitance, C_g is the total gate capacitance, f_{SW} is the average switching frequency, V_{dmax} is the high level voltage at the drain (i.e., 4.2 V), and V_g is the turn-on voltage of the MOSFET switchers (i.e., 4.2 V). The switching loss is related to both the device width and the switching frequency. A smaller device width can have smaller gate and drain capacitances, but causing higher conduction loss due to its higher on-resistance. For the selected MOSFET switchers, the total drain capacitance and

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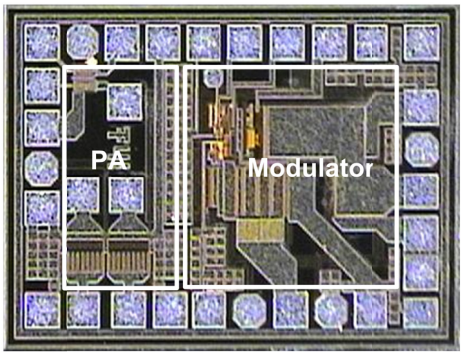

Fig. 24. Chip micrograph of the fully monolithic BiCMOS ET-PA

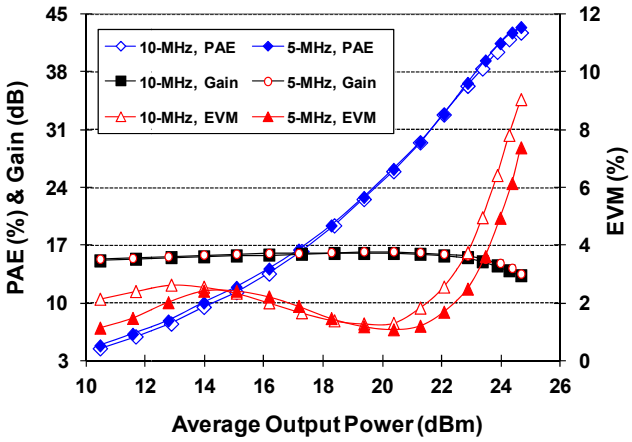

Fig. 25. Measured gain, EVM and overall PAE of the ET-PA for the LTE 16QAM 5 MHz and 10 MHz signals, V_{DD} = 4.2 V

gate capacitance are ~51 pF and ~52 pF obtained from the SPICE simulations, respectively. Additionally, according to the SPICE simulation, the average switching frequency is 0.9 MHz with an inductor of 56 µH. Therefore, the calculated conduction loss is ~1.6 mW from (8). By comparing the values of conduction loss and switching loss, the conduction loss is dominant to the total power loss of the switching stage with a relatively low switching frequency. It is worth noting that the switching frequency of our SM is relatively lower than those of other works [9]-[11], due to the large inductor purposely chosen for low switching ripples and a relaxed linear stage bandwidth as discussed in Section II.

V. Performances of the Full Monolithic ET-PA

In this section, we will verify that our design approach of the cascode ET-PA can achieve a high overall efficiency with a relatively low switching frequency of the SM, thus the spectral mask can be satisfied without any need of DPD techniques. The overall ET-PA at V_{DD} of 4.2 V is evaluated for the LTE 16QAM signals with the PAR of 7 dB. The die picture of our fully monolithic ET-PA is shown in Fig. 24, fabricated in the TSMC 0.35 µm SiGe BiCMOS technology. The total chip size is 1.5 × 1.1 mm^2. No DPD will be used in the measurement.

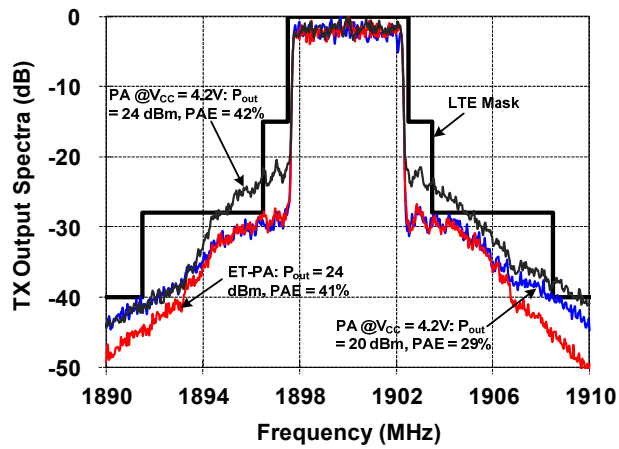

Fig. 26. Measured output spectra of the ET-PA and the stand-alone fixed supply PA for the LTE 16QAM 5 MHz signal

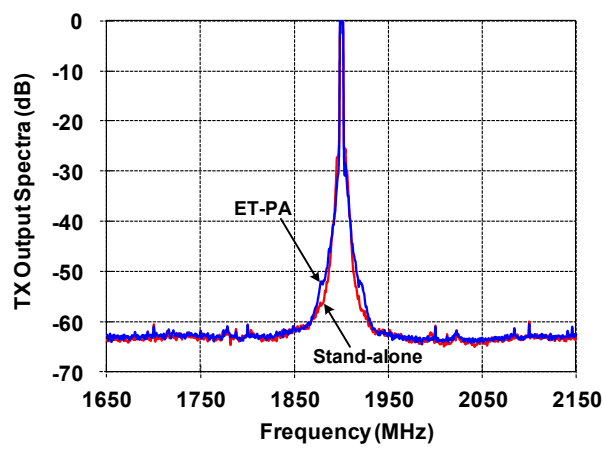

Fig. 27. Measured far-out output spectra of the ET-PA and stand-alone PA for the LTE 16QAM 5 MHz signal, both at P_{out} of 24 dBm

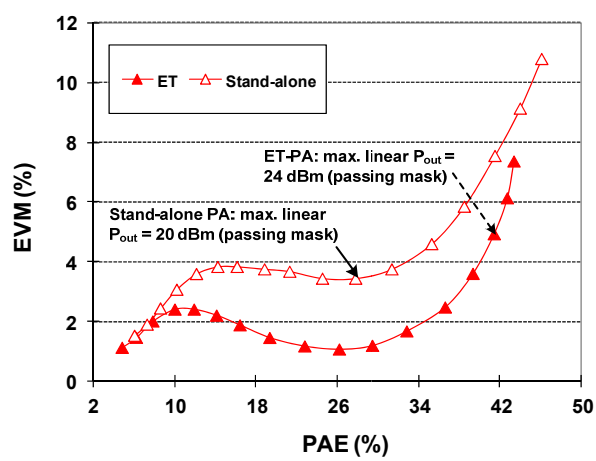

Fig. 28. Efficiency-linearity comparison for the ET-PA and the stand-alone PA for the LTE 16QAM 5 MHz signal

Fig. 25 shows the measured EVM, gain and overall PAE of the ET-PA for both the LTE 16QAM 5 MHz and 10 MHz signals at 1.9 GHz. While keeping the EVM below 5%, the

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TABLE I. SUMMARY OF OUR FULLY MONOLITHIC ET-PA AND THE COMPARISON WITH STATE-OF-THE-ART ET/POLAR PAS

	Freq. (GHz)	V_{DD} (V)	P_{out} (dBm)	*Overall PAE	EVM	Modulation	DPD	Technology
[9]	2.4	3.3	20	28%	5%	WLAN 64QAM 20 MHz	Yes	0.18 µm SiGe BiCMOS
[10]	1.88	3.3	29	46%	---	WCDMA 3.84 MHz	No	PA: 2 µm InGaP/GaAs SM: 0.13 µm CMOS
	1.88	3.3	23.9	34.3%	2.98%	WiMAX 64QAM 5	No	
[12]	2.535	6	29	43%	1.9%	LTE 16QAM 20 MHz	Yes	PA: GaAs HBT SM: 0.15 µm CMOS
[22]	2.0	3.3	19.6	22.6%	2.5%	WLAN 64QAM 20 MHz	No	0.13 µm CMOS
[24]	1.92	2.1	15.3	22%	1.5%	WiMAX 64QAM 5 MHz	Yes	0.13 µm SOI-CMOS
[27]	1.85	5	28.9	42.2%	2.69%	LTE 16QAM 10 MHz	No	PA: 2 µm InGaP/GaAs SM: 0.18 µm CMOS
[28]	1.88	3	24.22	38.6%	3.64%	WiBro 16QAM 5 MHz	No	PA: 2 µm InGaP/GaAs SM: 0.13 µm CMOS
[29]	2.535	3.6	25.8	32.3%	3%	LTE 16QAM 10 MHz	No	PA: 2 µm InGaP/GaAs SM: 0.35 µm CMOS
[30]	2.35	3.5	24.7	25.5	4.5	LTE 16QAM 20 MHz	No	0.18 µm SiGe BiCMOS
This work	1.9	4.2	24	41%	4.9%	LTE 16QAM 5 MHz	No	0.35 µm SiGe BiCMOS
			23.4	38%	4.9%	LTE 16QAM 10 MHz		

Note: * Overall PAE includes the efficiency of the SM

maximum linear P_{out} is 24 dBm with an overall PAE of 41% for the LTE 5 MHz signal. In order to achieve the same EVM for the LTE 10 MHz signal, the maximum linear P_{out} needs to be 0.6 dB lower than the case of LTE 5 MHz, resulting in an overall PAE of 38% at P_{out} of 23.4 dBm. When the ET-PA is backed off 0.5 dB from the maximum linear P_{out} levels, better EVMs of 3.6% and 3.7% can be achieved with overall PAEs of 39% and 37% for the LTE 16QAM 5 MHz and 10 MHz signals, respectively.

The output spectra of the ET-PA and the stand-alone fixed supply PA (V_{CC} = 4.2 V) are plotted in Fig. 26. The ET-PA successfully passes the LTE spectral mask at P_{out} of 24 dBm. However, at the same P_{out} of 24 dBm, the stand-alone fixed-supply PA fails the LTE spectral mask, forcing it to be backed off by at least 4 dB. The maximum linear P_{out} of the stand-alone PA is, therefore, only 20 dBm with a PAE of 29%. The linear P_{out} and PAE are thus 4 dB and 12% lower than those achieved by the ET-PA, respectively. Fig. 27 plots the far-out output spectra of the ET-PA and the stand-alone PA measured without any external filtering. Compared with the stand-alone PA, the ET-PA has little spectral regrowth at the offset of 20-30 MHz from the center frequency, but no strong spur appears at the offset frequency above 50 MHz. Such a spurious emission performance was achieved due to the low average switching frequency of the SM. To further demonstrate the advantages of the ET-PA, Fig. 28 compares the measured EVM of the ET-PA and the stand-alone PA against the PAE values. The ET-PA has a better EVM with the same PAE. Table I provides the performance summary of our fully monolithic ET-PA together with the state-of-the-art results.

VI. CONCLUSION

The complete design path towards our fully monolithic BiCMOS ET-PA has been presented. A discrete hybrid switching SM was first implemented to study the effects of its switching frequency and bandwidth limitation to the overall ET performance. The same circuit configuration was used to design our CMOS SM integrated with the self-biased cascode SiGe PA under our proposed envelope shaping function. By analyzing the power losses of the CMOS SM for our special ET operation, we showed that high efficiency can still be achieved with a relatively low average switching frequency, which helped to improve the overall ET linearity. At 1.9 GHz, our BiCMOS ET-PA achieved 24/23.4 dBm with the overall PAE of 41%/38% for the LTE 16QAM 5/10 MHz signals, respectively. The EVM below 5% and the LTE spectral mask were both satisfied without any need of DPD techniques. The literature survey indicates that our design achieved one of the highest efficiency for Si-based ET PAs, approaching those III-V semiconductor PAs for broadband mobile applications.

ACKNOWLEDGMENT

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