Newly Developed Low Power Tristate Buffers for Low-power and High Performance Applications with Limited Energy Resources

Karol Niewiadomski and Dietmar Tutsch

Chair of Automation and Computer Science - University of Wuppertal

Wuppertal, Germany

Email: {karol.niewiadomski, tutsch}@uni-wuppertal.de

Abstract—The adaptiveness of integrated electronics is a key feature in current and future mobile applications. Despite the continuous improvement of battery capacity, reconfiguration capabilities of integrated electronics are an inevitable step to cover the rising demand for processing power. Without any further adjustments for efficiency, power consumption becomes a limiting factor for runtime performance. Field programmable gate arrays provide suitable configuration capabilities, but lack of efficient power saving design measures. To overcome this challenge, different approaches were proposed in recent research activities. A substantial contributor to battery load are general purpose input output circuits, which serve the purpose of connectivity. In this paper, we present a modified tristate buffer, which is a key component in a typical general purpose input output design. Modifications for active power reduction and standby leakage current suppression are applied at circuit level to achieve a better energy efficiency. This new tristate buffer design is compared to already existing designs. Furthermore, this newly developed design is modified for either higher output impedance or faster switching frequency. All modifications done are explained and discussed by putting a focus on their pros and cons.

Keywords–Tristate buffer; Battery lifetime; Power reduction; Leakage suppression; Output impedance.

I. Introduction

Mobile computing is the driving factor for innovations on the field of instant availability of information. It is expected to have the same computing performance in mobile devices like smartphones, tablets and even sometimes in vehicles, as known from high performance computers in very demandable applications [1]. Vehicles exhibit a rising degree of functions supporting autonomous driving which require fast evaluation of different driving situations in real time. This comes along with a urgent demand for continuously rising computing power, whilst batteries do not experience comparable proceedings in terms of higher capacities. Field programmable gate arrays (FPGAs) offer vast reconfiguration capabilities way beyond their earlier use case as glue logic [2]. Depending on the size of the FPGA in terms of number of configurable logic blocks (CLBs), different designs can be loaded into the FPGA and, therefore, synthesized by an intelligent routing of CLBs. However, in most cases implemented designs do not use all resources of reconfigurability, leading to a waste of energy due to leakage currents flowing through blocks in standby mode. Unused blocks inside an integrated circuit, which is intended to be used in mobile applications, should be switched off and only turned on again, if more resources are needed. Different design methodologies can be used on different hierarchical levels to realize a fine-grain and coarse-grain approach for reduction of consumed power. This can be achieved by an

efficient combination of design decisions at circuit level, e.g., power gating, clock gating, dynamic voltage scaling, etc. [3]. A breakdown of a CLB into its single blocks reveals further possibilities to modify the schematics towards the intended low power purpose, e.g., optimization of configuration random access memory (CRAM) [4] and data flip-flops (D-FFs) [5]. In addition to that, investigations have shown that a noticeable amount of power is dissipated by the general purpose input outputs (GPIOs), which serve as a generic input / output device for integrated circuits [6]. As the number of reconfigurable / adaptive electronics in mobile applications is expected to grow continuously, we believe that special attention in terms of improvements or redesign should be allocated to these special circuitry, which can not be neglected for the sake of well interconnectivity in integrated circuits.

In this paper, we investigate a standard tristate buffer design on its most significant characteristics, which are dynamic power consumption, standby leakage current and $highZ$ capabilities. In Section II, we give an overview about related work and key aspects of dependencies between performance and power consumption. In Section III, we introduce a reference design of a tristate buffer and discuss typical characteristics in operation and standby. In Section IV, a newly implemented tristate buffer is presented and its benefits for energy sensitive usage are introduced. In Section V, we compare the simulation results of the different investigated designs. In Section VI, all previous discussions are summarized and concluded.

II. Related Work

GPIOs are used in almost every integrated circuit as an interface to communicate with peripheral circuitry. These elements are designed for receiving data as inputs and to transmit data as output to other connected devices. Therefore, tristate buffers are bidirectional circuits with the ability to receive and to transmit logic signals by the same input/output pin. Due to this important functions, GPIO play a major role in consumed area of a chip and power consumption in each complex design [7]. Despite the importance of these crucial parts in each chip, GPIOs were optimized either for high speed or considerable driver capabilities in the past. Concepts for designing special function registers (SFRs) inside a GPIO have been presented [8] for handling difficulties of the rising design complexity of these blocks. These concepts are innovative and certainly of considerable value for future GPIO design, however, power aspects are not covered. Further research work focussed on the improvement of GPIO configurability by adding event-capture modules to the standard GPIO design [9]. This feature provides options to configure some registers by the user whilst power aspects are not in scope. IO transistors are used to

connect each chip to peripheral circuitry and should be taken into consideration when leakage currents shall be reduced. Thus, leakage optimization of IO transistors was handled by research activities in the past [10]. This is an important step ahead but a GPIO consists of further parts, which should be also carefully analyzed when overall power improvements are desired. Additional research activities have been focussing on maximizing circuit speed while still keeping the amount of dissipated power at an comparably acceptable level [11]. The results of this work were further elaborated and extended in advanced work, resulting in the implementation of low-power transmitter and receivers [12]. These implementations achieve good results for both, speed and low-power, but can not be categorized as real GPIOs. For that reason, the research activities of the work described in this paper were focusing on the development of a low-power GPIO. Operating frequency was not of first priority, but was also considered in alternative design, which also will be introduced in this paper. Figure 1 illustrates a simplified block diagram of a FPGA without any additional hard processing cores.
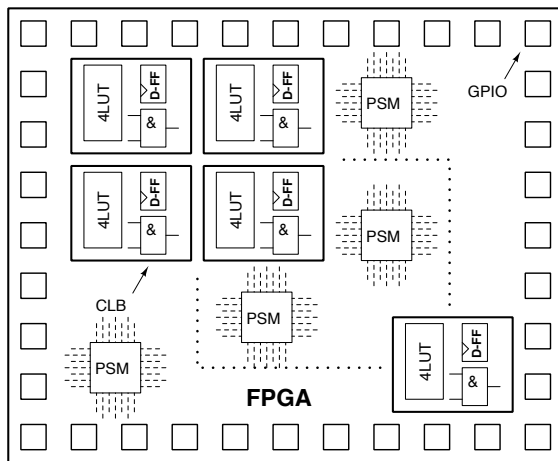

Figure 1. Simplified FPGA structure

As illustrated in Figure 1, all CLBs of this simplified internal hierarchy are surrounded by GPIO blocks. For the sake of simplicity, all further blocks, e.g., switching matrices (PSM), are displayed in a simplified way. In complex systems, several FPGAs may drive an internal bus for different purposes, e.g., data exchange, leading to potential conflicts when different circuits try to write different logic values to the same bus line.

Figure 2 highlights the described conflict and depicts a situation, in which two different FPGAs, connected to the same 4 bit data bus, drive the same line with different values: whilst FPGA1 drives one signal line of the bus with a logic 1 or V_{dd}, FPGA2 tries to do same but with a logic 0. The consequence is a floating voltage on the interconnection signal line, which is difficult to predict and an undefined state. For this reason tristate buffers play an important role inside each GPIO, since they offer one special output state beside their functionality to pass a logic value from the input to the output node: $highZ$, also called high impedance. By enabling this state, a tristate buffer cuts off the connection between its input and output node and, therefore, prevents an undesired throughput from the inputs of the GPIO inside an FPGA to the interconnection bus. So in general, we can identify three aspects to be of relevance
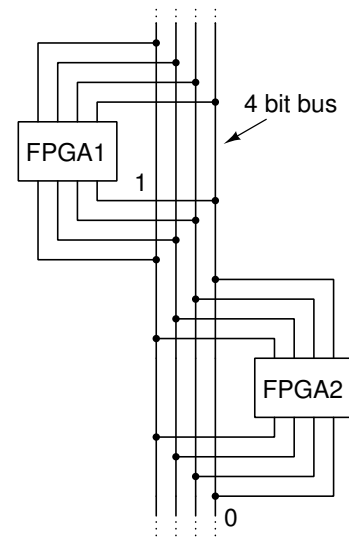

Figure 2. Interconnection bus

for optimization in terms of energy efficiency:

- Subthreshold / standby leakage
- Active power consumption
- $highZ$ behavior

Each of these bullet points has to be addressed by a careful analysis of parameters, which are responsible for different behavior and, therefore, also different results or performance of the circuit in scope. Subthreshold leakage current can be characterized by the following equations [13][14]:

$$J_{DT} \propto A(\frac{V_{ox}}{T_{ox}})^2 \tag{1}$$

$$I_{leak} \propto \frac{W}{L_{eff}} e^{(V_{GS}-V_{t0}-\gamma V_{SB}+\eta V_{DS})/nV_t}(1-e^{-\frac{V_{DS}}{V_t}}) \tag{2}$$

Equation (1) explains that a higher oxide thickness T_{ox} will subsequently lead to a lower current density J_{DT}, which is a favored effect for our purposes as we intent to limit undesired current flows as good as possible. On the other hand, (2) highlights the dependency of a subthreshold current I_{leak} to different factors, e.g., the transistor length L_{eff}, the gate-source voltage V_{GS} and the source-body voltage V_{SB}. On the other hand, active power consumption P_{dyn} depends on various factors showed in the following equation:

$$P_{dyn} = \alpha C_{load} V_{dd}^2 f_{Clk} \tag{3}$$

Equation (3) [15] shows that for significant reduction of consumed battery power several factors, e.g., the switching activity α, the load capacitance C_{load}, the supply voltage V_{dd} and the operating frequency f_{Clk} have to be designed in a way to keep P_{dyn} as low as possible. Some factors like C_{load} can not be easily controlled, however other factors can be adapted in a better way directly at circuit level. Last but not least, the $highZ$ attributes of a tristate buffer play an important role due to their ability to decouple this buffer from the remaining

signal chain. A careful design of the output transistors inside a tristate buffer offers heavy impact on this ability. Nevertheless, it should be stated here, that priority was put on low power characteristics of our newly implemented design. Measurement of the $highZ$ state with different output voltages was done after evaluating power consumption of all investigated designs. Furthermore, all measurements were compared against each other to figure out, which design performs best in general.

III. Tristate buffer cell design

The basic purpose of a buffer circuit is to forward the input value with a certain delay to the output node. Some applications might require the addition of a delay time for synchronizing different data paths. The easiest way to understand the basic function of a buffer is to imagine the logic function of two inverter in series. A tristate buffer adds a third, important feature to this functionality: the $highZ$ state. For a better understanding of the circuit's function, a tristate inverter is shown in Figure 3.
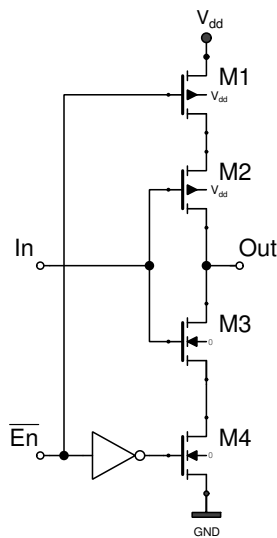
Figure 4. Standard design of a tristate buffer

were done at an operating frequency of $200MHz$ and with standard settings for all transistors' dimensions ($120nm$). Since all analyzed designs are not dynamic logic inheriting a dedicated Clk input, the operating frequency was modulated into the switching events of $\overline{En}$. The results of the first simulation run with active inputs are shown in Figure 5 and also displayed in Table I and Table II. This simulation was followed by further tests for alternative circuit states with the intention to build up a baseline database for further comparisons.

Figure 3. Tristate inverter

As long as $\overline{En}$ provides a logic *LOW* at the respective input node, the transistors *M1* and *M4* are turned on and subsequently provide a direct path to the voltage source V_{dd} and GND. As a consequence, the transistors *M2* and *M3* work as an inverter and, therefore, invert all signals applied to In. On the other hand, if $\overline{En}$ turns to *HIGH*, *M1* and *M4* are turned off and cut-off the internal transistors *M2* and *M3* from the supply voltage and ground path. In this special case, the voltage at the output node *Out* is floating and undefined. This means that in dependence of this floating voltage, only a very small current will flow either as leakage current from the tristate inverter into the circuitry connected to *Out* or from the load into the tristate inverter to GND. By adding one additional *nMOS* and *pMOS* transistor, the discussed tristate inverter can be modified to a tristate buffer, which is shown in Figure 4.

Different aspects of this tristate buffer's behavior have been investigated during simulations by a $90nm$ TSMC (Taiwan Semiconductor Manufacturing Company) technology and a Cadence toolchain (INCISIVE 6.1.5). All simulations, serving the purpose investigating the circuit's dynamic performance,
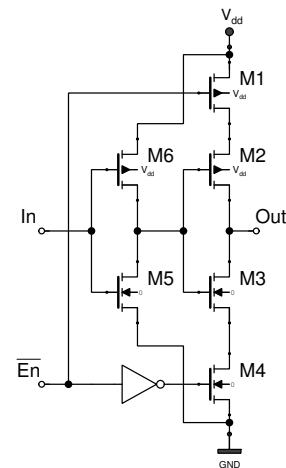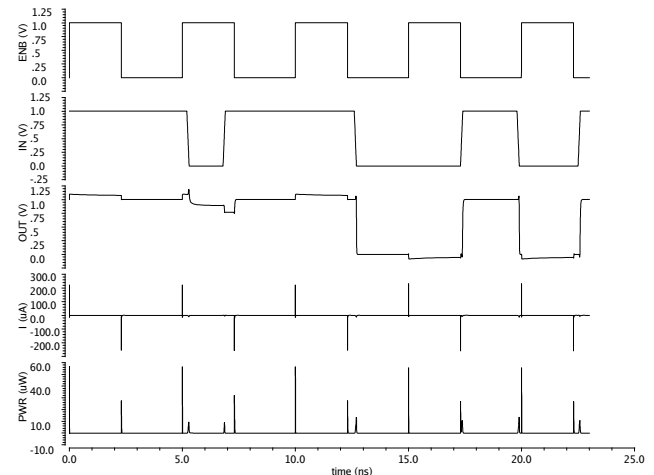
Figure 5. Simulation results of dynamic behavior of a standard tristate buffer

TABLE I. SIMULATION RESULTS (PWR)

Design type	Average Power nW	Max. Power uW	Min. Power pW
Reference	245	56.75	103.8

TABLE II. SIMULATION RESULTS I_{Vdd}

Design type	Avg. Current nA	Max. Current uA	Min. Current nA
Reference	215.2	230.5	261.4

The simulation results display the correct function of this tristate buffer, which directly passes the input value to *Out*

whenever $\overline{En}$ is set to *LOW*. Once $\overline{En}$ applies a logic *HIGH* to the cutoff transistors, the voltage level at *Out* starts to float and swings between voltage levels above V_{dd} and below $0V$ (GND). These floating voltages are not defined and also indicate that the whole circuit is in *highZ* mode. Active power dissipation is of high importance for the estimation of required energy resources, but regardless of these results it is also obligatory to have a closer look on the standby power characteristics when the circuit is lead into an idle phase or put completely into standby mode. This means that the data input is inactive and $\overline{En}$ active. The simulation results are shown in Figure 6.
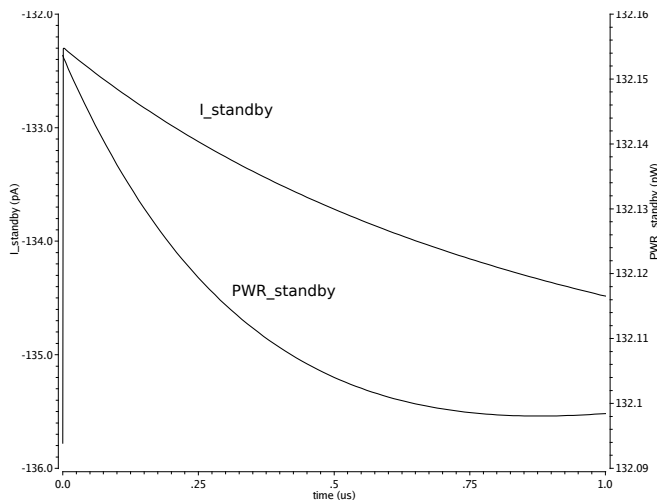

Figure 6. Simulation results of idle standby results

For this analysis and for a better observation of the standby current, the simulation runtime was set to $1\mu s$. The simulation curves of both, standby current and standby power dissipation, show the discharging process of all internal parasitic capacitances after powering on the circuit at the very beginning of the simulation process. Both, standby current and the allocated dissipated power, continuously decrease over time, resulting in an average leakage current I_{leak} of $133.6pA$ and a related average power dissipation of $132.1pW$.

The remaining aspect to be considered at this point is the behavior of the reference tristate buffer in *highZ* mode after setting $\overline{En}$ to *HIGH*. First of all, it should be stated here that there is no unambiguous answer on this question, since this depends on the voltage, which will be applied by the load to the output node *Out* of the tristate buffer. In addition to that, there is always a small throughput from the input node on the output in case that the tristate buffer in *highZ* is still stimulated with input date, which might be a realistic situation when the related control logic fails. Thus, two different situations, active and inactive inputs, must be considered. Based on the assumption that the voltage applied to *Out* may vary from $0V$ to$1V$, a dc sweep simulation was done. The results of both test runs are displayed in Figure 7.

Active input data has a remarkable influence on the circuit's capabilities to decouple its internal switching events to the output node. In case of setting the input node to a $0V$ and, therefore, making it 'inactive', Figure 7 reveals a sweetspot in terms of output impedance and which is closely allocated
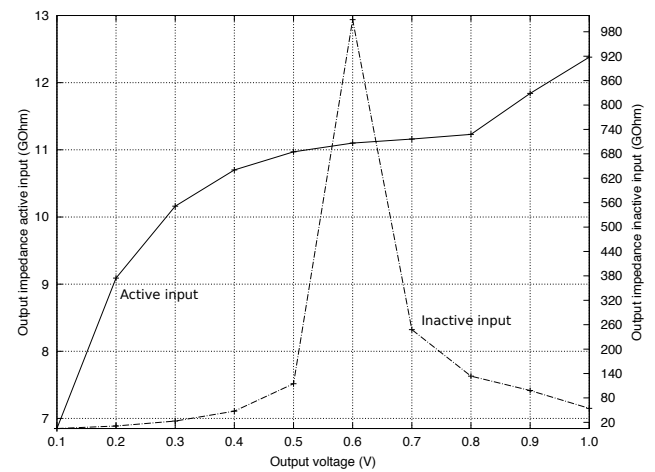

Figure 7. Simulation results of output impedance in *highZ* state

to almost $V_{dd}/2$. Having this striking high output impedance ($\approx 1.01T\Omega$) at this voltage range is a desirable situation, since this implements an almost perfect balance between current source and current sink. If input data are applied to *In*, a drop the output impedance can be observed after simulation. Even with turned of decoupling transistors *M1* and *M4*, the throughput originating from the buffer's input is strong enough to lower the impedance at *Out*. Therefore, a stronger decoupling mechanism would probably lead to better results.

IV. MODIFICATIONS

A careful analysis of the reference tristate buffer pointed out that there is still room left for different improvements. Thus, a noticeable adaption of circuits for sensitive low-power application can only be achieved by a synergy of different power savings measures for imaginable operating states.

A. Power Gating

On our way to develop a low-power tristate buffer, the implementation of a 'hold'-mechanism for standby-phases was an inevitable step. The difficulty here was the fact, that this design does not imply clocked inputs, which could have been gated. Instead of this, a more stringent design technique was applied: power-gating. This modification can be applied in different ways, by adding a gating transistor between the supply voltage and the circuit or by inserting a transistor between *GND* and all internal nodes. A third alternative comes along with a combination of both design modifications and can be found in Figure 8 (transistors *M5* and *M10*).

The addition of two transistors to a design with a total number of eight transistors <u>before</u> this modification means an increase 20% and a high probability for penalty in terms of area consumption. Regardless of the chosen technology for synthesis and allocated continuous proceedings in technology node shrinking, a higher number of transistors is always considered as a drawback. On the other hand, this modification is responsible for a noteworthy limitation of leakage current running through the design under test (DUT), since we achieve a complete decoupling of the tristate buffer vor V_{dd} and *GND* respectively.
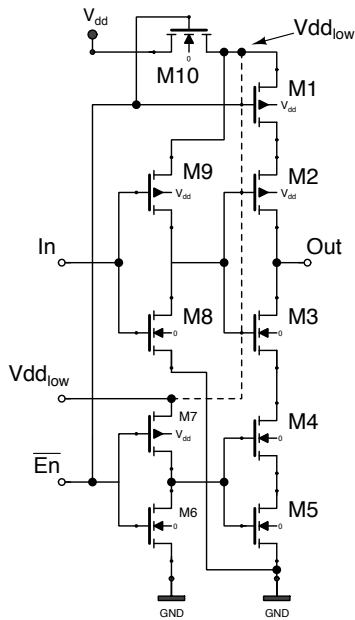
Figure 8. Low-power tristate buffer

B. Leakage Current Reduction

A reasonable extension of power gating is the use of special transistors with a higher oxide thickness T_{ox}, which can be also seen in (1), where T_{ox} is in the denominator and, therefore, has the ability to limit the electrons tunneling through the transistor's gate connector. This results in a reduction of the leakage current in idle / standby state. Despite these benefits it should be mentioned that high T_{ox} transistors have a slower switching frequency than standard T_{ox} do. Hence, adding these transistors should be carefully waived taking a decision upon it. In our case, *M5* and *M10* have an increased T_{ox} than the remaining transistors have for keeping the penalty in performance degradation as low as possible.

C. Subthreshold Current Reduction

Whilst power gating is an effective method for a total shutdown of a circuit, there should be an alternative for measurable reduction of a current flowing through a transistor with an applied gate-source voltage V_{gs} below the threshold. voltage V_{th}. This led to the decision to apply high V_{th} transistors, which have the ability to cut off subthreshold electron tunneling. This method might have a negative impact on the maximum operating frequency and should be carefully applied. Nevertheless, these special transistors can not be neglected during the design of low power designs. All internal transistors, except the gating transistors, have been replaced by their hight V_{th} counterparts and simulated.

D. Multi Supply Voltage

An operating circuit in low power applications should not only be optimized for static power reduction but also for energy efficiency in active mode. As shown in Equation 3, the supply voltage has a vast influence on the overall dissipated power. It's obvious that the best approach would be to decrease the global supply voltage V_{dd}, but might lead to the necessity of additional level restorers for a smooth signal transmission

to other circuitry. An alternative is the careful partial supply voltage reduction within a design after analyzing certain parts of a design, which could be powered by a lower V_{dd}. On the other hand, lowering V_{dd} comes along with a slower computation time of the input values, therefore, a smaller supply voltage $V_{dd_{low}}$ was only applied to the internal inverter *M6* and *M7*. In principle, there are two different ways how to generate $V_{dd_{low}}$: this can be realized by an external voltage source (illustraed by the additional voltage source V_{ddlow} in Figure 8) or by exploiting internal voltage nodes (illustrated by the dashed line in Figure 8). The second option shows its beauty by an inherent voltage reduction automatism. Once $\overline{En}$ goes *HIGH M10* is turned off and, therefore cutting off *M7* from V_{dd}, but keeps the internal inverter still working. Minor adaptions to the width of *M7* have to made due to the decreased internal supply voltage. Nevertheless, both options work well with the low power tristate buffer.
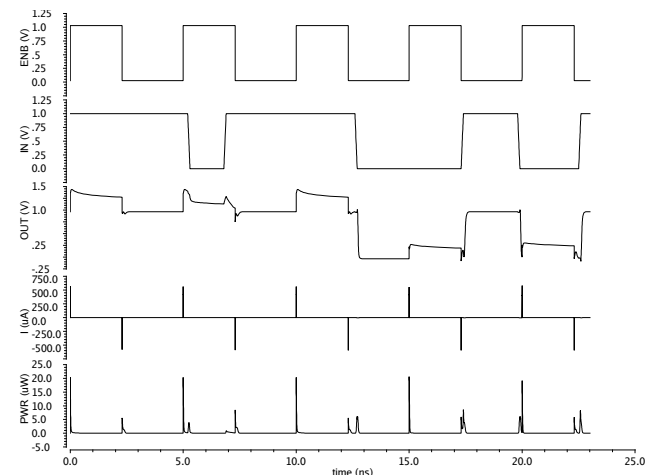

Figure 9. Simulation results of dynamic behavior of the low-power tristate buffer

Figure 9 shows the dynamic behavior of the low power tristate buffer. Compared to the simulation curves shown in Figure 5, it can be seen that the low power tristate buffer is superior in terms of dissipated power during active runtime. The related simulation results are summarized in Table III and Table IV.
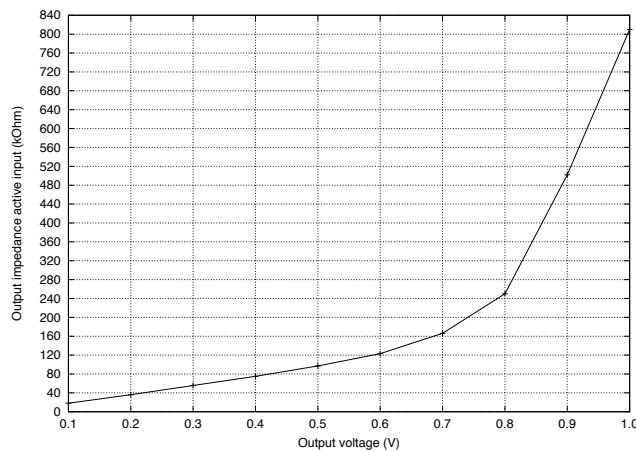
TABLE III. SIMULATION RESULTS (PWR)

Design type	Average Power (*nW*)	Max. Power (*µW*)	Min. Power (*pW*)
LP tristate	191.3	29.72	22.36

TABLE IV. SIMULATION RESULTS I_{Vdd}

Design type	Avg. Current (*nA*)	Max. Current (*µA*)	Min. Current (*nA*)
LP tristate	225.8	194.8	206.9

Furthermore, an analysis of the standby behavior revealed an improved average leakage current I_{leak} of $24.1pA$ and a related average power dissipation of $22.04pW$. As a final step, the *highZ* characteristic was investigated for having a better comparison to the reference design. The simulation results are displayed in Figure 10.

Figure 10. Output impedance in *highZ* state (low power tristate buffer)

Figure 11. Low-power tristate buffer with swapped output transistors

Figure 12. Transient analysis of modified low power tristate buffer

In contrast to the reference tristate buffer, the newly implemented tristate buffer shows a different behavior. First of all, the output impedance shows a smaller order of magnitude ($G\Omega \rightarrow k\Omega$) and in addition to this, the output curve strongly depends on the voltage at the output node and reveals a proportional dependency. The higher the voltage at *Out* is, the higher the output impedance will be. Despite the fact that the low power tristate buffer's active *highZ* curve has a smaller order of magnitude, the evaluated results are still acceptable and give an evidence about the appropriateness for the usage as an connecting element in complex designs. These results could be improved by modifying the gate lengths of the output transistors *M2* and *M3*. The downside of this modification would lead to necessary modifications of the manufacturing process, but which can be easily handled by modern technology nodes. By picking up this thought, the question for an alternative design may arise. The internal buffer of the low power tristate buffer, consisting of transistors $M2, M3, M8$ and $M9$, provides a direct signal propagation path from *In* to *Out*, regardless of the built-in decoupling measures from the supply voltage and *GND* and, in the worst case, vice versa. Like mentioned before, tweaking the gate length of these transistors, especially of $M8$ and $M9$ would be a suitable way to raise resistance of each MOSFET, but this should be rather treated like the last option. Hence, anticipating any external throughput on internal nodes can be achieved by swapping the transistors of the internal (and simple) core logic with the cut-off switches, shown in Figure 11.

Now, the circuit is still similar to its predecessor shown in Figure 8 but features some mandatory adaptions. First of all, the internal buffer, which was placed right in the centre of the predecessor's circuit before, is now split up into the transistors $M1, M4, M8$ and $M9$. So, the idea here is that the second inverter of the internal buffer, implemented of $M1$ and $M4$, is now 'pulled apart' and flanked by transistors ($M2, M3, M5$ and $M10$), which serve as cut-off switches to V_{dd} and GND. All previously described energy saving measures have been applied here in the same way and simulated, respectively, to all tests done before. The simulation results can be seen in Figure 12.

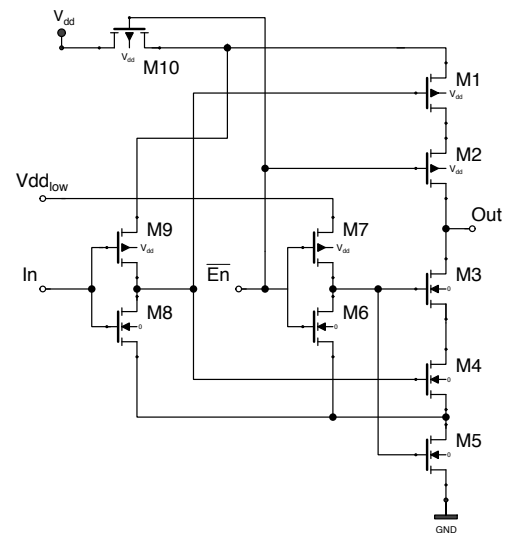As expected, the modified low power tristate buffer works fine and transmits correctly all input data in normal operation mode. Activation of the *highZ* mode works fine as well, by driving the output voltage to a not specified, floating voltage value. The 'kink' of *Out* during the falling edge if *In* goes back to the fact that the input signal switches *after* right after normale operation mode was activated by *ENB* switched from $1 \rightarrow 0$. Transient analysis in standby mode is pictured in Figure 15. An extended simulation with a transient analysis of $1ms$ is shown in Figure 14. After the verification of the correct function, the next step was to evaluate the circuit's power loss and to compare it with the previous design.

Compared to the results displayed in Table III and Table IV, it can be seen that the average power consumption is around 28.6% higher than before. But it should be taken into consideration that the internal inverter ($M6$ and $M7$) is still powered by V_{dd} and not by a lower, internal supply voltage. So, a few adjustments needs to be done here to figure out how this can be improved towards a lower power loss. Investigations of this circuits behavior have been made by scaling Vdd_{low} from the original $1V$ down to $500mV$ and are shown in Figure 16. This picture is a snapshot from the full simulation and all curve progressions in this figure depict a $1 \rightarrow 0$ transition while
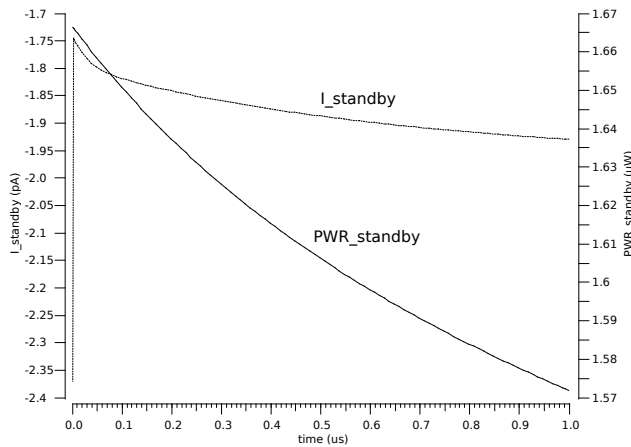
Figure 13. Transient analysis of modified low power tristate buffer in standby mode
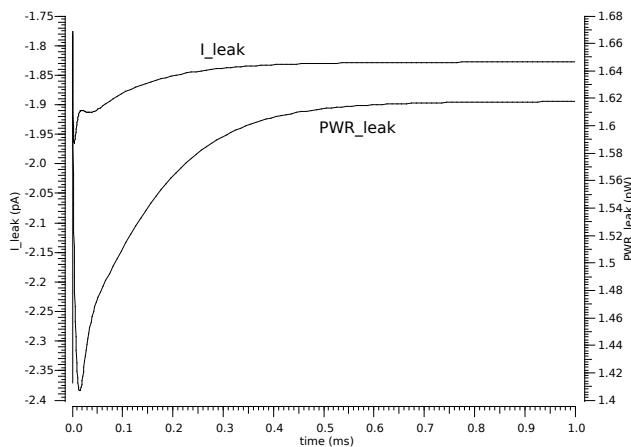

Figure 14. Extended simulation time of power dissipation and leakage current in power-off mode of the modified low power tristate buffer

leaving *highZ* mode and entering normal operation mode. It can be clearly seen how a lower internal supply voltage of the embedded inverter impacts signal propagation. Whilst lowering the supply voltage from $1mV$ to $800mV$, the penalty in signal delay is approximately $77ps$, further decreasing of Vdd_{low} down to $600mV$ leads to a higher penalty of approximaltey $622ps$. Going further down to 50% ($500mV$) of the original supply voltage, the correct function is not provided any more as a reliable inversion of *IN* gets disrupted.

TABLE V. SIMULATION RESULTS (PWR)

Design type	Av. PWR (nW)	Max. PWR (μW)	Min. PWR (pW)
LP tristate	268	19.81	17.69

TABLE VI. SIMULATION RESULTS I_{Vdd}

Design type	Av. Current (nA)	Max. Current (μA)	Min. Current (nA)
LP tristate	133.2	563.8	585.8

As expected, the modified low power tristate buffer works fine and transmits correctly all input data in normal operation mode. Activation of the *high Z* mode works fine as well, by

driving the output voltage to a not specified, floating voltage value. The 'kink' of *Out* during the falling edge if *In* goes back to the fact that the input signal switches *after* right after normale operation mode was activated by *ENB* switched from $1 \rightarrow 0$. Transient analysis in standby mode is pictured in Figure 15. An extended simulation with a transient analysis of $1ms$ is shown in Figure 14. After the verification of the correct function, the next step was to evaluate the circuit's power loss and to compare it with the previous design.
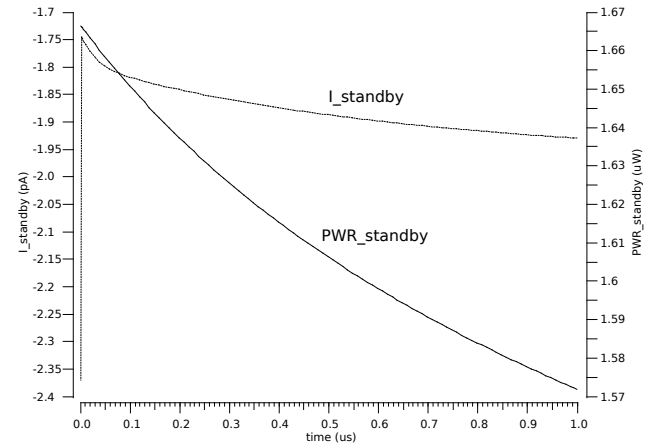

Figure 15. Transient analysis of modified low power tristate buffer in standby mode

Compared to the results displayed in Table III and Table IV, it can be seen that the average power consumption is around 28.6% higher than before. But it should be taken into consideration that the internal inverter ($M6$ and $M7$) is still powered by V_{dd} and not by a lower, internal supply voltage. So, a few adjustments needs to be done here to figure out how this can be improved towards a lower power loss. Investigations of this circuits behavior have been made by scaling $V_{dd_{low}}$ from the original $1V$ down to $500mV$ and are shown in Figure 16. This picture is a snapshot from the full simulation and all curve progressions in this figure depict a $1 \rightarrow 0$ transition while leaving *high Z* mode and entering normal operation mode. It can be clearly seen how a lower internal supply voltage of the embedded inverter impacts signal propagation. Whilst lowering the supply voltage from $1mV$ to $800mV$, the penalty in signal delay is approximately $77ps$, further decreasing of Vdd_{low} down to $600mV$ leads to a higher penalty of approximately $622ps$. Going further down to 50% ($500mV$) of the original supply voltage, the correct function is not provided any more as a reliable inversion of *IN* gets disrupted.

However, what is encountered at this point is a typical trade-off between power consumption and operating speed. Thus, the important aspect here is to make a distinction between thinkable target application of the device during development and then to put an appropriate nucleus on one these applications. Since energy efficiency comes first in the scope of this research work, the decision made was to set Vdd_{low} to $600mV$ and to continue further investigation about the circuit's characteristics. So, the next question to look up for was to see how the output impedance in *high Z* will look like. Similar to earlier investigations, simulation were carried out to check the modified low power tristate buffers capabilities in terms of decoupling itself from a bus. The outcome of
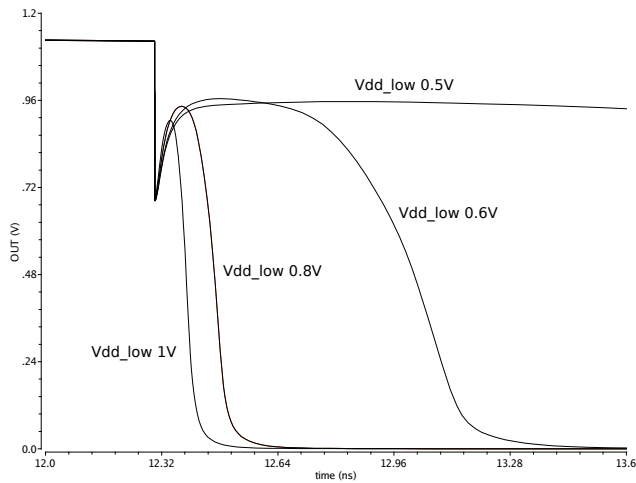
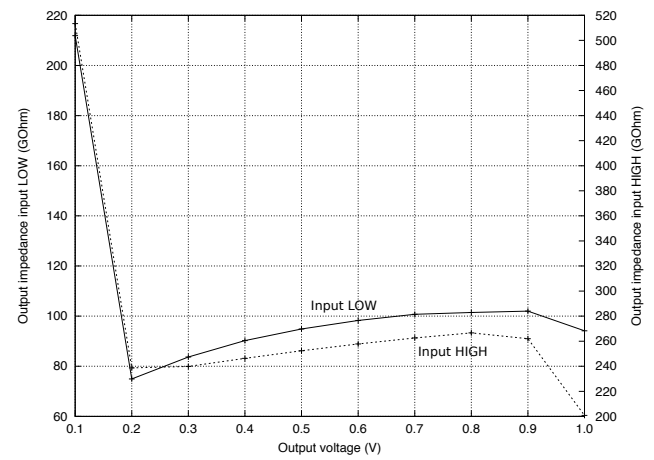Figure 16. Transient analysis of modified low power tristate buffer with scaled Vdd_{low}

Figure 18. Output impedance in highZ state (modified low power tristate buffer)

these simulations are shown in Figure 18. In direct comparison to Figure 17 the output curves of the modified low power tristate buffer show an obviously more synchronized tracing, regardless of the applied input data. Since this is a feature of an improved decoupling mechanism from the output node(s), it can be considered as beneficial characteristic. For the next step, it was interesting to see how the circuits behave and compete in worst case scenarios. This is summarized in Table VII and in Table VIII.

TABLE VII. OUTPUT IMPEDANCE $(G\Omega)$

Type \In/Out	0V \0V	0V \1V
Ref	6.85	12.38
LP	189	95.69
Mod. LP	211.9	94.16

TABLE VIII. OUTPUT IMPEDANCE $(G\Omega)$

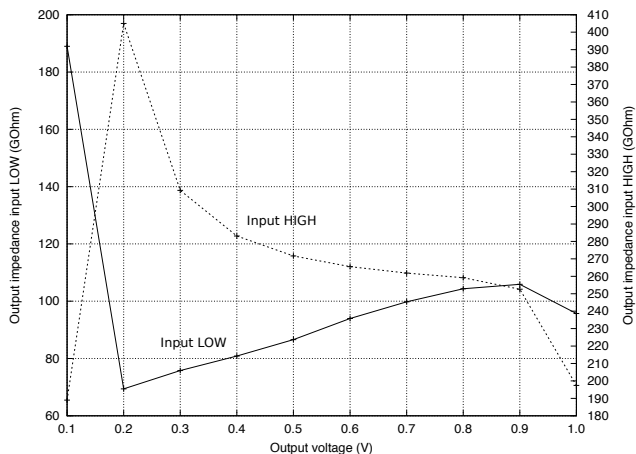| Type \In/Out	1V \0V	1V \1V
Ref	4.8	54.3
LP	189	197.4
Mod. LP	513.4	200.78

Figure 17. Output impedance in *highZ* state (low power tristate buffer)

After completing the low-power and *highZ* evaluation of the introduced circuits, the question came up whether it is still possible to achieve further improvements with a complete redesign of the common architecture. The circuit of this new buffer is illustrated in Figure 19.
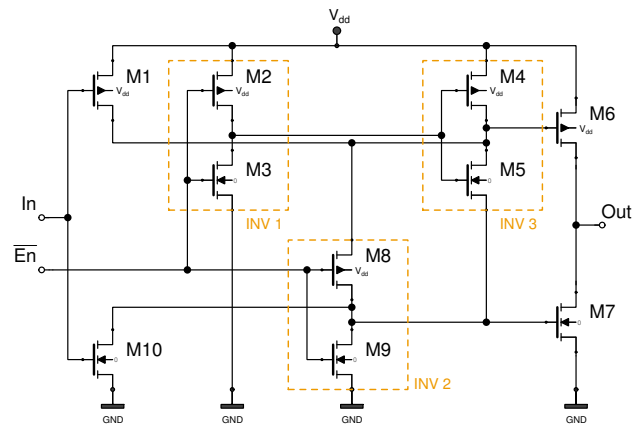

Figure 19. Alternative Tristate Buffer

The basic idea of this new, alternative (AT) tristate buffer is to have a separate decoupling of each of the four transistors ($M1$, $M6$, $M7$ and $M10$), which form the core buffer by additional inverters ($INV1$, $INV2$ and $INV3$). Buffer functionality is ensured by two inverters, consisting of $M1$ and $M10$ (input inverter) as well as $M6$ and $M7$ (output inverter). For normal operation mode $\overline{En}$ is turned to *LOW*, which leads to turning on the pMOS transistors $M2$ of $INV1$ and also $M8$ of $INV2$. So, $M2$ pulls the output of $INV1$ to V_{dd} and, therefore, turns on $M5$ of the next inverter ($INV3$). In parallel to this, $\overline{En}$ also turns on $M8$ of $INV2$, which short-circuits the drain node of $M1$ to the drain of $M10$. The short-circuit loop, which ensures this functionality is displayed in Figure 20.

By closing the internal shirt-circuit loop the output node of the input inverter is connected to input node of the output inverter, which leads to the desired buffer function in case that no *highZ* mode is demanded. If $\overline{En}$ is turned to *HIGH*,
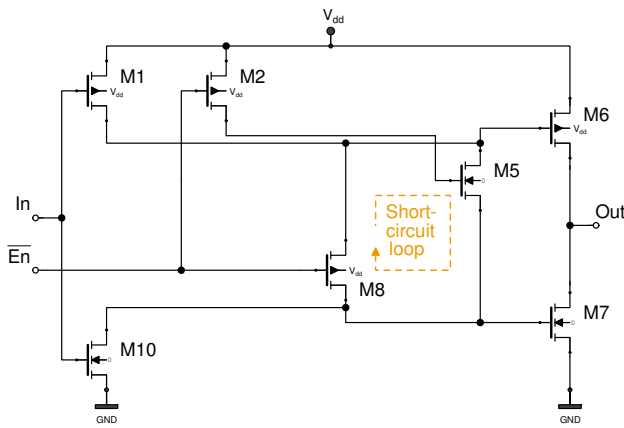
Figure 20. Short-circuit loop in normal operation mode

Figure 22. Transient analysis of alternative tristate buffer

transistor $M3$ of $INV1$ is activated and subsequently pulls the input node of $INV3$ to GND. As consequence $M4$ is turned on, pulling the output of $INV3$ to V_{dd}, which then turns off $M6$. At the same time, $\overline{En}$ also turns on $M9$ of $INV2$, which leads to turning off $M7$. So, the outcome of this procedure is that each of the output inverters' transistors is switched off separately and *Out* successfully decoupled from the tristate buffer. This is also illustrated in Figure 21 where all related, active transistors are displayed and all turned off transistors are faded out. These measures shall ensure a better, well balanced output impedance regardless of the input signal, which might be applied even when no data shall be transferred to the output. In addition to that, low power consumption and a fast operating frequency are also points of interest, although it is clear that a trade-off between these factors is not avoidable.
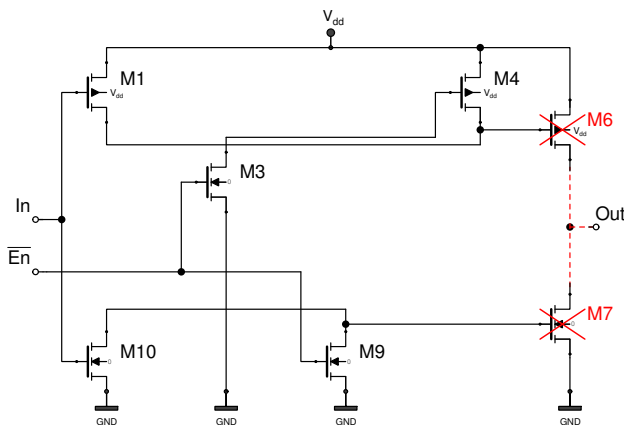
TABLE IX. SIMULATION RESULTS (PWR and (I_{Vdd}))

Design type	Av. PWR (μW)	Max. PWR (μW)	Min. PWR pW
AT tristate	449.1	80.69	26.74

AT tristate buffer shows a poorer performance, at least when talking about a preferably low-power operation mode. The reason for this drawback is the lack of additional power reduction measures, which have been applied to the predecessors. Of course, all of these measures could have been added here as well but the basic intention was to design a completely new tristate buffer, which does not exceed a comparable number of transistors. The transient behavior of the AT tristate buffer is shown in Figure 23 and Figure 24, which depicts the outputs curves with an extended duration of the simulation time. The extracted numbers are shown in Table X and underline the previous statements about the low-power capabilities of this design. A better mitigation of dissipated power and leakage current could be achieved by several add-on measures like power gating, multi-V_{th}, multi-V_{dd} and multi T_{ox}. If desired these modifications can be implemented into the AT buffer by accepting the drawbacks described earlier.

Figure 21. Decoupling of the output inverter in *highZ* mode

In the next step, the alternative tristate buffer was simulated under the same conditions like the previous circuits and the simulation curves are shown in Figure 22.

Figure 22 proves the correct function as the circuit reacts correctly on the applied input data. Similar to the previous investigations, the average, maximum and minimum power dissipation was extracted from the output curves and is summarized in Table IX.

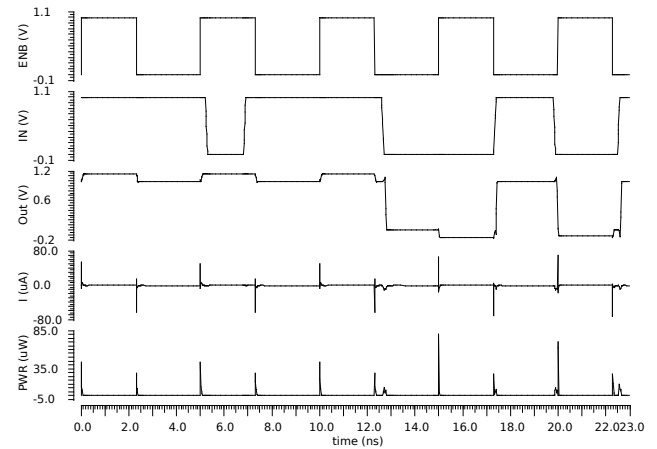In comparison to the results of the modified LP tristate buffer shown in Table V and Table VI, the newly implemented
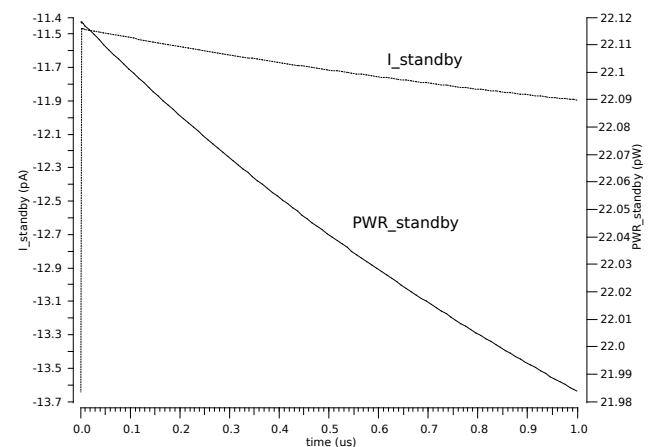

Figure 23. Transient analysis of the AT tristate buffer

After finishing the evaluation of the AT tristate buffer's energy consumption, the focus was put on investigating the
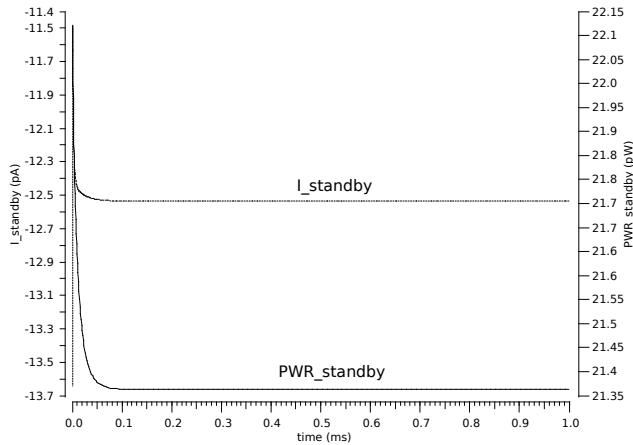
Figure 24. Extended simulation time of power dissipation and leakage current in power-off mode of AT tristate buffer

TABLE X. STANDBY RESULTS COMPARISON

Buffer type	Mod. LP	AT
Av. PWR (*pW*)	1.61	22.04
Av. Current (*pA*)	1.877	11.7

highZ behavior. For this purpose, the circuit was simulated with an active and inactive input in order to check how this might impact the output impedance. The related output curves are shown in Figure 25.
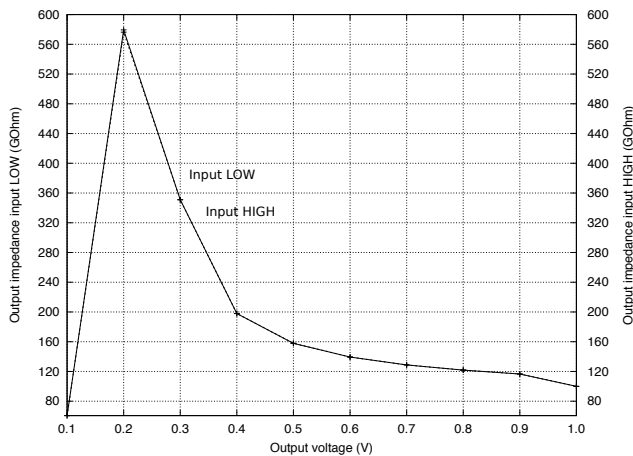

Figure 25. Output impedance in highZ state (AT tristate buffer)

On the first glance, Figure 25 shows that the output curves almost match perfectly on each other. This is a desirable effect as the same output impedance is provided by the circuit regardless of the applied input. Strong, separate driving forces to cut-off each of the output transistors $M6$ and $M7$ are shown in Figure 21. This effect could be even reinforced by using deep cut-off measures when applying a negative V_{GS} voltage at the gates. However, the out-of-the-box result is still considerable.

V. RESULTS COMPARISON

For a better comparison of the investigations, which have been done, all results were summarized in Table XI. The low

power tristate buffer outperforms in almost each aspect the reference design, which highlights its appropriateness for use in applications with limited energy resources. Results of dynamic behavior show that power dissipation is reduced significantly, no matter whether the average, maximum or minimum power consumption is in focus of discussion. The most remarkable reduction is allocated to static behavior of both circuits. Here, the standby leakage current and the dissipated power in idle mode are lowered by over 80%, which emphasizes the effect of implemented low power measures.

TABLE XI. SIMULATION RESULTS I_{Vdd}

Design type	Reference buffer	Low power buffer	$\Delta\%$
Av. PWR (nW)	245	191.3	22 ↓
Max. PWR (uW)	56.75	29.72	47.63 ↓
Min. PWR (pW)	103.8	22.36	78.46 ↓
Av. Current (nA)	215.2	225.8	5 ↑
Max. Current (uA)	230.5	194.8	15.49 ↓
Av. Leak. Current (pA)	133.6	24.1	82 ↓
Av. Standby PWR (pW)	132.1	22.04	83.32 ↓
highZ max.	12.38 $G\Omega$	81 $G\Omega$	↑↑
highZ min.	6.85 $G\Omega$	18 $k\Omega$	↑↑

The appropriate choice of process technology due to the multi-oxide requirements as well as careful layout of transistor parameters requires special attention and allows additional improvements. However, the low power tristate buffer delivers remarkable out of the box performance without further detailed optimization. These adaptions are achieved with a small penalty in terms of transistor count and area. Xilinx provides 372 *Maximum User I/O* and 165 *Maximum Differential I/O Pairs* [7], which could be realized in 537 GPIOs. Implementing a new FPGA design by usage of the low power tristate buffer requires 1074 additional transistors. Here it comes to the point where an efficient layout of the overall chip could be a measures to catch up this drawback. In addition to that, the achieved minimum *highZ* state of the new design of about $14k\Omega$ does not perform as good as the result of the reference tristate buffer ($6.85G\Omega$). This could be improved by a further optimization of the transistor parameters in terms of length and width. However, this might lead to a higher energy consumption and should be carefully decided case by case, depending on which characteristic is of higher importance for the respective application. Despite the additional parasitic capacitances, which come along by adding transistors, nearly all measured insights does not weaken the positive overall print.

VI. CONCLUSION

We analyzed an existing design of a tristate buffer, which was baselined as a reference design serving for further comparisons. During the analysis we did a deep dive into the characteristics of this design for the evaluation of its active and standby performance in terms of dissipated power, average current consumption and the special ability to enter a *highZ* mode. The outcome of these activities was that we wanted to develop a tristate buffer, which is superior in terms of energy savings during runtime and idle state. Due to the lack of a clock signal and, therefore, the impossibility to apply clock gating, we implemented power gating by choosing special high T_{ox} transistors. These transistors have the ability to decouple the tristate buffer from V_{dd} and *GND* as well as the function of gate

tunneling mitigation. For subthreshold current reduction we decided to use high V_{th} transistors, being aware of accepting a penalty in the maximum operating frequency, which was not in the focus of our work though. Simulations have shown that the low power tristate buffer delivers outstanding performance in terms of, e.g., average power consumption in active mode, which is decreased by 22% compared to the reference design. This is a noticeable improvement, since it shrinks the losses of energy in active mode of almost a quarter compared to the reference design. In standby mode, our design outperforms the legacy design by 82% related to average I_{leak}, which is a remarkable result. This low power design features the ability to provide the generation of an internal, smaller supply voltage without any extra *enable* signal from external circuitry. The *highZ* mode abilities of the legacy design are better by a higher order of magnitude, nevertheless, we consider the achieved results of the new tristate buffer as acceptable. These results come at the cost of a higher transistor count and an additional input for an internal, decreased supply voltage I_{Vddlow} as an option. Several possibilities exist for future investigations and improvements. A very simple but effective method for achieving remarkable power savings would be the choice of a technology library with shorter channel lengths, e.g., $28nm$. A technology shrink usually leads to a measurable reduction of consumed power, however, this comes along with some drawbacks like the short-channel effect. Applying negative V_{GS} voltages is an effective way to suppress subthreshold leakage currents after turning a transistor off. Of course, this requires auxiliary logic for generation of negative V_{GS} gate voltages, but this should be a small amount of additional transistors. Further supporting measures can be applied at a higher hierarchical layer, e.g., at architectural level. Controlled dynamic voltage scaling offers the potential to drive the whole. circuit into a deep sleep mode if a standby mode is not crucial for operation of the whole logic. These suggested measures will be starting points for further elaboration of enhanced energy balance with strong focus on a extended battery lifetime in mobile applications.

ACKNOWLEDGMENT

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