Integrated Streak Camera With on Chip Averaging for Signal to Noise Ratio Improvement

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***Abstract*— A technique to reject the noise of the Trans-Impedance Amplifiers (TIAs) of an integrated streak camera in the case of a repeatable input signal is proposed. The modifications of the sensor architecture are marginal with only one additional power supply connected to the column buffer of the sampling cell. The noise rejection can be adjusted independently of the effective bandwidth of the system. The simulation results show that the TIA noise can be reduced from 3.5mV to 0.31mV, which is the limit of the used sampling cells due to the thermal noise on capacitor (kTC). The resulting signal-to-noise ratio is more than 10 times better with an acquisition time of only 20 µs thanks to the on-chip analog averaging feature.**

Keywords—High-speed imaging; CMOS; N-path filter; noise.

I. INTRODUCTION

High-speed imaging using Complementary Metal-Oxide Semiconductor (CMOS) or Charged Coupled Device (CCD) sensors has seen a sharp increase with the apparition of commercial products able to achieve a frame rate of 20 Mega frames per second (Mfps) [1][2]. Thanks to the concept of burst imaging introduced in 1993 by Pr. Etoh Goji [3], this sensor can generate a pixel rate in the range of 1 Tera pixels per second by storing the images within the sensor during the acquisition. Recently, the 3D microelectronic technology allowed to push the state of the art of the 2D high speed burst video sensors with some new functionalities such as an on-the-fly digitalization [4] and an enhanced frame rate of 100 Mfps [5][6]. Nevertheless, in order to reach a higher frame rate, the 2D acquisition paradigm has to be abandoned to the benefit of the streak imaging paradigm. The streak imaging approach is the sampling of just a single spatial line of the scene per unit of time. As a consequence, a spatial dimension is lost and the video is no longer a pile of spatial images *I(x,y)* where *x* and *y* are the spatial dimensions, but a pile of lines which can be represented as a spatiotemporal image *I(x,t)*, where *t* is the time. Indeed, the fastest frame rate achieved with a CMOS sensor has been realized thanks to a streak imaging sensor, such as the one shown in Fig. 1 [7]. By releasing the silicon area constraints of the 2D imagers, one single pixel (the grayed line of Fig. 1) can set in a front end with a large sampling and storage unit beside the photodiode, with almost no spatial limit except the sensor width. Thus, a wideband front end and sampling unit can be embedded, and a line rate of 8 Giga lines per second with a temporal resolution better than 500 ps has been demonstrated [7].

The drawback of such a high bandwidth performance is the noise of the system that increases with the cut-off frequency. Although a high bandwidth is required for single shot measurements, there are some other approaches to measure a repetitive event. Time correlated single photon counting is obviously a very good technique to measure the temporal evolution of a light pulse with a very high signal-to-noise ratio, but the acquisition time can be quite long and these sensors are intrinsically unable to achieve a single shot measurement [8]. In this paper, we propose a technique to reduce the noise of a single shot integrated streak camera with very few modifications of the architecture.

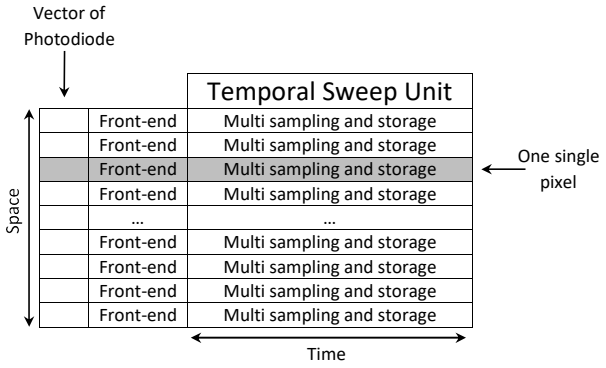

Fig. 1. A streak camera sensor architecture

The overall system architecture and theory of operation are detailed in Section II. The approach functionality and efficiency are then assessed with simulation results depicted in Section III. Section IV concludes on the work.

II. SYSTEM ARCHITECTURE AND OPERATION

A. System architecture

A pixel of the integrated streak camera is composed of a photodiode, a wideband Trans-Impedance amplifier (TIA) and a sampling and storage line, which is a bank of capacitors switched with NMOS (N-type Metal Oxide Semiconductor) transistors, as described in Fig. 2. Each NMOS switch is driven by the S_i signal generated by the temporal sweep unit with $i \in [1;N]$ and N the number of images of the line stored in the sensor. The S_i signals are set on and off sequentially in order to sample the signal applied on the common line by the TIA *A*, which gives an image of the light intensity on the photodiode. After the sampling of the signal, the voltage C_i on each holding capacitor C_{Hi} is then readout by a source follower. Both the photodiode and the readout unit are not presented in Fig. 2 for clarity reason, but they are detailed in [7].

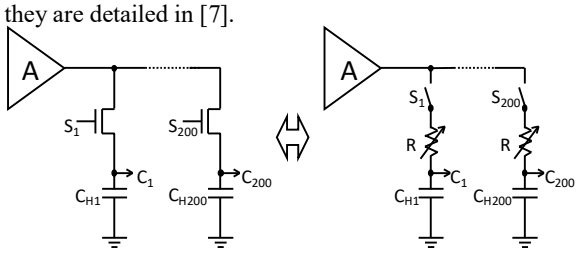

Fig. 2. Simplified architecture of a single pixel and its equivalent model

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The bandwidth of the sampling cell can be well above the bandwidth of the TIA which is about 1 GHz. Thus, each time the NMOS is switched on, we can assume that the voltage on the node C_i follows instantaneously the TIA output. This is the operation in the single shot mode. Nevertheless, the noise at the output of the TIA is also sampled and affects the signal-to-noise ratio.

B. Theory of operation of the on chip averaging

It is well known that averaging a signal reduces the temporal noise and, if the signal can be repeated, multiple acquisitions of a single shot can be readout and averaged on a computer. However, the repetition rate of the event is then limited by the readout time, i.e., about a few Hz. This bottleneck can be circumvented by a high repetition rate on chip averaging. By reducing the voltage of the gate of the NMOS transistor, the "on resistance" R of the transistor can be increased and the behavior of the sampling cell is equivalent to an ideal switch followed by a resistor and the holding capacitance, as depicted in Fig. 2.

If the RC_{Hi} time constant of the sampling cell is higher than the switch on duration T of the S_i signal, the voltage on the node C_i does not have time to follow the output of the TIA. At the same time, the TIA noise is also filtered by the RC_{Hi} filter. When the camera is synchronously triggered by the laser source or vice versa, each time the signal is repeated, the node voltage C_i tends to reach the signal during the switch on duration T. In the meantime, the temporal noise is still filtered and is randomly positive or negative. As a consequence, a high noise rejection can be achieved by reducing the sampling cell bandwidth. The system behaves like an N-Path filter and the transfer function can be written as [9]:

$$\frac{V_{out}(s)}{V_{in}(s)} = \sum_{K=-\infty}^{K=+\infty} \mathrm{sinc}^2\left(\frac{K\pi}{N}\right) \cdot G\left(s - jK\omega_0\right),\ K \in \mathbb{Z} \qquad (1)$$

where $V_{in}(s)$ is the signal at the output of the TIA, $V_{out}(s)$ is the signal reconstructed with the readout of the C_i node voltage and $G(s)=1/(1+RC_H \cdot s)$ is the transfer function of the RC_H filter. Equation (1) is equivalent to a comb Dirac modulated by a sinc due to the gate function of the S_i signal and convolved to the elementary filter $G(s)$.

The complete transfer function from (1) is illustrated in Fig. 3 for sampling cell bandwidths of 100 kHz and 10 kHz for N=200 cells and a sampling rate of 1 GHz, i.e., a period T of 1 ns. As the signal is periodically repeated, it can be decomposed in a Fourier series with fundamental frequency at 1 GHz/200, i.e., 5 MHz and its harmonics. Thus, the complete transfer function for the measured signal is almost equal to 1 for its fundamental and is slightly modulated by the sinc function for its harmonics. Indeed, each sample trends to be the mean voltage of the TIA signal along the gate duration T of the sampling signal which is the reason of the low pass behavior of the sinc function.

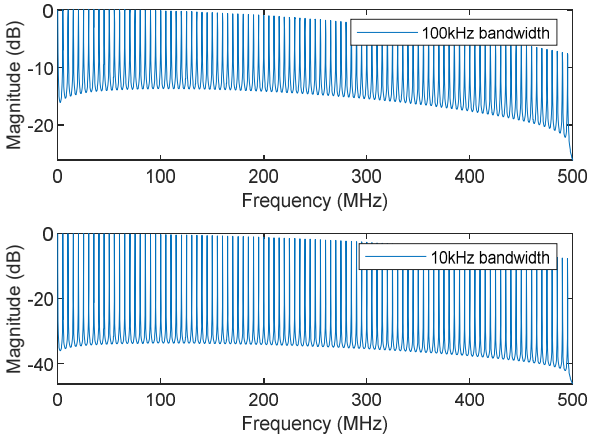

Fig. 3. Complete transfer function of the on-chip averaging system for sampling cell bandwidths of 100 kHz (top) and 10 kHz (bottom)

C. Noise rejection

Fig. 4 is a close-up view of the complete transfer function at the frequency of 5 MHz for sampling cell bandwidths of 100 kHz and 10 kHz. Its magnitude at 5 MHz is actually 0 dB in order for the signal fundamental to fully pass through the filter. The other spectral peaks of the complete transfer function look similar, except for their magnitude modulated by the sinc function.

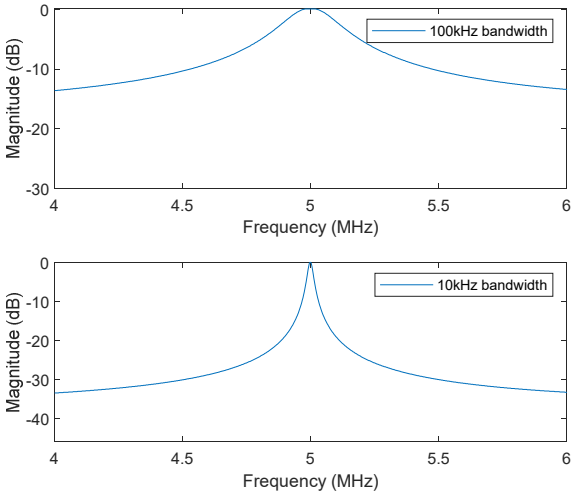

Fig. 4. Close-up view of the fundamental at 5 MHz of the complete transfer function of the one chip averaging system for sampling cell bandwidths of 100 kHz (top) and 10 kHz (bottom)

If we assume that the temporal noise at the output of the TIA is a white noise, this noise is rejected between two spectral peaks thanks to the low pass filter G(s). The narrower are the peaks, the higher is the rejection. Nevertheless, the overlap of the response of two peaks limits the maximal rejection. Indeed, the transfer functions given in Fig. 3 and Fig. 4 indicate a rejection of about 15 and 30 dB for a filter bandwidth of respectively 100 kHz and 10 kHz. With an ideal brickwall filter, the noise rejection should be increased by √n where n is the ratio of the filter bandwidth, i.e., the rejection should be √10 higher with a filter bandwidth of 10 kHz with respect of the one at 100 kHz.

TABLE I. NOISE REJECTION IMPROVEMENT FOR SEVERAL FILTER BANDWIDTH

100 kHz ➔ 10 kHz	10 kHz➔1 kHz	1 kHz➔100 Hz
4.25	3.36	3.1

TABLE I. gives the computed white noise rejection for the transfer function (1) with a first order filter G(s) = 1/(1+RCs) and a bandwidth of 100 kHz, 10 kHz and

1 kHz respectively. The noise rejection is close to √10=3.16 for a decade of bandwidth.

D. Practical limitations

Lowering the filter bandwidth rejects the noise but, as a drawback, a higher number of signal repetition is required. Indeed, a sampling cell is switched on only during the sampling duration T, i.e., the duty cycle is nominally 1/N. As a consequence, the apparent constant time τ_a of the cell is about N times the constant time of the RC_H filter, i.e., $\tau_a=N{\cdot}R{\cdot}C_H$. Moreover, the sampling cell suffers from a leakage current that makes it unable to operate with a too long time constant. In a conventional CMOS technology, the leakage time constant is in the range of 100 ms. Thus, the minimal usable filter bandwidth is in the range of 1 kHz.

The noise rejection is also limited by kTC noise which is the thermal noise of the resistance R integrated on the capacitance and is given by (2).

$$V_{ktc} = \sqrt{\frac{k \cdot T}{C_H}} \qquad (2)$$

III. SIMULATION RESULTS

A. Bandwidth tunning

The bandwidth of cell filter $G(s)$ can be adjusted by adjusting the gate to source voltage V_{GS} of the NMOS transistor in order to obtain an on resistance R that matches $f=1/(2{\cdot}\pi{\cdot}R{\cdot}C_H)$ where f is the required bandwidth and C_H is the value of the holding capacitance. The on resistance follows a strongly nonlinear response according to V_{GS} that allows generating a large dynamic of resistance value R and thus, a large dynamic of bandwidth. The Gate voltage is generated thanks to buffers with an adjustable power supply. Though the source of the transistor is following the TIA output and consequently, the V_{GS} is signal dependent. Fig. 5 gives the small signal bandwidth of the sampling cell filter versus the buffer power supply voltage for different TIA output voltages for the designed sampling cell. More than 3 decades can easily be covered thanks to this technique which does not require any additional transistors within the sampling cell. The only modification relies on the tuning of the supply voltage of the buffer that drives the S_i voltage. These buffers are common for a whole column of the sensor and each column buffer is powered by the same power supply. As a consequence, the only modification of the system architecture is to add a specific power supply for these buffers.

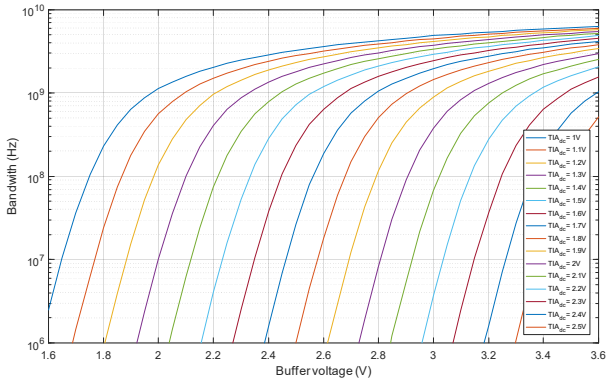

Fig. 5. Small signal bandwidth of the sampling cell filter versus the buffer power supply voltage for different TIA output voltage

B. Sinusoidal signal acquisition

The noise rejection has been evaluated with a SPICE simulation for two sinusoidal signals of 5 and 50 MHz at the input of the TIA. The total added rms noise at the output of the TIA integrate from 10 Hz to 10 GHz is 3.5mV rms. The results are shown in Fig. 6 for several filter bandwidth of 1 GHz down to 1 MHz. The displayed curves are the concatenation of the voltage C_i from the sampling cells i=1 to 200 after 100 accumulations of the same signal. The simulated time is then 200 cells×1 ns×550 accumulations = 110 µs.

With a filter bandwidth of 1 GHz (pink curve of Fig. 6), the sampled signal with 100 accumulations is almost the image of the last one. Indeed, during the 1 ns long aperture of the switches, the voltage at the nodes C_i has enough time to reach the TIA output. In this case, the results are very close to a classical sampling and we can see that the noise added by the TIA is present on the sampled signal.

With a filter bandwidth of respectively 100 MHz (green), 10 MHz (blue) and 1 MHz (red), the noise is less and less present on the sinusoids. We can also see that the shape and amplitude of the sinusoids are not affected by the filter bandwidth reduction and that the 50 MHz signal can be measured even with a filter bandwidth of only 1 MHz. This simulation demonstrates that the white noise can be efficiently rejected without altering the periodic signal.

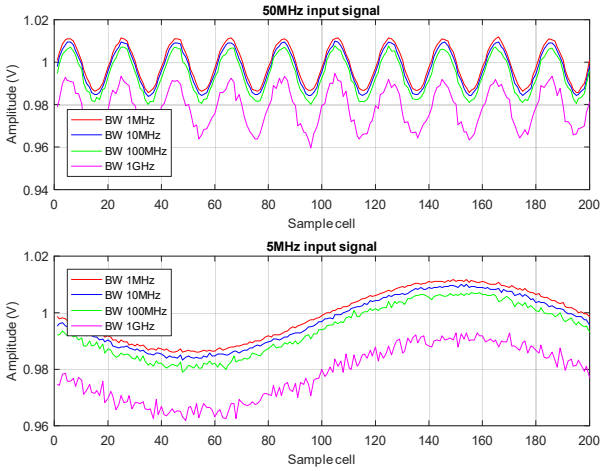

Fig. 6. Simulation of the noise rejection on a sinusoidal input signal of 50 MHz (top) and 5 MHz (bottom) for a filter bandwidth of 1 GHz down to 1 MHz. A cell is equivalent to 1 ns

C. Noise rejection assessment

In order to characterize the noise rejection, the same simulation as the previous one was made without any signal at the input. The observed signal should be the operating point of the TIA output, i.e., a static voltage of about 1 V. The result is shown in Fig. 7.

Once again, we can clearly see that the noise is rejected and that the reconstructed signal becomes less noisy. The equivalent power spectral densities of the measured noises are plotted in Fig. 7. We can see that the rejection is applied on the whole spectrum of the white noise and especially also for the low frequencies. The statistical distributions of theses samples are also depicted in Fig. 8. The assessed noise with a bandwidth of 1 GHz is 1.75 mV rms and is reduced down to 0.769 mV rms for a bandwidth of 100 MHz, i.e., a

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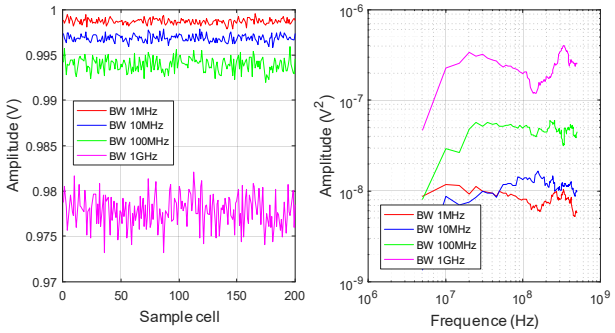

Fig. 7. Simulation of the TIA white noise rejection for different filter bandwidth. Acquired Samples (left) and equivalent power spectral density (right)

rejection of 2.3. For a bandwidth of 10 Mhz, the noise is reduced again down to 0.383 mV rms, i.e., the rejection from 100 to 10 MHz is about 2. Finally, the rejection over the decade from 10 to 1 MHz is only 1.2 with a noise at 1 MHz of 0.31 mVrms. This last simulated rejection ratio is less than expected because it is limited by the kTC noise of the sampling cell which integrates a holding capacitance of 40 fF, i.e., $V_{kTC} = 0.32$ mV. The proposed noise rejection technique makes the TIA noise negligible with respect to the kTC noise level.

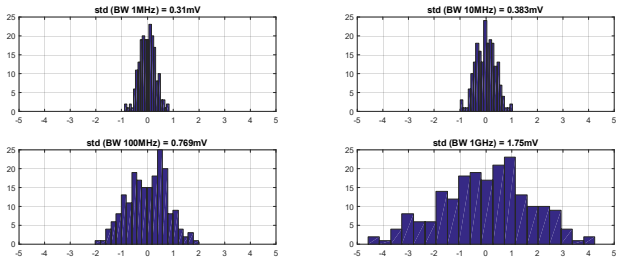

Fig. 8. Noise distribution (mV) of the simulated sample for noise rejection assessment for different filter cell bandwidths

IV. Conclusion

A technique to reject the noise of the TIAs of an integrated streak camera in the case of a repeatable input signal is proposed. The modifications of the sensor architecture are marginal with only one additional power supply connected to the column buffer of the sampling cell. The noise rejection can be adjusted independently of the effective bandwidth of the system. The simulation results show that the TIA noise can be reduced from 3.5mV to 0.31mV which is the limit of the used sampling cells due to the kTC noise. The resulting signal-to-noise ratio is more than 10 times better with an acquisition time of only 20 µs thanks to the on-chip analog averaging features.

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