Simulation Model of the Integrated Hall Element Implemented in Verilog-A

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***Abstract*—The paper describes the development of the improved simulation model based on a six terminal Hall element implemented in the hardware description language Verilog-A. The new simulation model considers temperature effects, offset voltage, influence of mechanical stress, external magnetic field and internal magnetic field generated by the internal microcoil. To obtain the best accuracy of the Verilog-A based model, all key parameters of the simulation model were determined and characterized by measuring the manufactured Hall plate bonded into a ceramic package. The verification of the improved simulation model was performed in the Cadence Spectre simulator. The Hall element simulation model was designed in the 0.18µm technology but can be easily adapted to any technology to a certain extent by adjusting its parameters according to the measurement results.**

Keywords-Hall element; simulation model; Verilog-A.

I. INTRODUCTION

Hall sensors are still widely used in the magnetic sensors market, although the emerging magnetoresistive sensors, such as Anisotropic Magneto-Resistance (AMR), Giant Magneto-Resistance (GMR) and Tunnel Magneto-Resistance (TMR) are showing impressive performance results. Recently, a comprehensive sensor market study has been taken. It concludes, that Hall-effect sensors will still lead the future of the sensor market exceeding $1.2 billion in 2030, although the Hall effect in semiconductor has been extensively studied in the past few decades [1]. The Complementary Metal Oxide Semiconductor (CMOS) Hall sensors are used to measure relative or absolute position, electric current, energy, speed, angle, Earth's magnetic field, etc. The main reasons why CMOS Hall effect sensors lead the field of magnetic sensors are their linearity over a wide dynamic range, their low process costs compared to their competitors due to their compatibility with standard CMOS technology and their robustness. There are also many disadvantages of the Hall element compared to its magnetoresistive competitors, which need to be solved by researches. The low sensitivity, high power consumption and low signal to noise ratio are just a few of them. The next is the relatively large offset voltage, which is a function of geometry and production errors. However, the high offset voltage and 1/f noise can be greatly reduced by applying the well-known current spinning technique [2], which is commonly used in the art of designing a magnetic microsystem with the Hall elements. The second is the temperature variation of the sensitivity of the Hall element. The variation of sensitivity is non-linear and depends on the mechanical stress. One way to overcome the problem is to use an integrated microcoil that generates an internal reference magnetic field to calibrate the sensitivity of the magnetic microsystem [3].

The magnetic system with an array of N Hall sensors is used to measure the spatial distribution of the magnetic field or to increase the low sensitivity of the Hall element by the factor N, to increase the signal to noise ratio and to minimize the offset by a factor $\sqrt{N}$ [4]. The second is the use of ferromagnetic structures, also known as magnetic concentrators, where they are used as planer magnetic amplifiers [5]. Basically, the magnetic concentrator converts the parallel magnetic field into a magnetic field that is orthogonal to the surface of the Hall element. The mentioned disadvantage of the solution is an additional step in the production of the System on Chip (SoC).

To reduce the power consumption of the magnetic microsystem, the bias current of the Hall element can be pulsed during signal processing. In order to simulate and design the high performance magnetic microsystem, an accurate simulation model of the Hall element must be used. Such a simulation model should take into account the offset voltage, the external magnetic field, the internal magnetic field, the mechanical stress and the temperature variations of the sensitivity [6]. Sometimes integrated circuit manufacturers do not provide all the necessary technological parameters required for a successful implementation of the Hall element model in e.g. multiphysics software such as COMSOL. In a case, where the technological parameters are treated as confidential, the Hall element model can be created using the measured results and know-how.

The rest of the paper is structured as follows. In Section 2, the theory and the measured results of the Hall element designed and manufactured in the 0.18µm Bipolar CMOS Double Diffused Metal Oxide Semiconductor (DMOS) (BCD) technology are collected. In Section 3, the development and verification of the Verilog-A model are presented. Finally we summarize the paper in Section 4.

II. THEORY AND MEASURED RESULTS

The Hall effect in semiconductor can be briefly described as a deflection of charge carriers caused by the Lorentz force when the magnetic field is present. If the magnetic field is perpendicular to the semiconductor surface and the Hall element is connected to the power supply, i.e., the current flows through the semiconductor then, the small Hall voltage appears at the edges of the Hall plate [7]. The Hall element

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can be biased with current or voltage. This means that the Hall voltage can be described as a function of the selected bias [8]. If the Hall element is voltage biased, the Hall voltage is given by (1),

$$V_H = G\frac{W}{L}\mu_H V B_z, \quad (1)$$

where the correction factor G depends on the shape of the Hall element, W and L are the width and length of the sensor, respectively, μ_H is the Hall mobility, V is the supply voltage and B_z is the applied magnetic field orthogonal to the surface of the Hall element. Secondly, the Hall element can be biased using the current source. In this case, the Hall voltage is expressed as (2):

$$V_H = G\frac{r_H}{qnt} I B_z, \quad (2)$$

where r_H is the Hall factor, q the electron charge, n the doping concentration in n-doped silicon, t the thickness of the active N-well region and I the bias current flowing through the Hall element [8].

The Verilog-A model is based on the six terminal Hall element model presented in [9] and serves as the starting point for a new Hall element model. The simplified electrical Hall element model and its cross-shaped layout model with four contacts *U – Up*, *D – Down*, *L – Left* and *R – Right* are shown in Figure 1. The electrical model consists of four N-well resistors representing the N-well Hall element resistance. The cross-shaped Hall element is widely used due to its 90° symmetry, which reduces potential mask misalignment errors. It is also useful when current spinning technique, i.e., electrical rotation of its terminals, is used to minimize the offset voltage. The complete cross-shaped Hall element with integrated microcoil is shown in Figure 2. The active area width of the Hall element is 13 µm. It is worth mentioning that the minimization of the Hall element is crucial, e.g. to increase the spatial magnetic field resolution and the bandwidth of the magnetic microsystem. One of the disadvantages of miniaturization is a larger offset and errors e.g. due to etching. In addition, the efficiency of the microcoil is increased because it is closer to the active area of the Hall

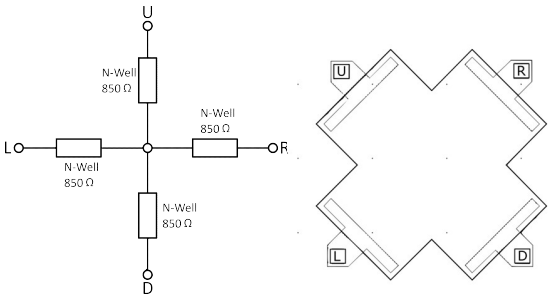

Figure 1. The simplified electrical model of the Hall element (left) and its cross-shaped layout model (right).

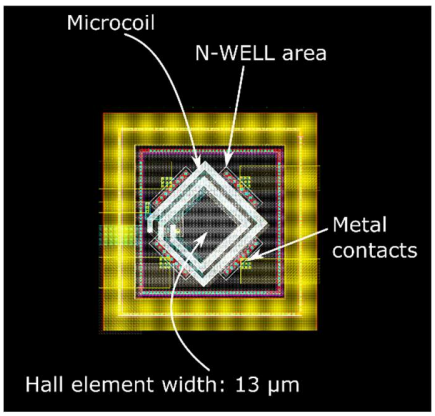

Figure 2. The complete cross-shaped Hall element with microcoil.

element. The number of microcoil turns is another parameter that is important when designing the internal reference magnetic field. The N-well area, microcoil and metal contacts are shown in Figure 2 as well. The complex electrical circuit schematic of the six terminal Hall element model is shown in Figure 3 [9]. The Hall element has four basic contacts *U*, *D*, *L*, *R* and an auxiliary contact *B* for the simulation of the external magnetic field. In addition, there are two more contacts *CI*, *CO* each representing the input and output of the internal microcoil. The resistance of the Hall element is represented by four N-well resistors connected in the resistor bridge. Four resistors are added between *U* and *ua*, *D* and *da*, *L* and *la* and *R* and *ra* as current sensing element. The value of each resistor is 1 **Ω**. This means that the voltage drop across the resistors directly represents the bias current of the Hall element. At each branch, 8 Voltage Controlled Resistors (VCR) and 8 Current Controlled Current Sources (CCCS) form a current loop. Four pairs (red current loops) are active when the external magnetic field is present and the other four pairs (green current loops) are active when the internal magnetic field is generated. VCRs only work for positive values (positive resistance), so two current loops are added to each branch. The value of the four VCRs when the external field is applied is determined by the voltage drop across the sensing resistors caused by the bias current of the Hall element. The others value is 0. The current in each loop depends on the CCCS controlled by the current flow (*vm*) through the resistor connected between contacts *B* and *gnd*. The mentioned current depends on the voltage signal at terminal *B*, which represents the external magnetic field. Similarly, when the internal magnetic field is applied, the current in the other four loops depends on the current flowing (*vs*) through the 50 **Ω** resistor, which represents the resistance of the microcoil. The electrical model contains 8 Voltage Controlled Voltage Sources (VCVS) representing the offset voltage of the Hall element. The controlled voltage depends on the voltage drop across the current sensing resistors caused by bias current of the Hall element. The four current sensing resistors are used to maintain the symmetry of the resistor

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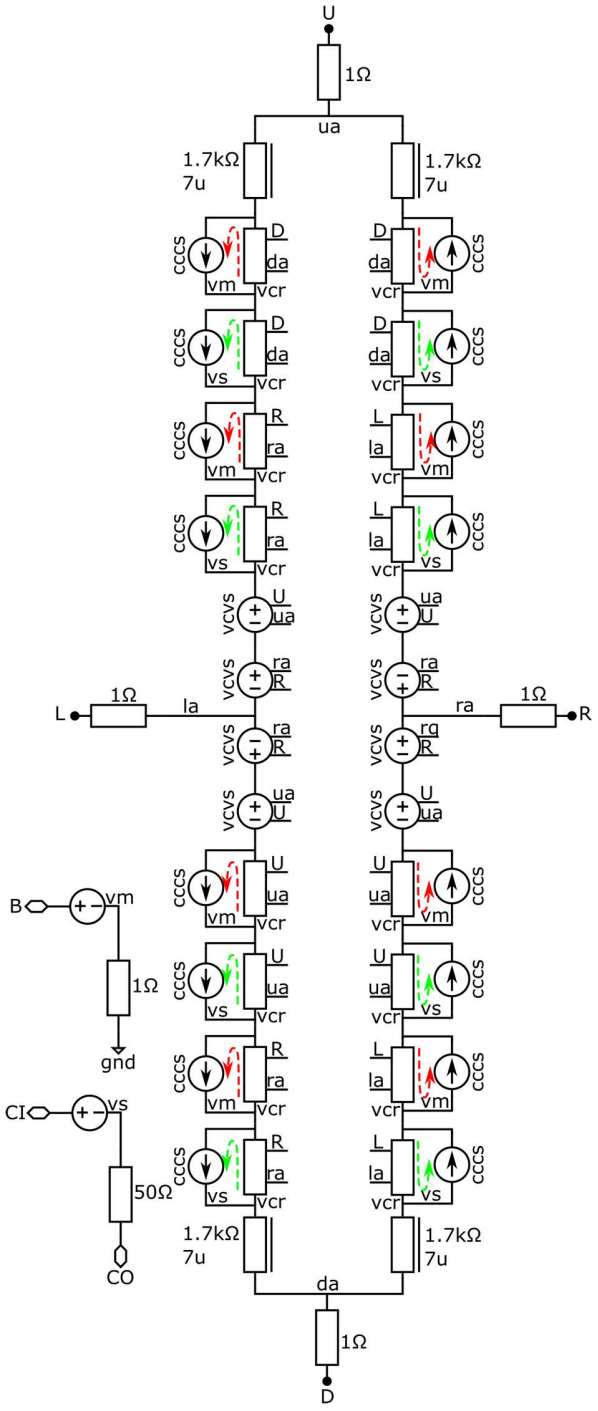

Figure 3. The complex electrical schematic of the six terminal Hall element model in 0.18 µm BCD technology.

bridge. From a functional point of view, only two of them could be used. The microphotography of the Hall element manufactured in the 0.18 µm BCD technology is shown in Figure 4. The Hall element was bonded with 30 µm bond wires into a ceramic package. The Hall element was exposed

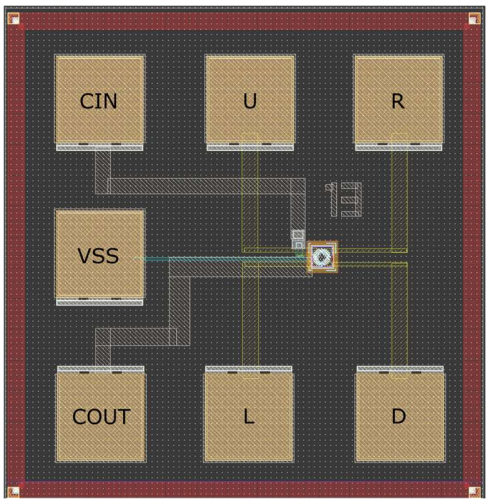

Figure 4. The microphotography of the Hall element with corresponding contacts.

to an external magnetic field of 34 mT or 340 G between two circular magnetic coils - Helmholtz pair, which generated an almost uniform magnetic field. Thermal tests were carried out in the temperature chamber from -40 °C to 120 °C. First, the offset voltage was measured at different temperatures and in different bias modes without applied magnetic field. The average measurement results of the offset voltage based on N=20 samples are gathered in Table 1. When the Hall element is voltage biased, the bias current *Ib* decreases with temperature due to the positive temperature coefficient of the N-well. This means that the N-well resistance increases with increasing temperature and consequently influences the offset voltage *Voff*. When the Hall element is current biased, the changes in offset voltage are greater due to the applied constant current. The results show that the Hall element suffers from a large offset voltage (mV) therefore current spinning technique should be used to reduce it to (µV). The

TABLE I. OFFSET VOLTAGE MEASUREMENT RESULTS

	Voltage Biased		**Current Biased**	
T (°C)	***Voff (mV)***	***Ib (mA)***	***Voff (mV)***	***Ib (mA)***
-40	-0.324	2.000	-0.324	2
-20	-0.445	1.918	-0.465	2
0	-0.529	1.828	-0.588	2
20	-0.656	1.733	-0.768	2
40	-0.793	1.636	-1.005	2
60	-0.926	1.542	-1.247	2
80	-1.050	1.445	-1.531	2
100	-1.168	1.360	-1.838	2
120	-1.272	1.280	-2.167	2

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offset voltage changes locally from die to die or globally from wafer to wafer, so it is a random function. In this case, the offset voltage could be expressed as a third order polynomial:

$$V_o(x) = 2 \cdot 10^{-8}x^3 - 2 \cdot 10^{-5}x^2 - 0.0042x - 0.297, \quad (3)$$

where x represents a temperature. The polynomial is found as a line that best fits the measured data. Equation (3) is used later in Verilog-A description of the Hall element.

Then, the sensitivity of the Hall element to the external and internal magnetic field was measured. The results are shown in Table 2. The measurement was performed for both bias modes. Figure 5 and Figure 6 show the average measurement results of the current related sensitivity *SI* and voltage related sensitivity *SV* respectively for N=20 samples. The temperature coefficient of the Hall element sensitivity depends on the carrier mobility, the Hall element factor and the mechanical stress. To describe the absolute value of the current-related sensitivity variation with temperature, the relative error δ_{SI} can be added as:

$$\delta_{SI}(x) = 8.83 \cdot 10^{-6}x^2 - 1.50 \cdot 10^{-3}x - 0.0035, \quad (4)$$

where x stands for the temperature. In this case, the relative error 0 at 0 °C is selected. Again, equation (4) is found as a line that best fits the measured data, so the relative error deviates slightly from 0 at 0 °C.

The sensitivity of the Hall element to the internal magnetic field generated by the integrated microcoil is 26 V/AA or 26 µV at 1 mA of the bias current of the Hall element and 1 mA of the current flowing through the microcoil. The integrated coil generates a magnetic field of 0.52 mT or 5.2 G at 1mA DC current. The resistance of the microcoil also changes with temperature, so the temperature coefficient of the microcoil should not be neglected. Its measured value is $3 \cdot 10^{-3}$ /°C.

With the measurement results obtained, the Verilog-A based Hall element model can be developed.

TABLE II. THE MEASURED RESULTS OF THE HALL ELEMENT SENSITIVITY

T(°C)	SV (V/VT)	SI (V/AT)
-40	0.034	54.2
-20	0.032	51.9
0	0.029	50.1
20	0.027	48.8
40	0.025	48.0
60	0.023	47.5
80	0.022	47.4
100	0.020	47.2
120	0.019	47.4

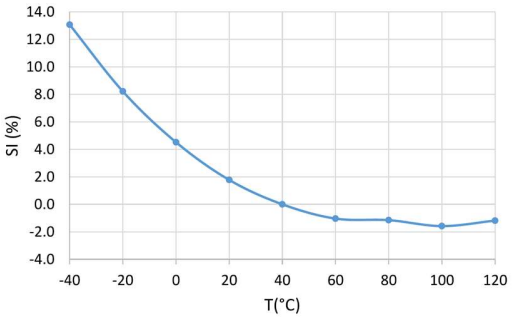

Figure 5. Current related sensitivity of the Hall element.

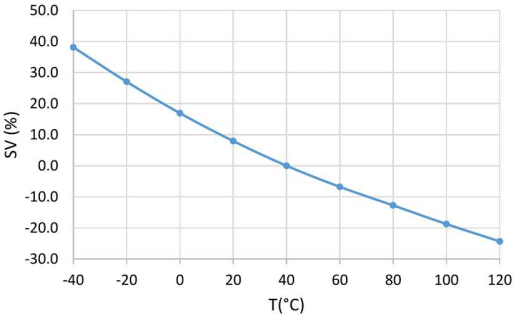

Figure 6. Voltage related sensitivity of the Hall element.

III. DEVELOPMENT OF THE VERILOG–A BASED HALL ELEMENT MODEL

In this Section only a crucial part of the Verilog-A code will be analysed as, the rest is a top level description of the Hall element shown in Figure 3. The first part of the code is shown in Figure 7 and describes the VCR. The value of the resistor is represented by the voltage drop between *p2* and *n2*.

```
// VerilogA, VCR
‘include "constants.vams"
‘include "disciplines.vams"
            module vcr (p2, n2, p1, n1);
            inout p2, n2, p1, n1;
            electrical p2, n2, p1, n1;
            real vctrl;
analog begin
            vctrl=V(p2,n2);
            if (vctrl<1e-05) begin
                        vctrl=1e-05;
                        I(p1,n1)<+V(p1,n1)/vctrl; end
            else
                        I(p1,n1)<+V(p1,n1)/vctrl; end
endmodule
```

Figure 7. VCR description in Verilog-A.

The current through *p1* and *n1* is proportional to the voltage difference between terminals *p1* and *n1* divided by *vctrl*. To avoid division by zero error or negative resistance, the *vctrl* is limited to $1 \cdot 10^{-5}$. This is achieved by using a conditional statement.

The second part of the code is shown in Figure 8 and represents CCCS. The *I(out)* depends on the voltage drop

```
// VerilogA, CCCS
`include "constants.vams"
`include "disciplines.vams"
            module cccs (pi, ni, p, n);
            inout p, n, pi, ni;
            electrical pi, ni, p, n;
            parameter real gain=1;
            parameter real rm=1;
            branch (p, n) out;
            branch (pi, ni) in;
            parameter real pt=($temperature-273.15);
            parameter real ksen3=0;
            parameter real ksen2=0;
            parameter real ksen1=0;
            parameter real nsen=0;
            parameter real sen=0;
            real ksen=0;
analog begin
            if (sen==1) begin
ksen=(ksen3*(pt)*(pt)*(pt)+ksen2*(pt)*(pt)+ksen1*(pt) + nsen);end
            else if (sen!=1) begin ksen=0; end
            I(out)<+((1+ksen)*(gain*V(in)))/rm; end
endmodule
```

Figure 8. CCCS description in Verilog-A.

V(in) across the current sensing resistor, which represents the current that controls CCCS. The value of the current depends on the ports used (*branch (pi, ni) in*). First, when the input port *B* is selected, the current depends on the input voltage applied to port *B*, which represents external magnetic field. Second, when input terminal *CI* is selected the current depends on the input voltage applied to terminal *CI*, which represents internal magnetic field. The variable *pt* represents temperature. The absolute value of sensitivity to the external or internal magnetic field can be adjusted by the *gain* parameter. The polynomial *ksen* with the corresponding coefficients *ksen3*, *ksen2*, *ksen1* and *nsen* representing the relative error δ_{SI} is used when the parameter *sen* is equal to 1. If *sen* is 0 then, the relative error or *ksen* is zero.

The third part of the code is shown in Figure 9 and describes the VCVS, which adds the offset in the model of the Hall element. The controlled voltage *vctrl=V(p2,n2)/2* depends on the voltage drop across the current sensing resistor, which represents the bias current of the Hall element. The polynomial *koff* with the corresponding coefficients *koff3*, *koff2*, *koff1* and *noff* is added to simulate the offset voltage. The offset voltage can be switched on or off by setting the *off* parameter to one or zero.

```
// VerilogA, VCVS
module vcvs (p2, n2, p1, n1);
inout p2, n2, p1, n1;
electrical p2, n2, p1, n1;
parameter real pt=($temperature-273.15);
parameter real koff3=0;
parameter real koff2=0;
parameter real koff1=0;
parameter real noff=0;
parameter real off=0;
real vctrl;
real koff;
analog begin
vctrl=V(p2,n2)/2;
if (off==1) begin
koff=(noff+koff3*(pt)*(pt)*(pt)+koff2*(pt)*(pt)+koff1*(pt)); end
else if (off!=1) begin koff=0; end
V(p1,n1)<+vctrl*abs(koff);
end
endmodule
```

Figure 9. VCVS description in Verilog-A.

Figure 10 shows the Hall element and its parameters which can be set according to the measurement results. The absolute value of the sensitivity can be adjusted by changing the parameters *emf* (external magnetic field) and *imf* (internal magnetic field). The resistance of the N-well resistor can be changed by the parameters *nw* (width) and *nl* (length). The temperature coefficient of the microcoil can be adjusted by changing the parameter *tc_coil*.

The next step in the development is the verification of the Hall element written in Verilog-A. Figure 11 and Figure 12

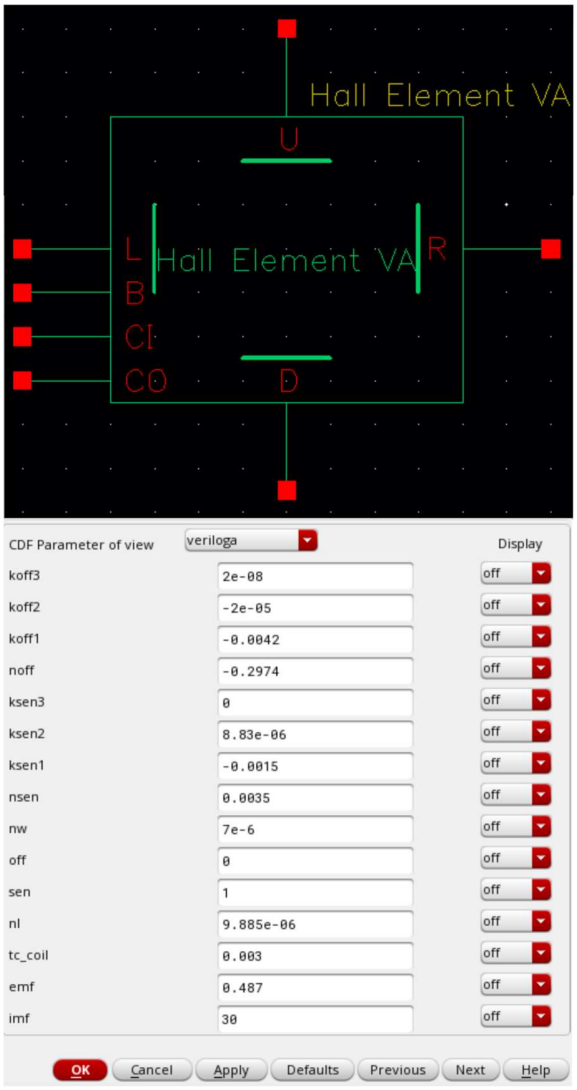

Figure 10. The symbol of the Hall element and its parameters in Cadence Virtuoso®.

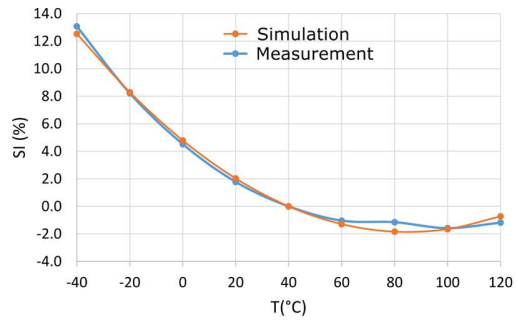

Figure 11. Current related sensitivity of the Hall element.

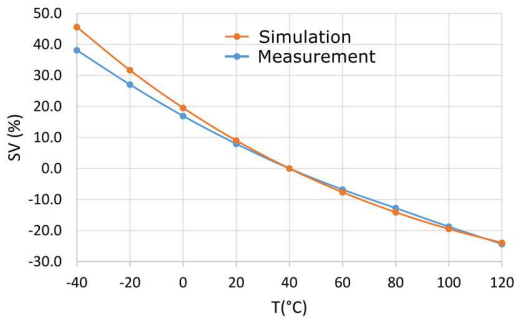

Figure 12. Voltage related sensitivity of the Hall element.

show the comparison between measurement and simulation results. The proposed model shows a good agreement with the measurement results of N=20 Hall element samples bonded into the ceramic packages.

IV. CONCLUSIONS

A development of the Hall element model written in Verilog-A was presented. Some solutions for characterizing the Hall element in case, the technological data are not fully available are described in the paper. The proposed Hall element model takes into account the internal magnetic field, the external magnetic field, and offset voltage, the temperature dependence of the sensitivity of the Hall element and its offset voltage, and the packaging stress. The simulation results show a good agreement with the measurement results.

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