Wide Dynamic Range Readout for CMOS Pixel Using PWM and Direct Mode Sensing Techniques

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Abstract— Dynamic range is a critical figure of merit for image sensors. Then, many researchers have been working to improve this figure. As a result, various techniques have been developed with good results. However, any effort to improve even more the dynamic range is of great value. The multimode method combines more than one technique to use the best part of them. In this paper, a high dynamic range CMOS image sensor using multimode sensing is presented. Dynamic Range as high, as 160 dB is achieved combining PWM and direct mode techniques. The circuit proposed here has one of the higher dynamic ranges reported.

Keywords-wide dynamic range; CMOS imagers; PWM sensors; continuously operation sensors; multimode sensing.

I. INTRODUCTION

Currently, CMOS (Complementary Metal Oxide Semiconductor) technology allows the integration of complex electronic systems that include devices of various types. For example, optical sensors allow the formation of CMOS imagers that offer several advantages compared to CCD's (Charge-Coupled Device) [1], such as power consumption, low voltage, low cost, etc., which have enabled the creation of imagers that represent single-chip solutions [1].

In a CMOS imager, one of the most important figures of merit is the Dynamic Range (DR) [1] given by (1). The DR permits to differentiate between high and low excitation conditions in general, and, in the case of an imager, to distinguish between lightly and highly illuminated areas.

Then, it is clear that systems with higher DR would resolve extreme conditions without loss of information. As a consequence, nowadays, the increase of DR is an active area of research.

$$DR = 20\log \frac{V_{max}}{V_{min}} \,[\text{dB}] \tag{1}$$

Many efforts to obtain vision systems with a wide DR have been done. Different techniques to increase the DR have been reported; some of them are reviewed in [2-3], and enlisted here: logarithmic method, capacity well adjustment

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method, multimode sensors, frequency-based sensors, timeto-saturation sensors, multiple sampling methods, and multiple integration time methods.

As mentioned above, one technique to increase the DR is the multimode sensing system. To enhance the DR, multiple sensing techniques can be used, by taking advantage of the best resolution of each one.

Two types of readout that are used in CMOS imager, i.e., 1) integration-based sensors and 2) direct mode operated sensors, can be combined to improve the system response.

In the first case (i.e., integration-based sensor), photogenerated charges are integrated given a linear response. The current in the order of femtoAmperes can be detected by this method [4], corresponding to very small illumination intensities.

In the direct mode operated sensor technique, the current generated by a Photodiode (PD) is directly converted to voltage. In this case, the current detected is in the order of microA or miliA, corresponding to very high illumination intensities.

Then, a combination of both readout techniques allows detecting the current of a PD from femtoA to miliA.

In this paper, a combination of current integration and direct mode detection methods are used to increase the DR.

This paper is organized as follows: Section II presents the definition and basic assumptions of the multimode technique proposed. Section III presents the results obtained of the proposed circuit. Section IV summarizes the study.

II. PWM - DIRECT MODE TECHNIQUE PROPOSED

A block diagram of the multimode method used is shown in Fig. 1. As it can be seen, the photocurrent from the sensor could be integrated in the upper branch, or could be amplified directly in the lower branch.

In the integration mode, the photocurrent, I_{ph} , obtained in the step 1 is integrated and converted to a voltage ramp, steps 2. In step 3, when the voltage ramp reaches the comparator reference voltage a shot pulse is obtained. In the direct mode, step 4, the I_{ph} is directly fed to an amplifier. Both readout signals are passed into an analog-to-digital converter, and finally, in step, 5 a Digital Word (DW) is obtained proportional to the incident light in the sensor.



Figure 1. Multimode sensing block diagram.

A. Pulse Width Modulation Mode Readout

In integration mode (or lineal mode), the parasitic capacitor of a PD is charged to a reference potential and when light shines on it; this potential decreases almost in a linear fashion, due to the photocurrent discharging the capacitor.

By measuring the voltage drop, the amount of light can be obtained, using (2), where I_{ph} is the photocurrent, T_{int} is integration time, and C_{PD} is the parasitic capacitor of the PD.

$$\Delta V = \frac{I_{ph} T_{int}}{C_{PD}} \tag{2}$$

In Pulse Width Modulation (PWM) [5] mode, each pixel controls the integration time T_{int} , and can integrate very small signals until an adequate output is obtained.

The circuit shown in Fig. 2 is an example of how to implement the PWM mode. The current is integrated and then compared with the reference voltage.



Figure 2. Circuit used to implement the PWM technique. The upper graph shows the Vpd voltage linear decay due to the incident light. The lower graph shows Vout as a function of time.

The PMOS (P-type Metal Oxide Semiconductor) transistor works as a reset switch; on the ON state the PD voltage (V_{pd}) is near V_{dd} . Then, the switch is turned OFF and the incident light produces V_{pd} to decrease linearly.

When V_{pd} reaches the reference voltage, the comparator generates an output voltage pulse. By measuring the width of this pulse, the amount of light shining on the PD can be measured.

The problem with this technique is that pixels working in integration mode have a limited DR at higher levels of photocurrent; this is, the integration time will be too short, and in some cases imperceptible. Then, this technique increases the DR at small light power levels but fails to work adequately with high power levels, as shown in Fig. 3. In other words, low illumination level produces small photocurrent, as the light intensity augment the photocurrent increases reducing the integration time. If the light is intense the integration time will be very difficult to measure.

To solve the high current problem, bright light will be detected by direct current amplification.

B. Direct Mode Readout

In direct output mode, the PD current is directly transferred to current mirrors with or without amplification. This architecture suffers from low sensitivity at low level of illumination; however, works fine detecting high illumination levels.

Flipped-Voltage Follower (FVF) in current mode [6] is used to sense the PD current due to its low input impedance and because it can drive large input current variations, as shown in Fig. 4. The FVF is shown in Fig. 4a; in this circuit, the input impedance Z_{in} is very low and given by

$$Z_{in} = \frac{1}{g_{m1}g_{m2}r_{o1}}$$
(3)

where g_{m1} and g_{m2} are the transistor transconductances and r_{01} is the transistor's output resistance of M1.



Figure 3. Photocurrent vs integration time, as the current increases the time tends toward zero.



Figure 4. a) Flipped-Voltage Follower in current mode and b) current mirror.

The input impedance is low due to the shunt feedback provided by M2. The output current is given by the expression $I_{out} = I_{ph} - I_{bias}$, where I_{bias} is the bias current provided by the source current in M1, and I_{ph} is the current from PD.

Normally, the current needs to be amplified; so, a current mirror is used and the gain is given by the ratio W/L of the transistors.

To make the mirrored current as accurate as possible is necessary to use an operational amplifier, as shown in Fig. 4b, that keeps the bias voltage equal in both branches.

Fig. 5 compares the fidelity of the current copy with and without operational amplifier topologies. As shown, the advantage of using the operational amplifier is clear.

C. PWM-Direct Mode Circuit Implementation

A schematic diagram of the proposed circuit is shown in Fig. 6, which combine both readout topologies: PWM and direct mode. When low illumination is shining on the PD, the PWM mode works, and when bright illumination is received, the direct mode topology comes into operation.

Internal switches, which are controlled by the PWM output, select one or the other topology.



Figure 5. Input and output current comparison in the current mirror with and without operational amplifier.



Figure 6. Dual mode circuit, when S1 and S2 are closed the direct mode is activated. On the other hand, when S1 is open and S2 is at the REF voltage the PWM mode is activated.

The PWM output voltage for a single sensor signal is shown in Fig. 7a; when the voltage ramp reaches the voltage reference a step is produced and the voltage gets a constant value. This voltage is then used to switch to the direct mode, and the output current increases to a new value proportional to the current in the sensor, as shown in Fig. 7b.

As displayed in Figs. 2 and 4, an operational amplifier is needed in both topologies. So, sharing the operational amplifier in each pixel to run both techniques reduces the number of transistors and improves the circuit performance.

III. SIMULATION RESULTS

Fig. 8 shows the result of simulations when dull incident light shines on the sensor. As it is shown, the integration time starts when the reset command is triggered and V_{pd} is at V_{dd} (3.3V); then, different V_{pd} voltage ramps are produced by different light intensities. After some time, each ramp reaches the reference (in this case 1.5V). At that moment, the comparator output produces a voltage step.



Figure 7. Output voltage and current of the PWM and direct mode sections, in a) the ramp of voltage is shown and after it reaches the reference a constant voltage step is produced. In b) as the PWM mode is active the I_{out} is low, and when the direct mode is activated the Iout increases proportional to the sensor's current.

This voltage step triggers the switches S1 and S2 to start the direct mode, and also it is used to bias the transistor, M4, allowing that the I_{out} increases to a value given by $(I_{ph}-I_{bias})$.

Fig. 8b shows the PWM output current, as can be seen the current is zero until the voltage reference is reached, then a high current is obtained. The elapsed period can be used to estimate the light intensity. In this case, the input current used was from 20 up to 200 picoA (labels A and B correspond to the lower and the higher intensities respectively).

For example, in this simulation, the first ramp, that corresponds to the intensity B, lasts 0.1ms, as shown in Fig. 8b; the last ramp lasts 0.47 ms (intensity A). Let us suppose that it is the real response of the circuit under illumination, and the light shining on the sensor is monochromatic and is the same for all ramps shown in Fig. 8a. So, we can say that the first ramp would be produced for a more intense beam than that of the last ramp. Furthermore, the beam that produces the first ramp is approximately five times more intense than that of the last ramp.

On the other hand, in Fig. 9, simulation results of a high current regime are shown.

In Fig. 9a, the PWM V_{out} is presented when the input current were from 50 to 500 nanoA (labels C and D correspond to the lower and the higher intensities respectively), comparatively with the results of figure 8a, after certain light intensity is not possible discriminate between the V_{out} ramps (intensities C and D can't be differentiated). In this case, the output current is directly proportional to the current sensor and it is processed by the direct mode circuit. In Fig. 8a, the step of current is constant at a low value, approximately 1.6 microA, and starts at different times; on the other hand, in Fig. 9a, the current steps are variable in amplitude and practically start at the same time. This way, it can be decided when direct mode is working.

The output current, I_{out} , is the addition of I_{ph} - I_{bias} when the output voltage switch to the direct mode and I_{ph} is higher than I_{bias} a detectable I_{out} current is obtained. Thenceforth, the output current is used to estimate the light intensity.

Let us suppose, again, that it is the real response of the circuit under illumination, and the light shining on the sensor is monochromatic and is the same for all output currents. Clearly, the higher current corresponds to the more intense beam.

As mentioned above, both topologies work for different illumination intensities; this allows increasing the DR. PWM topology works at tenuous light and direct current mode topology works at brighter illumination.

The circuit was simulated with HSPICE [7], and implemented in a CMOS technology of 0.5um from MOSIS. Fig. 10 shows, the layout of one pixel.

To measure the robustness of the design against process variations, 4-corners simulation is used submitting the circuit to extreme conditions.

Two examples of 4-corners simulation with 100 and 600 picoA input current (labeled Typ1 and Typ2, respectively) using PWM mode readout are shown in Fig. 11; as it can be seen in the first case (Typ1), there is no difference between the 4 simulations.

In the second case (Typ2), the maximum error was less than 5%, however the variation in the voltage step is 10% approximately.

Fig. 12 presents two examples of 4-corners simulation with 4 and 10 microA input current (labeled Typ1 and Typ2, respectively), in this case direct mode readout is used. In both cases, the worst case variation was 10% reflecting the 10% variations of the Vout.



Figure 10. Layout of the PWM and direct mode circuit. The sensor area is 13x13 square microns, and the total area is 50x50 square microns.



Figure 11. 4-corners simulation for PWM circuit with 100 and 600 picoA input currents, for the low current regimen no difference is observed. The high regime current shows variations of 5% in the ramp voltage and 10% in the voltage step.



Figure 12. 4-corner simulation for direct mode circuit with 4 and 10 microA input currents, variations up to 10% are obtained.

Fig. 13 presents Vout for PWM circuit and lout for direct mode circuit; as it can be seen in the low current regimen the PWM works well up to $1X10^{-08}$ A; after this value, the output current starts to be registered. Consequently, the DR obtained is 160 dB.

In Table 1, a comparison between different topologies using the multimode techniques to increase DR is presented. From the table is inferred that only one, the Lineal-Logarithmic, reports a higher DR than the one presented here. However, the authors [10] used a smaller technology and they do not report the power consumption.

Other articles present DR that exceeds the one reported here, but these works do not use the multimode technique, neither the same technology [13]. Some reports not even mention the methods or techniques used to obtain a high DR [14].



Figure 13. PWM and direct mode range comparison.

TABLE I. MULTIMODE SENSING TECHNIQUES COMPARISON

	Specifications					
	Tech	DR	Area	Power consumption	Year	Ref
Lineal – Logarithmic	0.35	124	7.5x7.5		2005	8
Lineal – Logarithmic	0.18	143	5.6x5.6	61mW y 84mW	2006	9
Lineal – Logarithmic	0.35	200	20x20		2006	10
Lineal – Logarithmic	0.35	112	9.4x9.4		2011	11
PWM - PFM	0.18	143	30x30	175mW	2011	12
PWM – Direct Mode	0.5	160	50x50	36uW		This work

Another advantage of our approach is the lowest power consumption compared with those in Table 1. This is due to the fact that FVF working in current mode consumes negligible power, and has low input impedance.

IV. CONCLUSIONS

A new topology using multimode sensing that increases DR has been demonstrated. PWM and direct techniques were combined to improve the DR obtaining 160 dB.

Using this technique and 0.5 microns CMOS technology, a single pixel circuit was designed, occupying 50x50 square microns of total area. In order to reduce area, an operational amplifier is shared by both techniques.

Compared with other circuits reported in the literature, our approach has one of the highest DR, and the smaller power consumption, as demonstrated by simulation. However, I_{out} variations can be as high as 10%. Nevertheless, we have to mention that we did not yet work to improve these variations.

REFERENCES

- J. Ohta, "Smart CMOS Image Sensors and Applications", CRC Press, 2008.
- [2] A. Spivak, A. Belenky, A. Fish, and O. Yadid-Pecht "Wide-dynamicrange CMOS image sensors: comparative performance analysis", IEEE Transactions On Electron Devices, vol. 56, no. 11, Nov. 2009, pp. 2446-2461.
- [3] D. Park, J. Rhee, and Y. Joo "A wide dynamic-range CMOS image sensor using self-reset technique", IEEE Electron Device Letters, vol. 28, no. 10, Oct. 2007, pp. 890-892.
- [4] B. Goldstein, D. Kim, A. Rottigni, J. Xu, T. K. Vanderlick, and E. Culurciello "Cmos low current measurement system for biomedical applications" IEEE International Symposium on Circuits and Systems (ISCAS), May. 2011, pp. 1017-1020.
- [5] A.Zarándy, "Focal-Plane Sensor-Processor Chips", Springer, 2011.
- [6] R. González, et al. "The flipped voltage follower: A useful cell for low voltage low power circuits design", IEEE Transactions On Circuits And Systems, vol. 52, no. 7, Jul. 2005, pp. 1276-1291.
- [7] Synopsys, "HSPICE", URL: http://www.synopsys.com/, 2013.

- [8] K. Hara, H. Kubo, M. Kimura, F. Murao, and S. Komori "A linearlogarithmic cmos sensor with offset calibration using an injected charge signal", IEEE International Solid-State Circuits Conference, vol. 1, Feb. 2005, pp. 354-603.
- [9] G. Storm, R. Henderson, J. E. D. Hurwitz, D. Renshaw, K. Findlater, and M. Purcell "Extended dynamic range from a combined linearlogarithmic cmos image sensor", IEEE Journal Of Solid-State Circuits, vol. 41, no. 9, Sep. 2006, pp. 2095-2106.
- [10] N. Akahane, R. Ryuzaki, S. Adachi, K. Mizobuchi, and S. Sugawa "A 200dB dynamic range iris-less cmos image", IEEE International Solid-State Circuits Conference, Feb. 2006, pp. 1161-1170.
- [11] M. Vatteroni, P. Valdastri, A. Sartori, A. Menciassi, and P. Dario "Linear-logarithmic cmos pixel with tunable dynamic range", IEEE Transactions On Electron Devices, vol. 58, no. 4, Apr. 2011, pp. 1108-1115.

- [12] C. Posch, D. Matolin, and R. Wohlgenannt "A qvga 143 dB dynamic range frame free pwm image sensor with lossless pixel", IEEE Journal Of Solid-State Circuits, vol. 46, no. 1, Jan. 2011, pp. 259-275.
- [13] N. Ide, W. Lee, N. Akahane, and S. Sugawa "A wide DR and linear response cmos image sensor with three photocurrent integrations in photodiodes, lateral overflow capacitors, and column capacitors", IEEE Journal Of Solid-State Circuits, vol. 43, no. 7, Jul. 2008, pp. 1577-1587.
- [14] Omron, "German venture company develops highly advanced wide dynamic range cmos image sensor", URL: http:// industrial.omron.fr/fr/news/news/cmos-image-sensor, 2003.



Figure 8. Simulations results of a low intensity light regimen, a) after 200us the Vpd linear decay starts and after reaching the reference a constant voltage is obtained, b) low intensities light sweep presents different integration time proportional to the light intensity.



Figure 9. Outputs Simulations results of a high intensity light regimen, a) the Vpd linear decay is too fast and it is not differentiable due to the high current, then b) the current is measured straight forward.