Edge-Based Technique for Ultra-Fast Gating of Large Array Imagers

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***Abstract*— Ultra-fast gating of large array imagers can be quite challenging to implement due to the distributed RC (Resistance Capacitance) nature of the metal wires used in all ICs (Integrated Circuits) for electrical connections. For the transmission of a signal across a long path, the metal line reduces the electrical bandwidth and adds a delay. The behavior of these lines has been modeled and a new solution is presented to circumvent these limitations. In this paper, we present an edge-based approach to the gating circuitry that allows sub nanosecond gating with a very low skew across the whole imager. Simulation data shows that our solution is an efficient way of reducing the effect of the distributed RC line delay with a small penalty on surface area and consumption.**

Keywords—SPAD, Ultra-fast Gating, Edge-triggered, Fast Pulse, skewless

I. INTRODUCTION

Over the last decade, ultra-fast imaging has been a booming field with many considerable breakthroughs. A key advancement to this technology has been the ability to design image sensors with a sub-nanosecond temporal resolution. These imagers could be configured in either single-shot mode in [4] and [6], or can be repetitive and based on Single-Photon Avalanche Diode (SPAD) arrays rather than classical photodiodes. In this case, the temporal resolution can be even lower. Currently, integrated streak cameras operate at the fastest frequency, therefore also requiring robust acquisition signals. These fast signals are used in order to have a sub-nanosecond shutter speed. Depending on the design, the temporal resolution of an integrated streak camera can vary from a few hundred picoseconds to several nanoseconds. A 1D [5] or 2D [4] approach of integrated streak camera solution can be found in [5], where a delay generator based on the propagation delay of logic gates is used for sub-nanosecond shuttering. The delay could be customized using current starved inverters. In [3] and [4], we see the use of edge-based control signals for fast gating.

Similar to a clock signal in a synchronous sequential circuit, the gating signals are distributed to the entire imager array. Due to the distributed RC (Resistance capacitance) line delay, the integrity of the signal is compromised along the row of pixels. This would degrade the performance as a pixel at the end of the array would not perceive the same signal as another near the beginning of the array. Moreover, it would be completely unusable for ultra-fast gating purposes as the rise time and fall time would be far greater than the gating time. This is especially true for ultra-fast image sensors as a signal commutes at the order of 100 picoseconds. It behooves us then to ensure that the signal is identical and useable for every single pixel in the array. Therefore, a more reliable approach would be to reduce the dependency on the pulse width and have an edge triggered gating. This solution was implemented in a 0.18 µm process. These approaches have been applied for smaller dimension image sensors and it is therefore interesting to propose a solution that is extendable to full resolution imagers.

II. THEORETICAL APPROACH

As mentioned before, in an imager array, the gating signal is being driven at the beginning of a row. Therefore, the signal perceived at the end of the row will no longer be a clean square pulse. Hence, it is interesting to study what the maximum row length for which the pulse will still be useable. Firstly, we can model this problem by looking at a single distributed RC model. Figure 1 shows the equivalent distributed line representation of a row containing N pixels where R_D and C_D are the resistance and the capacitance per length unit of the metal line respectively. The localized pixel input capacitances C_{pixel} act like a distributed capacitance according to the pixel pitch $C_{D_{pixel}}$ where,

$$C_{D_{Pixel}} = \frac{C_{pixel}}{\text{Pixel Pitch}} \tag{1}$$

The total distributed capacitance $C_{D_{total}}$ is thus given by the sum of the equivalent distributed input pixel capacitance and the line distributed capacitance, $C_{D_{total}} = C_D + C_{D_{pixel}}$.

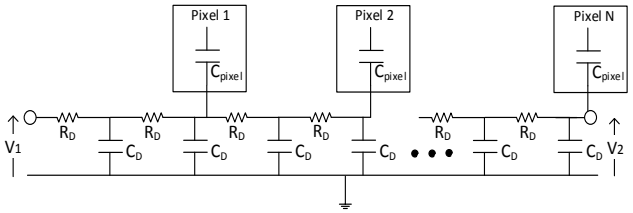

Figure 1. Distributed RC line representation of a sensor row including N Pixels.

The open-circuited Laplace transfer function from the beginning of the line V_1 to the end of the line V_2 can be written as [1][3]:

$$H(s) = \frac{V_2}{V_1} = \frac{1}{\cosh\sqrt{s \cdot R_D C_{D_{total}} \cdot l}}\ , \qquad (2)$$

where *s* is the Laplace variable, and *l* the length of the row. The behavior of the line can be approximated by the simplified circuit model depicted in Figure 2[2].

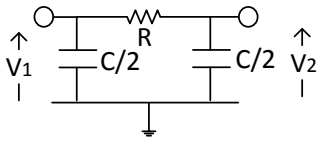

Figure 2. Simplified circuit of entire line

Where $R = R_D \cdot l$ and $C = C_{D_{total}} \cdot l$ are the total resistance and capacitance of the line. The unit step response gives us a clear indication that while not perfect, this approximation is sufficient to illustrate the distributed RC delay problem [2]. The distributed RC effect acrosss the line therefore affects the driver rise time. The fastest rise time of V_2 can thus be obtained by the following expression:

$$T_R = 0.35\pi \cdot R_D \left(C_D + C_{D_{pixel}}\right) \cdot l^2 \qquad (3)$$

Equation (3) states that the rising time increases with the square of the row length *l* and then can dramatically reach a value that makes it impossible to transport a nanosecond pulse across a large array sensor.

A. Parameters extraction

The parameters R_D and C_D can generally be found in the design kit documentation. Otherwise, the unit line and surface capacitance can be obtained by an analog extracted view simulation. Based on variants (square and rectangular) of the diagram in Figure 3, theses parameters can be deduced with two different sets of equations (4).

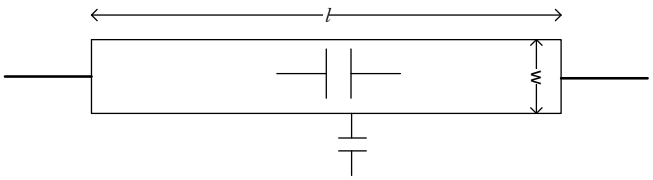

Figure 3. Diagram of layout model variants used (line and rectangle)

$$C_{line} = 2 \cdot C_{edge}\left(l + w\right) + C_{surface} \cdot w \cdot l \qquad (4)$$

Where *w* and *l* are respectively the width and the length of the line, C_{line} is the extracted line capacitance, C_{edge} is the edge capacitance, given in F/m, and $C_{surface}$ the surface capacitance of the line, given in F/m².

Then, the distributed capacitance for a long line can be approximated by:

$$C_D = 2 \cdot C_{edge} + C_{surface} \cdot w\,, \qquad (5)$$

where *w* is the width of the considered line.

The resistivity can be extracted in the same way or it can be obtained by process data, such as the metal resistivity ρ and thickness *T*. Therefore, the resistance per length unit R_D of a line of width *w* is given by:

$$R_D = \frac{\rho}{w \cdot T} \qquad (6)$$

III. Ultra-Fast Gating for Large Array Sensor

The Figure 4 shows the shape of a 1 ns pulse propagating in a sensor row at the beginning of the line, where the pulse is applied, in the middle and at the end of the line. If we assume the classic case where the logic of the pixel reshapes the pulse with a threshold voltage of half the power supply (solid line in Figure 4), we clearly see that after a certain length, the conventional gating is no longer adequate.

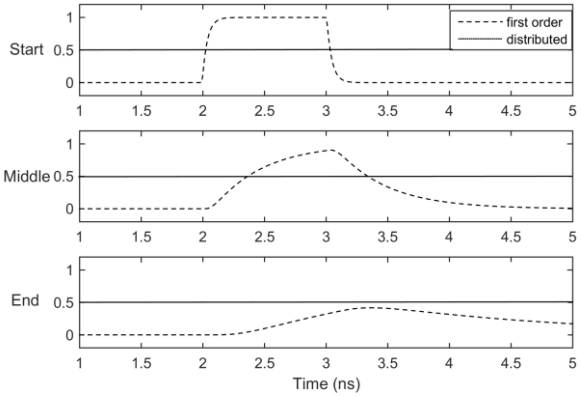

Figure 4. Illustration of lost signal integrity across a row of pixels

Furthermore, it is interesting to create a model in order to anticipate this signal distortion with respect to the length of the sensor. Based on the distributed model and a voltage threshold of half the power supply, Figure 5 compares the Full-Width at Half Maximum (FWHM) ratio of the in-pixel reshaped pulse versus the original pulse according to the original pulse FWHM to the rise time. The effective FWHM inside the pixel decreases as soon as the original FWHM pulse is below the rising time and is reduced to zero for a ratio of 30%.

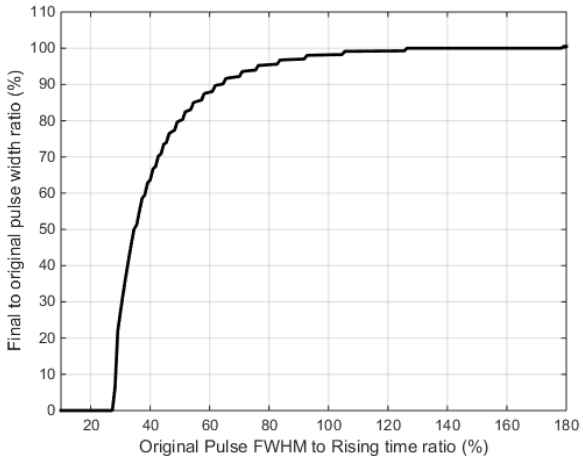

Figure 5. Final to original pulse width ratio versus the original pulse width to rising time ratio.

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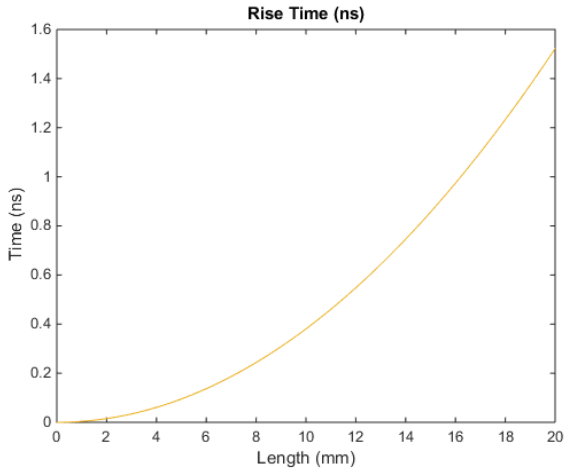

Figure 6. Rise Time of a signal seen across a pixel row through a metal line of up to 20 mm and a pixel pitch of 35 µm with the following parameters: ρ = 2.65.10^{-8} Ω.m, T = 425 nm, C_{pixel} = 2 fF, $C_{surface}$ = 0.015 fF/µm², C_{edge} = 0.032 fF/µm and w = 3 µm.

Using (3), the relationship between the increasing rise time and the length of the array is shown in Figure 6 for a metal line, level 2, of a typical 0.18 µm CMOS (Complementary Metal Oxide Semiconductor) process with a resistivity ρ of 2.65.10^{-8} Ω.m, a thickness T of 425 nm, a pixel pitch of 35 µm, an input pixel capacitance of C_{pixel} of 2 fF, a surface capacitance $C_{surface}$ of 0.015 fF/µm², an edge capacitance C_{edge} of 0.032 fF/µm and a width w of 3 µm. Sub-nanosecond rise times are not allowed for sensor dimensions above 16 mm.

A way to enhance the line bandwidth is to increase the line width w because it reduces the resistance of the line. Figure 7 shows the calculated rise time in the middle of the previous line according to the metal width w. Increasing the width of the metal track above 3 µm has minimal impact on rise time and thus becomes irrelevant.

Therefore, generating 200 ps FWHM gating within large sensor arrays over 10 mm is impossible with pulse propagation techniques. To ensure signal integrity, the use of edge-sensitive logic is mandatory.

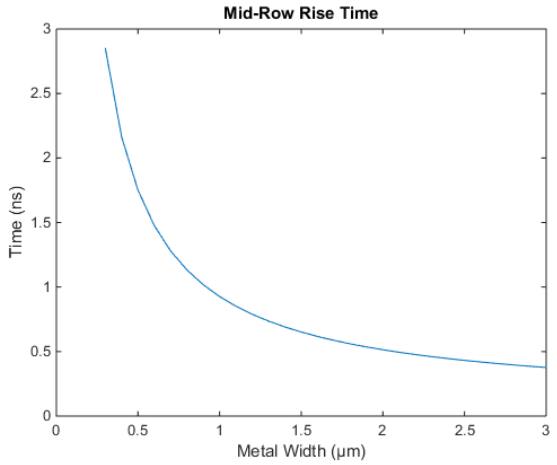

Figure 7. Rise Time with respect to metal track width at midway along a row of pixels

IV. Proposed Design of Edge-Triggered Gating

A. Edge-based Circuit for Ultra-fast Gating

In SPAD array image sensors, for ultra-fast gating mode there are three critical signals needed for optimal operation: Quench, Reset and Gate. Moreover, SPADs could be gated immediately after the reset to avoid the detection of photons arriving before the investigation time slot. While Quench is a much slower signal, the Reset and Gate signals can be sub-nanosecond pulses.

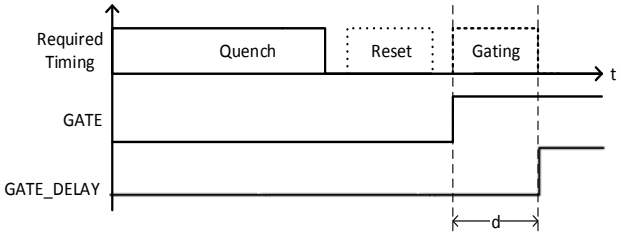

Figure 8. Timing diagram of typical SPAD quench, reset and gating with delayed (d) edge-based signals below.

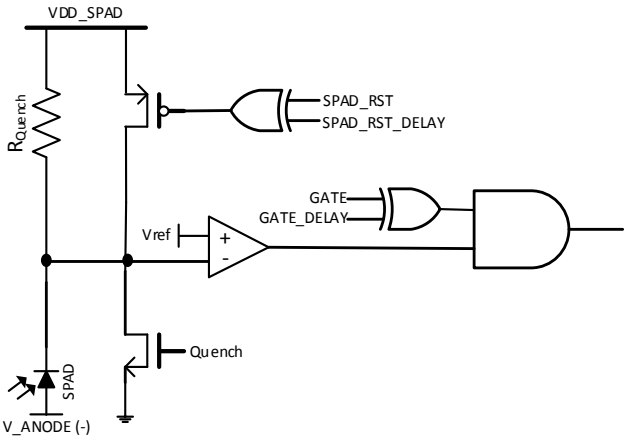

Figure 9. SPAD Edge-triggered circuit with active quench, reset and gating

Having shown clear limitations for ultra-fast gating in large SPAD array image sensors, a different approach is needed. This approach consists of an additional signal GATE_DELAY (Figure 8). GATE_DELAY is delayed thus creating the effective pulse of width d seen above through an XOR gate. It can therefore be extended to the Reset signal of the SPAD as seen in Figure 9. Hence, we are able to achieve gating in the range of 100 ps up to 1 ns while maintaining signal integrity throughout the SPAD array. Quenching time is much longer than the reset and gating signals and do not require an ultrafast signal generation.

B. Edge-based Driver for Ultra-fast Gating

In Figure 9, it can be seen that the GATE signal is delayed to obtain a GATE_DELAY signal. In order to generate the delay, we used a delay generator to drive the signals. The delay generator is constructed using a series of current starved double inverters as seen in [7].

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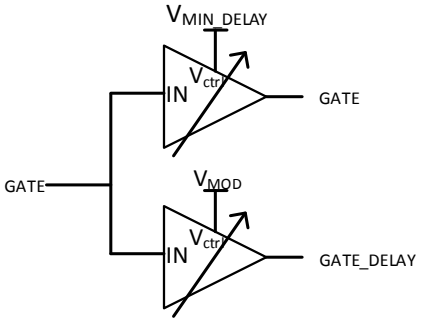

Figure 10. Delay generator block made up of double current starved inverters used to create GATE and GATE_DELAY signals

The delay of both signals (Figure 10) can be determined by a modifiable control voltage (V_{ctrl}). We are able to modify the pulse width by splitting the signal in two branches with one providing minimal propagation delay and the other being delayed with respect to the other. Both signals are then fed into an in-pixel XOR gate to obtain the desired pulse derived from the delay between the two signals.

C. Simulation of Edge-based technique

The presented solution can be demonstrated and validated through a Cadence simulation with two buffered lines of 20 mm long and a width of 3 µm based on the model presented in this paper in order to obtain a 300 ps pulse through an XOR gate.

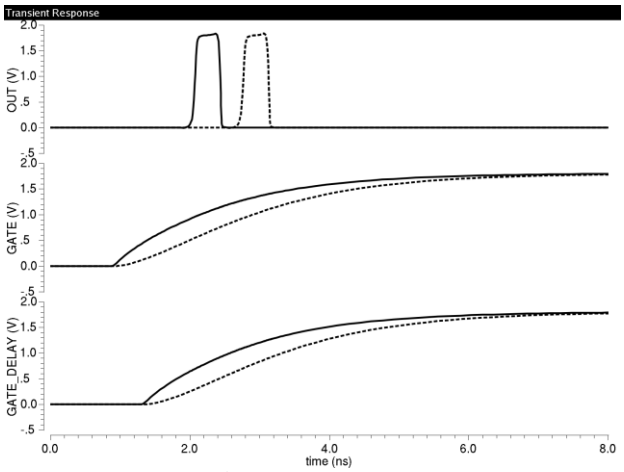

Figure 11. Simulation of a 300 ps pulse created using the edge-based technique (line: 20 mm length, 3 µm width). Signals at the beginning of the line (solid line) and at the end (dotted line)

In Figure 11, the FWHM of the pulse is 300 ps and our solution performs well in a Cadence simulation using the model presented in Figure 2 and the defining equations shown previously. However, a non-negligible skew is present.

V. ANALYSIS AND ELIMINATION OF SKEW

For large array ultra-fast image sensors, ensuring signal integrity across the array is only half of the challenge. As can be seen in Figure 6, a 20 mm sensor will introduce a skew of around 1.5 ns. Hence, the edge based technique is not sufficient for larger dimensions.

In order to present a more robust approach on ultra-fast gating, we proceed to eliminate the large skew present across the array mentioned. This can be done by introducing two skewed inverters on each branch (GATE and GATE_DELAY) before the XOR gate. The threshold voltage of each inverter can be modified by altering the beta ratio effects inside each inverter. Hence, the skew across the sensor array can be compensated.

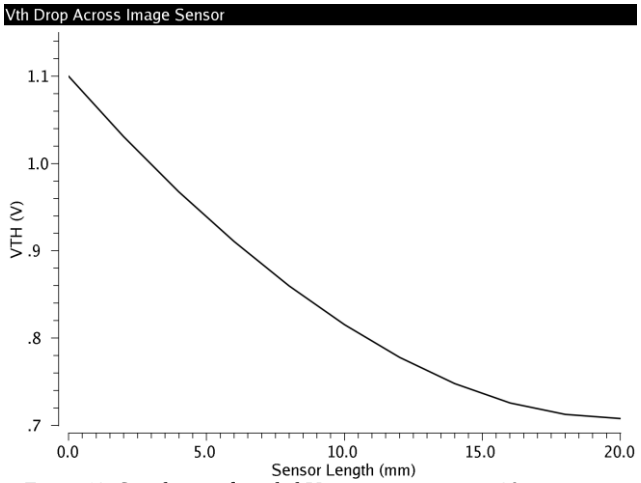

Figure 12. Simulation of needed V_{TH} variation across a 20 mm image sensor row using above mentioned parameters.

Figure 12 shows the simulation of needed V_{TH} variation across a 20 mm image sensor row using above mentioned parameters. The threshold voltage at the beginning of the sensor is arbitrary set at 1.1 V (above $V_{DD}/2$ where V_{DD} = 1.8 V) in order to maintain threshold levels across the array well above the $|V_T|$ of each transistor. For a required voltage V_{TH}, the inverter should be adjusted by modifying the geometry of the PMOS and NMOS transistors, thus changing the beta ratio.

This can be obtained by solving the following equation:

$$I_n = I_p, \text{for } \begin{cases} V_{in} = V_{th} \\ V_{out} = VDD/2 \end{cases} \quad (7)$$

In this case, both the NMOS and the PMOS transistor are in the saturated operation region, thus the currents are given by:

$$I_n = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)\left(V_{TH} - V_{T_N}\right)^2\left(1+\lambda\frac{V_{DD}}{2}\right)$$
$$I_p = \frac{1}{2}\mu_p C_{ox}\left(\frac{W_p}{L_p}\right)\left(V_{DD} - V_{TH} - \left|V_{T_N}\right|\right)^2\left(1+\lambda\frac{V_{DD}}{2}\right) \quad (8)$$

Replacing I_n and I_p in equation (7) leads to:

$$\mu_n\left(\frac{W_n}{L_n}\right)\left(V_{TH} - V_T\right)^2 = \mu_p\left(\frac{W_p}{L_p}\right)\left(V_{DD} - V_{TH} - \left|V_{Tp}\right|\right)^2 \quad (9)$$

Hence, we obtain the ratio ρ:

$$\rho = \frac{\left(\frac{W_p}{L_p}\right)}{\left(\frac{W_n}{L_n}\right)} = \frac{\mu_n}{\mu_p} \frac{\left(V_{TH} - V_T\right)^2}{\left(V_{DD} - V_{TH} - \left|V_{Tp}\right|\right)^2} \quad (10)$$

Furthermore, in order to keep the best fill factor, the inverter area A given by:

$$A = W_p L_p + L_n W_n = \rho \left(\frac{W_n}{L_n}\right) L_p^{\,2} + \left(\frac{L_n}{W_n}\right) W_n^{\,2} \quad (11)$$

has to be keep as low as possible. For a threshold voltage V_{th} above $V_{DD}/2$, the PMOS transistor has to be more conductive than the NMOS one, thus the ratio ρ should be greater than one. For this, we can consider using $W_n = W_{min}$ and $L_p = L_{min}$ as the best choice. The inverter area becomes:

$$A = \rho \left(\frac{W_n}{L_n}\right) L_{\min}^2 + \left(\frac{L_n}{W_n}\right) W_{\min}^2 = \rho \alpha L_{\min}^2 + \frac{1}{\alpha} W_{\min}^2 \quad (12)$$

Minimizing A according to the variable α leads to best sizes of the MOS transistors for the smallest use of surface area:

$$\frac{W_n}{L_n} = \frac{W_{\min}}{\sqrt{\rho} \cdot L_{\min}} \text{ and } \frac{W_p}{L_p} = \frac{\sqrt{\rho} \cdot W_{\min}}{L_{\min}} \quad (13)$$

In a similar way, the optimal sizes of the transistors for a threshold voltage V_{TH} under $V_{DD}/2$ can be computed as:

$$\frac{W_n}{L_n} = \frac{\sqrt{\rho} \cdot W_{\min}}{L_{\min}} \text{ and } \frac{W_p}{L_p} = \frac{W_{\min}}{\sqrt{\rho} \cdot L_{\min}} \quad (14)$$

In both case, the area of each threshold adjusted inverter is given by:

$$A = W_{\min} L_{\min} \sqrt{4\rho} \quad (15)$$

The more ratio ρ is distant from 1, the higher the surface area.

It would be ideal to designate an area of a pixel for the placement of automatically generated skewed inverters based on their position in the sensor row.

By employing this technique, it can be seen in Figure 13 that the pulse at the beginning of the sensor row and the pulse at the end are synchronized and the skew seen in Figure 11 is eliminated.

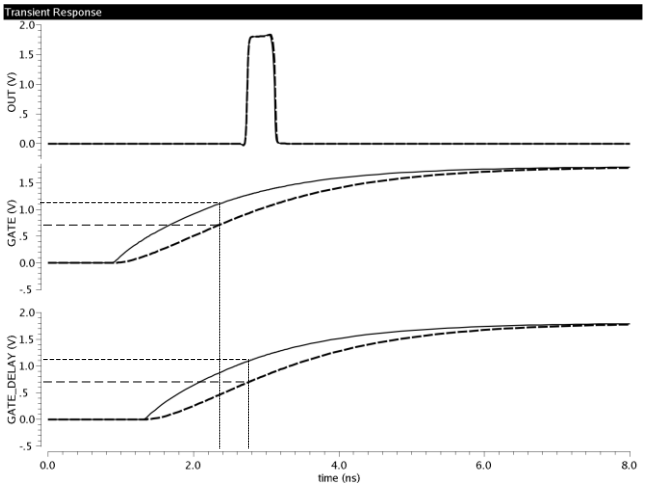

Figure 13. Simulation of skewless pulse. Solid line: signal at the beginning of the sensor, dotted line: signal at the end of a 20 mm sensor.

In an ideal fabrication process, this technique coupled with the edge-gating approach previously developed and is optimal for sub-nanosecond ultra-fast gating. Moreover, after performing a Monte-Carlo simulation on the possible dispersion existing between the two pulses (beginning and end of line), we obtain a sigma of only 18.42 ps. In order to circumvent the inevitable mismatch, it is conceivable to modify (post-fab) the supply voltages of the inverters added in order to fine tune the additional skew.

VI. CONCLUSION

In the increasingly relevant field of ultra-fast imaging, gating signals play a key role in assuring optimal operation. When designing large resolution sensors, acquisition pulses must be uniformly distributed throughout the entire array. Due to the delay effect of a distributed RC line, this becomes troublesome. For this, a conventional driver at the beginning of the line is no longer adequate and a more robust solution needs to be implemented. This new approach is independent to pulse-based gating and instead uses an edge-triggered gating. Moreover, the designer could place such edge-based drivers on either side of the sensor to obtain a near-perfect gating signal distribution. While this technique is still hindered by signal skew, it can be eliminated using the method presented in this paper.

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