Cost-effective Sensor Nodes for Wireless Sensor Networks

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Abstract— **Cost reduction in wireless sensor networks becomes an important requirement to extend their application in fields where a great amount of sensors is needed. Traditional approach to use multichannel analog-to-digital converter and/or analog multiplexers for analog sensors will not give any reduction in price. Moreover, the analog multiplexer introduces additional measuring error. This paper describes in details the developed advanced, robust but cost-effective sensor nodes' architectures suitable for further integration in a node-on-chip. Such sensor nodes can work with any analog and quasi-digital sensors and transducers, and its sensing sub-system lets achieve the best metrological performances. A comprehensive comparative study of sensor node's architectures and sensing sub-systems are presented.**

Keywords-sensor nodes; wireless sensor networks, frequency-to-digital converter, universal sensors and transducers interface, node-on-chip

I. INTRODUCTION

Wireless sensors and sensor networks can be deployed almost anywhere at a far lower cost than can a wired system. With the recent advances in embedded systems and wireless technology, the hardware used is becoming more inexpensive and more widely available. Wireless sensor devices connect sensors wirelessly among each other as well as to monitoring and management setups. According to the MarketResearch.com the global market for wireless sensor devices used in end vertical applications totaled $ US 790 million in 2011 and expected to increase at a 43.1 % compound annual growth rate (CAGR) and reach an estimated $ US 4.7 billion by 2016 [1].

Because wireless sensor networking is built around low-power radios, the nodes that make up the network play a key role in wireless communication. From a physical perspective, the deployment of nodes may take several forms depending on the sensor application and the desired pattern of communication. Deployment may also be a one-time activity, where the installation and use of a sensor network are strictly separate activities. It can also be a continuous process where more nodes are deployed over the lifetime of the network [2]. The application can vary from a single sensor node to multiple sensor nodes.

A wireless sensor net is made up of a group of sensor nodes. Wireless sensor nodes are the essential building blocks in a wireless sensor network. Each sensor node possesses the ability to monitor some aspect of its environment, and each is able to communicate its observations through other nodes to a destination where data from the network is gathered and processed. Recent developments in wireless technologies and the semiconductor fabrication of miniature sensors are making wireless sensor networks (WSNs) smaller and more cost-effective for a growing number of uses [3].

Cost reduction in wireless sensor networks becomes a requirement to extend their application in fields where a great amount of sensors is needed [4], for example, industrial applications. In this case it should be a good solution to connect many existing low-cost sensors both: analog and quasi-digital to one sensor node to reduce the cost of nodes. Traditional approach to use multichannel analog-to-digital converter (ADC) and/or analog multiplexers for analog sensors will not give any reduction in price. Moreover, the analog multiplexer introduces additional measuring error. Hence, the analog signal must be preliminary converted to the quasi-digital signal (frequency, period, duty-cycle, time interval, phase-shift, pulse number or pulse-width modulated (PWM) output).

The described in [4] sensor interface transforms the voltage provided by various sensors with different output ranges to a pulse signal, which frequency will depend proportionally on the input voltage. The conversion of the sensor signal to a frequency value will bear much less sensitivity to interferences. The further frequency-to-digital conversion is performed by using the classical direct counting method. This technique counts the number of pulses N_x of a signal of unknown period $T_x=1/f_x$ during a gate time window T_0 determined by n periods of a signal of known, reference frequency f_0. The unknown frequency f_x is calculated by the number of pulses into the counting window:

$$N_x = n \cdot \frac{T_0}{T_x} \Rightarrow f_x = \frac{N_x}{n \cdot T_0}. \qquad (1)$$

Such classical method has two well known disadvantages: the dependence of relative quantization error δ_x on frequency f_x, and redundant conversion time determined by the constant gate time T_0. In order to achieve acceptable performance in the conversion to digital values of the frequency signal, it is necessary to the different sensor output ranges are converted into the same frequency range. For this, the conditioning electronics must be able to change sensor's gain and offset voltage depending on the sensor signal characteristics.

The circuit [4] consists of two operational amplifiers, analog multiplexer, two programmable potentiometers and voltage-controlled oscillator, which performs the transformation to the frequency range. The low resolution serial digital-to-analog converter is used for self-calibration purposes. When a node of the network is activated, the microcontroller selects the sensor to be read by means of the control lines of the analogue multiplexer and carry out the conditioning and the conversion. However, such sensor interface has some disadvantages. It introduces additional error, because of mainly based on analog electronics components.

Mantracourt Electronics Ltd. (UK) manufactures Wireless Telemetry Pulse Acquisition Module (T24-PA) for quasi-digital sensors and transducers with frequency range from 0.5 Hz to 3 kHz and relative error 0.15 ... 0.25 % [5]. It can not be used with various quasi-digital sensors and transducers, which as rule have very broad dynamic frequency range: form part of Hz to some tens MHz, and low relative error 0.01 % and better [6]. In order to get the optimal trade-off between metrological performances and price for the sensor node it is expediently to use other, universal, advanced solutions based on the novel frequency-to-digital conversion method.

In order to design cost-effective sensor nodes, which satisfy to modern requirements, the following measures must be realized. Instead of voltage or current sensors, so-called quasi-digital sensors with frequency, period, time interval, phase-shift, pulse number or PWM output must be used. The frequency-to-digital converter should be based on the advanced method for frequency measurements, which have not disadvantages, mentioned above. In case of analog output sensors, the intermediate voltage-to-frequency converter(s) should be used.

The aim of this paper is to describe in details the developed advanced but cost-effective sensor nodes' architectures suitable for further integration in a node-on-chip for wireless sensor networks. The paper consists of four parts and is organized as follows. The first part includes state-of-the-art review and task definition. The second part describes a design approach for sensor nodes architectures based on a Universal Sensors and Transducers Interface circuit (USTI) and are suitable for any quasi-digital sensors and analog sensors, and the third part is devoted to the further design of a node-on-chip based on the USTI-WSN IC. The forth part includes results of experimental investigation of sensing sub-system based on the USTI IC. The last part of the paper provides conclusions and future research directions.

II. SENSOR NODES' ARCHITECTURES

A sensor node in a wireless sensor network is capable of performing some processing, gathering sensory information and communicating with other connected nodes in the network. Its architecture consists of the following components: sensing sub-system, processing sub-system, communication sub-system and power management sub-system. The sensing sub-system directly influences on metrological performances on the whole. However, during the last years a lot of publications have been devoted mainly to communication and power management sub-systems. This article will be focused on the sensing sub-system design, which satisfies to the modern requirements of relatively low cost, expansibility and power-aware [7]. The low cost means that sensor node should be cheap since wireless sensor network may have hundreds or thousands of sensor nodes. The expansibility signifies that hardware design must be expandable with a number of different quasi-digital and analog sensors to support a variety of applications. The power-aware means that hardware supports intelligent function, which allows algorithms to adapt themselves to the available power.

Let consider several advanced sensor node architectures for analog and quasi-digital sensors and transducers. All these architectures are based on novel USTI ICs developed by authors [8].

A. Sensor node architecture with analog multiplexer

A simple sensor node for analog and quasi-digital sensors with analog multiplexer and time division channeling is shown in Figure 1.

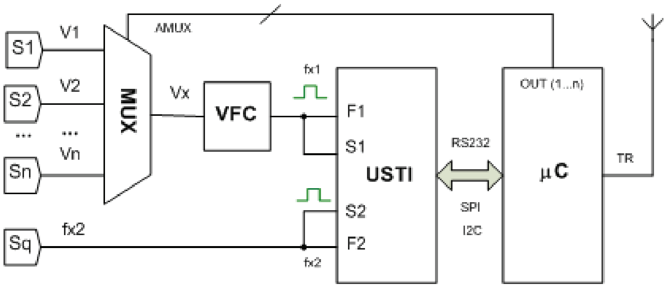


Figure 1. Sensor node with analog multiplexer.

Sensing sub-system in such architecture contains an analog multiplexes (MUX), voltage-to-frequency converter (VFC), and USTI ICs. A processing sub-system, communication sub-system and power management sub-system are realized on a separate microcontroller. The USTI is a core component of the sensing sub-system. It is based on advanced, modified patented frequency (period)-to-digital conversion method of the dependent count with a constant quantization error in all broad frequency range and non-redundant conversion time [8-10]. The dependence of relative error on conversion time is shown in Figure 2.

In this case it is not necessary to convert the different sensor output ranges into the same frequency range, as it was proposed in [4]. Only one voltage-to-frequency converter is used to convert sensor's output to frequency. As usually, integrated VFCs have broad frequency ranges and good metrological performances [11, 12]. In addition, one quasi-digital sensor can be directly connected to the second channel of USTI IC, and one sensing element (resistive, capacitance or resistive bridge) can be also connected to this IC [13].

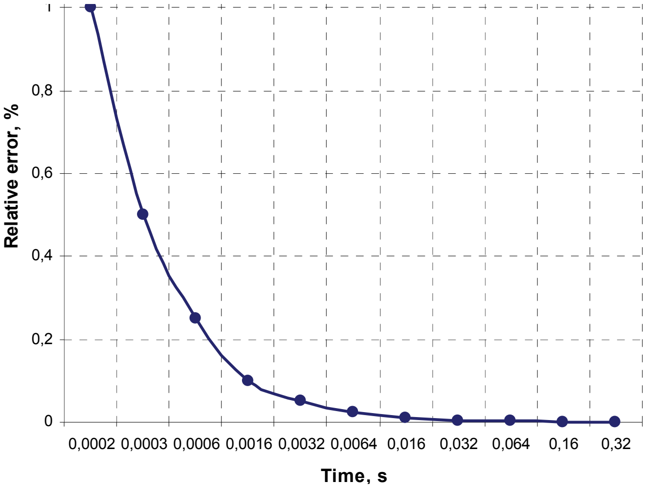


Figure 2. Relative error vs. conversion time.

B. *Sensor node architecture with digital multiplexer*

The analog multiplexer and VFC introduces additional measurement errors. To eliminate the error due to analog multiplexer, it is possible to convert voltage to frequency for each of analog output sensors before the multiplexer, and use a digital multiplexor (MX), instead of analog multiplexer. Such sensor node with the digital multiplexer and combined (time for digital signal domain and space for analog signal domain) channeling is shown in Figure 3.

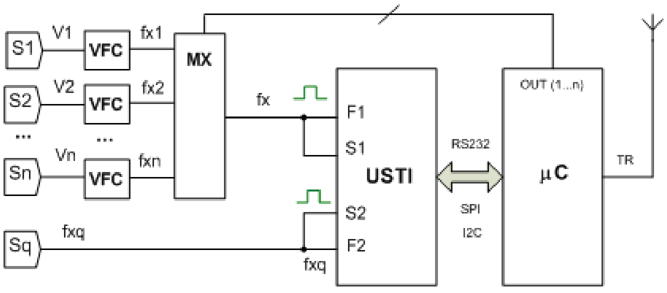


Figure 3. Sensor node with digital multiplexer.

For the time-division channeling, the cycle polling time τ can be calculated according to the following equation [14]:

$$\tau = n \cdot (T_{meas} + \tau_{delay1} + \tau_{delay2}) \,, \qquad (2)$$

where τ_{delay1} is the time delay between the ending of the conversion in the previous sensor and the command to poll the next sensor; τ_{delay2} is the time delay of the frequency conversion starting after the sensor connection; n is the number of sensors in the sensor node; T_{meas} is the measurement time. The measurement time T_{meas} for the USTI includes three main components: conversion rate (t_{conv}), communication time (t_{comm}) and calculations time (t_{calc}) [13].

The digital multiplexer does not introduce any additional error. However, the VFCs still do it. So, the solution with minimum possible hardware and high metrological performance is possible if instead of analog sensors to use quasi-digital sensors.

C. *Sensor node architecture for quasi-digital sensors*

A low-cost sensor node with high metrological performance for quasi-digital sensors and transducers is shown in Figure 4, which addresses the challenges of metrological performance improvement and node's cost reduction [4, 7, 13]. In this sensor node architecture no any VFC is necessary.

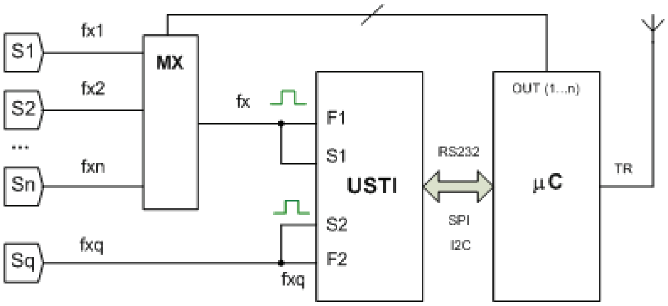


Figure 4. Low cost sensor node for qusi-digital sensors.

By this way it is possible to decrease the total measurement error, for example, from 0.14 % to 0.08 % (for the numerical example, described in [13]), and reduce the sensor node's price. For example, at the same price for analog and quasi-digital sensors, the core of sensor node - the 24-bit resolution, 8-channel ADC ADS1278 [15] costs 23.95 $ US (in quantities of 1,000) while the USTI IC with significantly better metrological performance and a digital 8-channel multiplexer costs only 18.95 $ US in the same quantities.

The space division and combining channeling also can be realized in this sensor node. In such sensor node instead of one USTI and the n-channel digital multiplexer, n ICs (according to the number of channels) and a microprocessor system with n inputs are used. That is, for simultaneous measurement of several frequencies, there is an independent channel with the USTI. The microprocessor simultaneously starts all converters and at the end of the measurement processes reads results. Quasi-digital sensors and transducers can be also connected in pairs to one USTI. In addition, one resistive, capacitive of resistive bridge sensing element can be also connected directly to the USTI. For one's turn, all USTI can be connected to a master microcontroller or microprocessor with the help of SPI or I2C buses. Each USTI IC can serves up to 3 channels by itself in a sensor node.

The cycle polling time τ for the space-division channeling is decreased approximately in k times in comparison with the time-division channeling and should be calculated as:

$$\tau = T_{meas} + t_{readout,} \quad (3)$$

where $t_{readout,}$ is the time for result reading by a microprocessor.

In the case of analog sensors, an addition VFC in each channel should be also used. Such solution lets achieve maximum possible speed at a little bit increased cost for a sensor node.

Another benefit to use quasi-digital sensors and transducers instead of analog sensors in WSN is a possibility to transmit frequency-time signals without preliminary conversion to digital. Two examples are described below.

The RF transmitter using pulse width modulation (PWM) method is reported in [16]. It does not use an analog to digital converter for the RF transmission of analog data. The transmitter consists of a pulse width modulator, a voltage-controlled oscillator (VCO) and on-chip antenna. The PWM method digitally encodes analog signal levels, but the PWM signal remains quasi-digital. By keeping the signal quasi--digital, noise effects are minimized. The modulated signals are inputted into the VCO using PWM. If the voltage of the modulated signal is the high level, the VCO is oscillated, and the RF carrier waves for transmission can be obtained. Then, the output of the VCO is transmitted by the on-chip antenna [16]. The transmitter was possible to transmit with low power dissipation of 0.75 mW the carrier of 315 MHz.

An interdigital capacitor based battery-free wireless pressure sensor is described in [17]. It consists of an interdigital capacitor (IDC) that serves as a pressure sensing element and an inductor, which works as a passive power source and data communication element. These two components work together as an LC resonator to realize the wireless pressure sensing and remote power to eliminate the need for wire connection in conventional pressure sensor. The sensing element is comprised of a set of linear parallel electrodes coated with Polyvinylidene Fluoride pressure sensing material on the top. The change of capacitance in the IDC is a function of the geometry of the electrodes and the electric properties of the sensitive layer. The sensor prototype demonstrated that it performs well in the range of 0 psi to 60 psi with an average pressure sensitivity of 25 kHz/psi [17].

III. NODE-ON-CHIP

The future step to reduce hardware expenses is to use the recently designed IC USTI-WSN of node-on-chip instead of the USTI IC and μC [13]. The USTI-WSN IC contains all sensor node's sub-systems (see Figure 5). The USTI-WSN IC prototype is shown in Figure 6.

The prototype can work with two various quasi-digital sensors or transducers and one sensing element at the same time. It has a high speed embedded transmitter with high data rate transceiver for the 2.4 GHz ISM band. The radio transceiver provides high data rates from 250 kb/s up to 2 Mb/s for wireless communications and provides frame handling, outstanding receiver sensitivity and high transmit output power enabling a very robust wireless communication. High performance RF-CMOS 2.4 GHz radio transceiver designed for industrial and consumer applications targeted for IEEE 802.15.4, ZigBee, IPv6/6LoWPAN, RF4CE, SP100, WirelessHART and ISM applications. Supply voltage is 3.6 V. Power consumption is less than 18.8 mA in active mode, and < 250 nA in sleep mode. The operation temperature range is -40 ºC to 85 ºC.

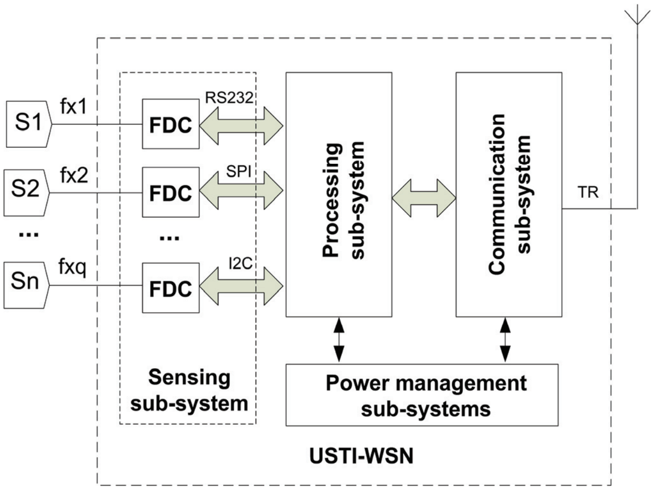


Figure 5. Block-diagram of node-on-chip.

Figure 6. USTI-WSN IC prototype in 64-pad QFN package.

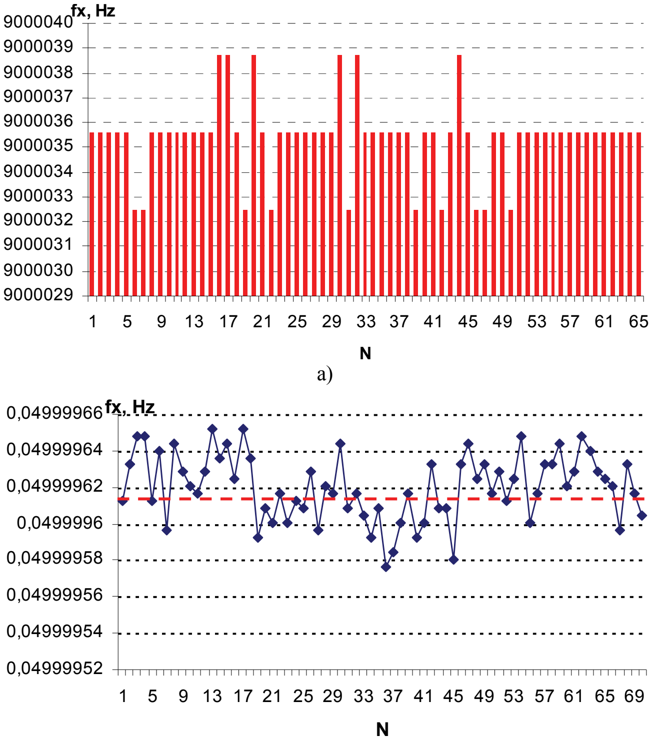
IV. EXPERIMENTAL RESULTS AND FUTURE RESEARCH

The USTI IC has been tested with various quasi-digital temperature, humidity, acceleration, light, displacement, etc. sensors with frequency, period, duty-cycle and PWM outputs, and sensing elements such as resistive, capacitive and resistive bridges. The maximal possible input frequency of a square waveform pulse signal for the USTI was 9.1 MHz without prescaling, the minimal possible frequency was 0.04 Hz. The IC was programmed to measure frequency with the minimal possible relative error δ_x=±0.0005 %. Experimental results of measurements for 9 MHz and 0.05 Hz frequencies square waveform pulse signals are shown in Figure 7 (a) and 7 (b) respectively.

Before measurements, the USTI was calibrated in the working temperature range: +23.5 ºC … + 25.4 ºC with the purpose to compensate the quartz oscillator's systematic error [18]. The statistical characteristics are presented in Table I.

As it is visible from the table, the maximal relative error does not exceed the programmable $\delta_x < \pm 0.0005$ % in all frequency range including high and infralow frequencies.

For 0.05 Hz frequency the relative error does not exceed $\delta_x = \pm 0.00009\ \% < \pm 0.0005\ \%$.



a)

b)

Figure 7. Experimental results for frequency measurements: 9 MHz (a), and 0.05 Hz (b).

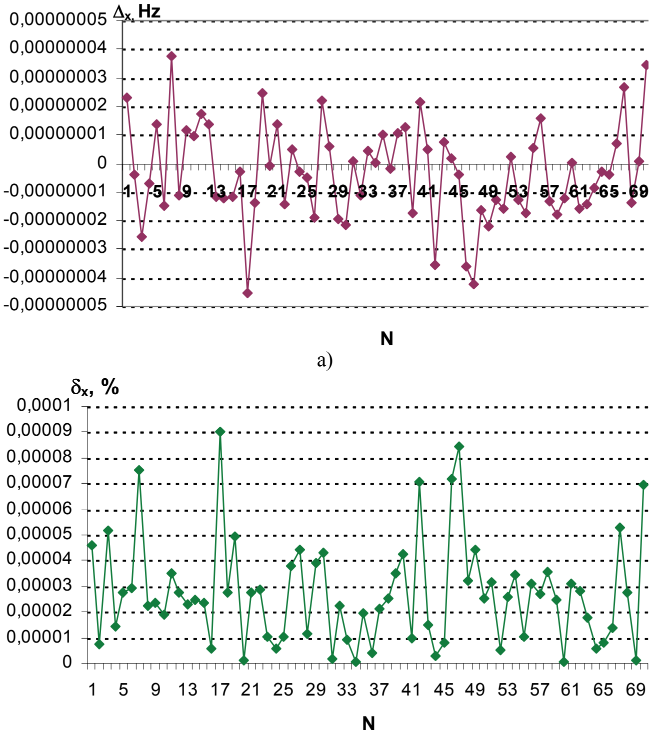
TABLE I. STATISTICAL CHARACTERISTICS.

Parameter	Value *fx*	
	9 MHz	0.05 Hz
Number of measurements, *N*	65	70
Minimum f_x (min), Hz	9000032.48	0.049999576263
Maximum f_x (max), Hz	9000038.73	0.049999652243
Sampling Range, f_x (max)- f_x (min), Hz	6.2515	7.6E-0008
Median	0	0
Arithmetic Mean, Hz	9000035.42	0.04999962
Variance	2.405	3.4E-0016
Standard Deviation	1.5508	1.8E-0008
Coefficient of Variation	5803428.66	2709716.49
Relative error, %	0.00039 < 0.00050	0.00009 < 0.0005

The absolute and relative errors for infralow frequency measurements (f_x=0.05 Hz) are shown in Figure 8 (a) and 8 (b) respectively. The χ^2 test for goodness of fit test was applied to investigate the significance of the differences between observed data in the histograms and the theoretical frequency distribution for data from the Gaussian distribution law. The number of equidistant classes was calculated according to the following equation [19]:

$$k = 1.9 \times \mathrm{N}^{0.4}, \qquad (4)$$

where *N* is the number of measurements.



a)

b)

Figure 8. Absolure error (a), and relative error at 0.05 Hz frequency measurements.

At probability P = 97 %, and 5 equidistant classes (k=5), the hypothesis of Gaussian distribution law can be accepted for all sets of measurement data because of $S < \chi^2_{max}$, where S = 1.7593 is the sum of deviations between the dataset and the assumed distribution; $S < \chi^2_{max} = 7$ is the maximum possible allowable deviation in the χ^2 distribution. Hence, the hypothesis of normal (Gaussian) distribution can be accepted.

Experimental results confirmed high metrological performances and justified, that the USTI IC can be used with all quasi-digital sensors existing on the modern market [6]. The comparative analyze of proposed solution for sensor nodes and convenient solution described in [4] is shown in Table II.

The comparative metrological and technical performance of proposed solution and wireless module T24-PA available on the market [5] are shown in Table III. As it is visible from this table the wireless sensor node based on the USTI IC has significantly better metrological performance. In addition, the USTI IC has much wider functionalities and can work not only with frequency and period output sensors but also with any duty-cycle, pulse-width modulated, phase-shift, time interval, pulse number output sensors and transducers.

The further reduction of power consumption will be able due to the use of advanced method for frequency-to-digital converter with non-redundant, programmable reference frequency [20]. It will allow to change accuracy for power consumption and opposite dependent on sensor node's activity, measuring algorithm and available power.

TABLE II. COMPARISON RESULTS OF SENSOR NODE DESIGNS.

No.	Traditional Solution [4]	Proposed Solution	Benefits
1.	Analog sensors	Quasi-digital sensors	More robust and cheaper; less sensitive to interferences and noises
2.	Analog multiplexor	Digital multiplexor	No addition error
3.	Analog and mixed IC design	Digital IC design	Easy integration in standard CMOS technological processes
4.	Low metrological performances	High metrological performances	Wide applications
5.	Need a frequency range unification	Does not need any frequncy range unification	Lower hardware expenses
6.	Classical direct counting method	Modified method of the dependent count	Constant programmable quantization error; Non-redundant conversion time; Broad range of input frequencies
7.	Adaptation features: no	Adaptation features: yes	Self-adaptation; wide applications

TABLE III. COMPARATIVE PERFORMANCES.

	T24-PA	USTI IC
Relative error, %	0.15 ... 0.25	0.0005
Frequency Range, Hz	0.5 ... 3 000	0.04 ... 9 000 000
Time range, s	333E-06 ... 2	1.5E-06 ... 250
RPM range (presuming 1 pulse / rev), rpm	30 ... 180 000	3 ... unlimited
Power Supply Current, mA	35	9.5

V. CONCLUSIONS

The proposed sensor node architectures and design approach are suitable for any quasi-digital sensors and transducers. It is based on the designed USTI IC, which lets to achieve high metrological performances at relatively low cost, and get robust solution, less sensitive for various interferences, noises and distortions. Due to the USTI's broad frequency range of input signals and constant quantization error, it is not necessary to convert the different sensor output ranges into the same frequency range. The proposed sensor node architectures can also work with analog sensors. In this case the output voltage must be preliminary converted to the frequency with the help of voltage-to-frequency converter. In addition, the advanced, modified method of the dependent count for frequency measurements provides the best tradeoff between accuracy and operation time, giving a relative error less than ±0.0005 % at 0.32 s conversion time or ±1 % at 0.00016 s conversion time respectively.

The USTI IC is available on the market since 2011 from the Technology Assistance BCNA 2010 S. L., Spain. The USTI-WSN IC will be introduced on the market in 2013-2014.

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