# A 26μW, Two-stage VCO and Mixer for Direct DPSK Conversion in MedRadio

Ilya Chigrev and Predrag Spasojevic
Winlab/ECE Department
Rutgers University
Piscataway, NJ 08854, USA
e-mail: spasojev@winlab.rutgers.edu

Jeffrey S. Walling
PERFIC Lab/ECE Department
University of Utah
Salt Lake City, UT 84112, USA
e-mail: jeffrey.s.walling@utah.edu

***Abstract*—A 26μW voltage controlled oscillator (VCO) and mixer have been designed in an 130nm RF CMOS process for a direct conversion DPSK demodulator in the MedRadio frequency band (401-406MHz). The circuit utilizes a two-stage (VCO) design directly coupled to a passive ring mixer. With biasing circuits it requires an active die area of 49×39 um. The circuit is designed to operate from a 1 V supply and achieves a post-extracted simulated phase noise of -118dBc/Hz when injection locked. With the passive mixer, conversion gain is -18.4dB.**

***Index Terms*—Low Power CMOS; MedRadio; Passive Mixer; Ring Oscillator; Vance Demodulator**

## I. INTRODUCTION

There is a growing need for low power radio frequency (RF) technology for medical implant devices. The original Medical Implant Communication Services (MICS) band has been expanded in recent years to the new MedRadio band, increasing the available spectrum to 401-406 MHz [1].

Current technologies for low power radio consume an order of magnitude more power than is acceptable for implantable operation. Proposed in this paper is a two-stage (VCO) and mixer configured as a Vance demodulator [2]. The design is intended for use in a direct conversion, differential phase-shift keying (DPSK) receiver front-end for a MedRadio transceiver. The circuit has been designed to operate with minimal power consumption in moderate inversion while maintaining performance and reliability.

The design and implementation of the circuit are discussed in detail in Section II, including information on design methodologies for low power design in deeply scaled CMOS processes. In Section III simulated, post-extracted design results will be discussed. Finally, conclusions and future directions will be discussed in Section IV.

## II. CIRCUIT DESIGN

In order to reduce power consumption a two-stage VCO was designed using the Maneatis delay-cell, which uses positive feedback to reduce the required transconductance to achieve oscillation [3]. This VCO is designed to be directly coupled to a passive ring mixer; the loading from the mixer is accounted for in the delay calculation. By injection locking the ring oscillator to the incoming signal, the quadrature output of the oscillator represents a delayed version of the incoming signal. The input signal is mixed with this delayed replica to form a Vance demodulator, which can directly downconvert and demodulate DPSK signals [2]. The block diagram (Fig. 1) for the proposed receiver front-end represents a minimal set of circuitry needed to demodulate such DPSK signals. Though not included, the literature contains microwatt LNA [4]. Details of the oscillator and mixer designs follow.

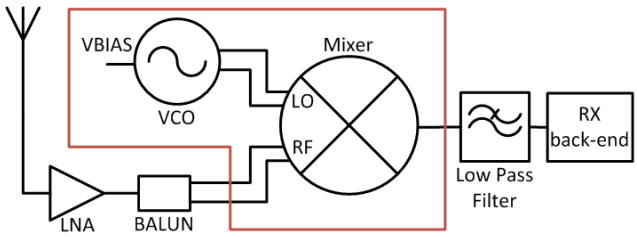


Fig. 1. Block diagram of the system. The outlined area represents the design for this work.

### A. Voltage Controlled Oscillator Design

The Maneatis delay cell based VCO topology is shown in Fig. 2. The delay cell uses positive feedback to reduce the parasitic conductance at the output of the cell, reducing the required transconductance required for startup. The oscillation frequency is given by the following equation [5]:

$$f_{osc} = \frac{1}{2\pi} \cdot \frac{G_m}{C_{tot}} \quad (1)$$

where $C_{tot}$ is the total capacitance and $G_m$ is the total transconductance at the drain of the delay cell. Examining the half-circuit of the schematic yields the following expression for $G_m$:

$$G_m = \sqrt{g_{m_{M3}}^2 - \left(g_{m_{M1}} - g_{m_{M2}} + g_{ds_{M1}} + g_{ds_{M2}} + g_{ds_{M3}}\right)^2} \quad (2)$$

The negative transconductance terms result from the cross-coupled transistors, $M_{2,5}$, in parallel with the active load transistors, $M_{1,4}$. The conductance can be cancelled for a given bias and transistor size, reducing the expression for frequency of oscillation to the following:

$$f_{osc} = \frac{1}{2\pi} \cdot \frac{g_{m_{M3}}}{C_{tot}} \quad (3)$$

By exploiting this reduced formula the entire VCO can be implemented using two differential Maneatis delay-cells connected in quadrature with no external passive components, reducing the size and complexity of the VCO. Because the

 ISBN: 978-1-61208-433-6 

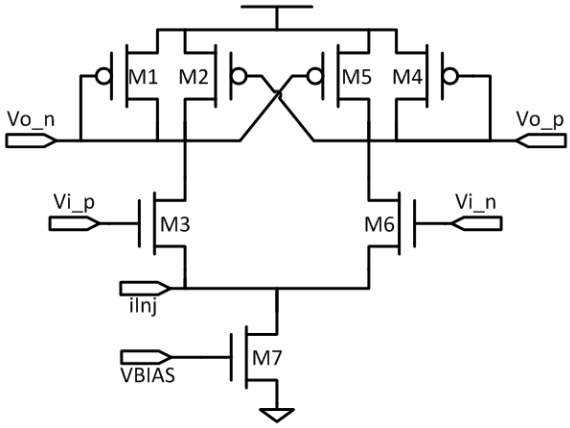


Fig. 3. Maneatis delay-cell schematic.

oscillator utilizes only active components with small feature sizes, the oscillator occupies little die area. Due to the quadrature connection, each of the two cells contributes a 90° phase shift, with the final 180° phase shift necessary for oscillation contributed by a cross-coupled connection from the output of the oscillator back to the input.

Wideband frequency control of the VCO can be achieved by controlling either the bias current or supply voltage, with the former preferred. This allows the oscillator to operate over a relatively large tuning range, allowing for guaranteed functionality while operating in the low power moderate inversion region. This region of operation is more susceptible to PVT variations; hence a wide tuning range allows for more robust operation. The first tuning method is to vary the bias current by changing the voltage at the gate of the current source, $M_7$. This is used to adjust the free running frequency of the oscillator in implementation, allowing it to be more easily injection locked to the incoming signal. This can be adjusted via an on-chip generated control voltage, or more likely, by segmenting and digitally controlling a current mirror to

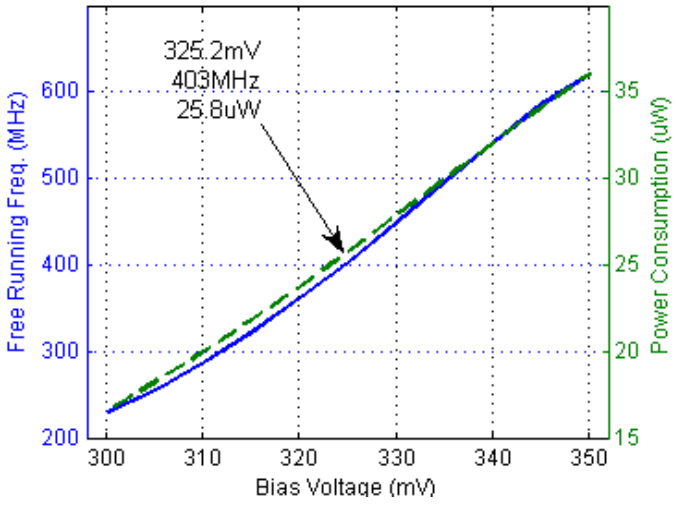


Fig. 4. VCO free running tuning range (solid line) and power consumption (dashed line) as a function of the biasing voltage.

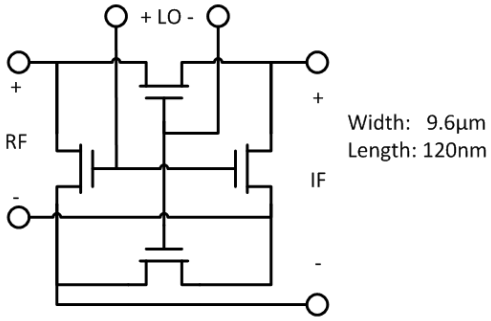


Fig. 2. Passive ring mixer schematic.

increase/decrease bias current as needed. Using this tuning method, the oscillation frequency changes nearly linear with the applied change in the input current; this is consistent with theory as the transconductance varies linearly with the bias current for a given overdrive voltage (e.g., $g_m = 2I_D/V_{ov}$). The free running frequency of the oscillator and VCO power consumption is plotted versus input bias voltage is shown in Fig. 3.

As can be seen in Fig. 3, this design allows for a wide range of tunability, covering the entirety of the MedRadio frequencies and allowing for correction due to PVT variation.

The cell can be injection locked by inserting a frequency-dependent current into the *Iinj* port (Fig. 2). Simulations have validated functionality for injection signals as small as 1µA across process corners.

Injection locking is important in this application as it is necessary to create the delayed version of the signal needed for demodulation; it also reduces oscillator phase noise compared to its free-running state.

### *B. Passive Mixer*

To minimize power consumption in the receiver chain, a passive ring mixer has been selected. The passive ring (Fig. 4) is implemented using NMOS transistors to allow for the best tradeoff between size and switching resistance.

The mixer consists of a set of alternating switches that are selectively opened and closed by the injected signal and delayed replica, multiplying the two signals. The output of a low noise amplifier (LNA) can be used as the injection signal for the oscillator, which drives one branch of the mixer, while the LNA can drive the other branch. DPSK information is then demodulated in the following manner. The input signal is phase modulated, so the mixer will produce a high- (low-) output when the phase of the input signal leads (lags) the delayed replica.

In choosing the passive mixer, a tradeoff was made between gain and power consumption. For applications where more gain is necessary, an active mixer can be employed consuming similar power to the VCO delay cells.

### *C. Design Methods*

The circuit elements for both the VCO and the mixer were determined using the $g_m/I_D$ methodology, allowing for sizing of transistors using pre-derived look-up tables of geometry independent properties. This method produces more accurate

 ISBN: 978-1-61208-433-6

first-pass device sizes than square-law hand calculations [6]. This is because standard hand calculations do not take into account short-channel effects that start to become dominant in deep-submicron CMOS. The script is flexible enough to accommodate the addition of multiple stages and their associated loading effects, which is important for ultra-low power design.

A MATLAB script was written to automatically size the VCO and the mixer, taking into account the mixers loading effect on the VCO. A lookup table, generated using DC simulations of the BSIM4 device models, was generated using OCEAN scripting. The table contents are geometry independent parameters (e.g., current density, $I_D/W$ ; transconductance efficiency, $g_m/I_D$ , etc.). The script uses desired properties of the delay cell (e.g., total power consumption, desired oscillation frequency, and the desired operating points of the transistors in both the mixer and VCO) to lookup information in the tables to satisfy such conditions. For optimal power efficiency the $g_m/I_D$ values of the VCO were chosen in a region of moderate inversion, 23 $V^{-1}$, where decreasing the $g_m/I_D$ value results in increasingly strong inversion.

In addition to transconductance, the device capacitance per unit width was also found according to the desired power characteristics. Layout capacitance was estimated based on the cell size and the cell geometries were iterated in the script until a satisfactory solution was achieved that optimized the design for low power at the desired operating frequency. The final devices obtained from the script are shown in Table I.

## III. RESULTS

The VCO and mixer pair has been designed and extracted using an 8 metal, RF CMOS technology. The chip layout is shown in Fig. 5. The design is compact and is dominated by biasing and decoupling circuitry, occupying a die size of 49×39µm, not including bonding pads.

This design has been extracted and simulated at 37°C because the intended use is for a medical implant. The simulated results of the circuit show that the overall design consumes 25.8µA when the supply voltage is 1V, at typical operating conditions. The circuit has also been tested in fast and slow fabrication corners. Simple adjustment of the biasing current and supply voltage has been shown to allow the design to operate across expected PVT variations.

The VCO achieves a free running oscillation frequency of 403.5MHz at a typical process corner, with and associated phase noise of -51.8bBc/Hz. When the VCO is under injection lock conditions the phase noise improves to -118dBc/Hz, using an ideal injection lock signal. The free running and injection locked VCO phase noise characteristics are shown in Fig. 6.

Table I. LIST OF DEVICE SIZES FOR VCO

| Device | Width (µm) | Length (nm) |
|---|---|---|
| M1,4 | 0.6 | 240 |
| M2,5 | 0.96 | 240 |
| M3,6 | 2.13 | 120 |
| M7 | 2.6 | 360 |

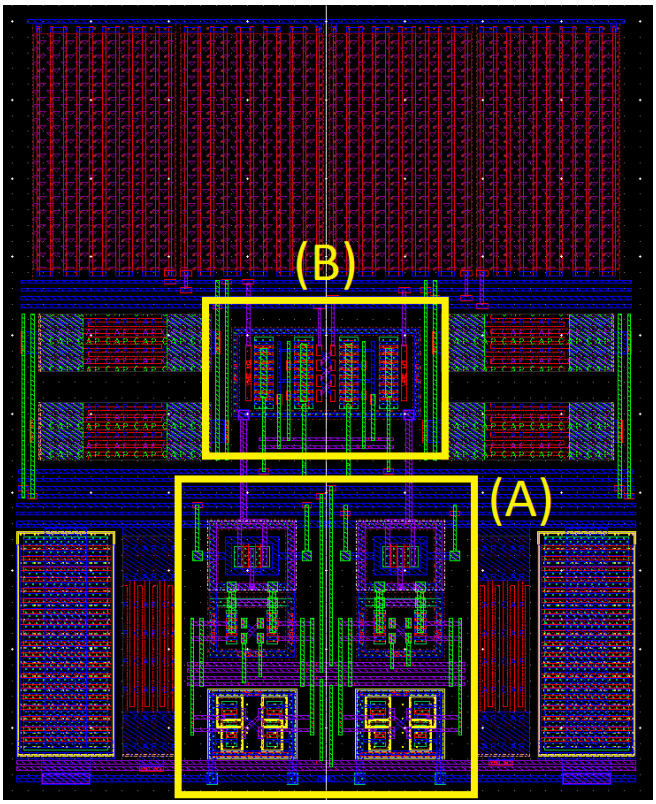


Fig. 5. The layout for the (A) VCO and (B) mixer. The surrounding area contains bias, bypass, and coupling circuits. The figure dimensions are 49×39µm.

The passive mixer achieved an overall voltage conversion gain of -18.4dB and 1 dB compression point of -13.5dBm, as shown in Fig. 7. This conversion gain is far below the theoretical limit (~ -4 dB) obtained when square wave drive signals are used. Such a signal would result in a significant power consumption increase in the VCO. Hence a tradeoff was made between power consumption and conversion gain. The effects of this tradeoff can be mitigated by using a high-gain LNA, or by using an active mixer.

Post-extracted simulations have demonstrated that this system is capable of demodulating a PSK signal. MATLAB is used to generate a piecewise linear voltage signal carrying the DPSK at the desired injection locking frequency. The signal is used as the injection locking frequency for the oscillator and to drive the RF port of the designed mixer. Representative input/output waveforms are shown in Fig. 8.

To compare this work with other low power VCOs, a figure of merit (FOM) by which different VCO designs can be compared and captures the two most critical design criteria, power consumption and the phase noise (NF) is calculated:

$$FOM = 10\log\left[\left(\frac{F_{osc}}{F_m}\right)^2 \frac{1}{P}\right] - L\{F_m\} \qquad (4)$$

where $F_{osc}$ and $F_m$ are the oscillation frequency and offset frequency, respectively, $P$ is power consumed, in mW, and $L$ is the phase noise at the offset frequency, in dBc/Hz [7]. It should be noted that DC offset correction has not been considered in

 ISBN: 978-1-61208-433-6 

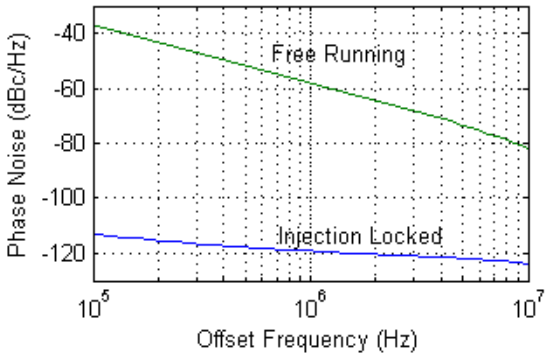


Fig. 6. VCO phase noise characteristic.

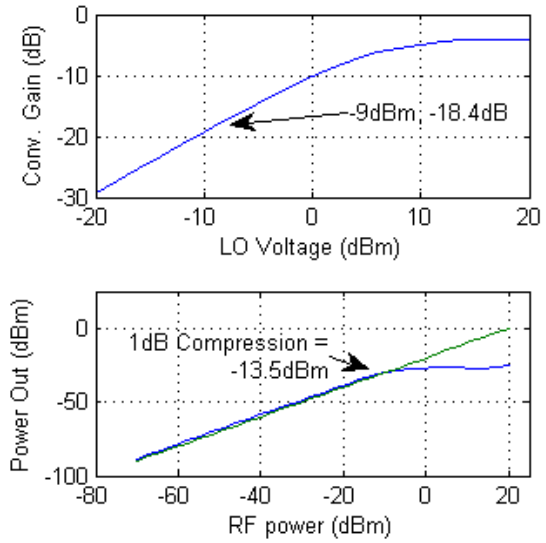


Fig. 7. Simulated mixer conversion gain as a function of VCO input power (top), and 1dB compression point (bottom).

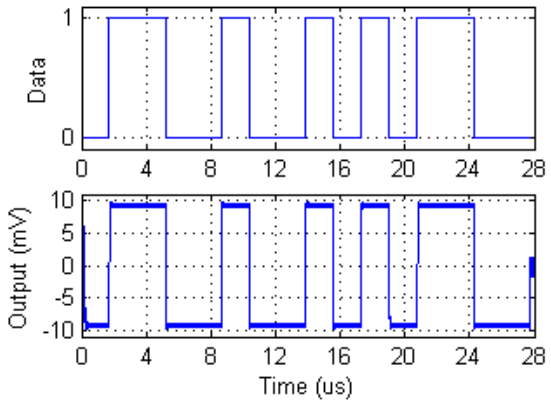


Fig. 8. Simulated mixer output with the injection-locked VCO.

this work, but prior methods are applicable for this circuit [8], [9].

As can be seen in Table II, this design exhibits a good phase noise while operating at a low power point. The work outlined in [7] has been include as a comparison point as the design outlined in it also uses a two-stage Maneatis cell VCO, while the other papers utilize other delay cells.

Table II. FIGURE OF MERIT COMPARISON

| | Frequency (MHz) | Phase Noise (dBc/Hz) | Freq. Offset (MHz) | Power (mW) | FOM (dBc/Hz) |
|---|---|---|---|---|---|
| **This Work[(1)]** | **403.5** | **-51.8** | **1** | **0.0258** | **119.8** |
| **This Work[(2)]** | **403.5** | **-118.9** | **1** | **0.0258** | **186.9** |
| [7][(1)] | **5650** | **-88.4** | **1** | **5** | **156.5** |
| [7] [(2)] | **5650** | **-121.7** | **10** | **5** | **169.8** |
| [10] | **403.5** | **-95.6** | **1** | **0.85** | **148.4** |
| [11] | **403.5** | **-107** | **0.1** | **1.2** | **178.3** |

[(1)]- Free running oscillation, [(2)]- Injection locked oscillation

## IV. FUTURE WORK & CONCLUSION

A low power VCO and mixer pair is implemented in this paper. The two-stage VCO, based on a Maneatis delay cell, has a phase noise of -118dBc/Hz at 1MHz offset when injection locked, and requires no external passive components. The passive ring mixer has a conversion gain of -18.4dB. The VCO and mixer configuration is used as a Vance demodulator designed for the MedRadio frequency band. Targeted for low power applications, the design consumes 26µW of power from a 1V supply. Future work will expand this design with the integration of an LNA and receiver back-end and examine effects of DC offset and compensation techniques.

## REFERENCES

[1] P. D. Bradley, "Wireless medical implant technology — Recent advances and future developments," in *Proceedings of ESSCIRC*, 2011, pp. 37–41.

[2] I. A. W. Vance, "An integrated circuit v . h . f . radio receiver," *Radio Electron. Eng.*, vol. 50, pp. 158–164, Apr. 1980.

[3] J. G. Maneatis and M. A. Horowitz, "Precise delay generation using coupled oscillators," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1273–1282, Dec. 1993.

[4] H. K. Cha, M. K. Raja, X. Yuan, and M. Je, "A CMOS MedRadio receiver RF front-end with a complementary current-reuse LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 59, pp. 1846–1854, Jul. 2011.

[5] C. Li and J. Lin, "A 1-9 GHz linear-wide-tuning-range quadrature ring oscillator in 130 nm CMOS for non-contact vital sign radar application," *IEEE Microw. Wirel. Components Lett.*, vol. 20, pp. 34–36, Jan. 2010.

[6] F. Silveira, D. Flandre, and P. G. a Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1314–1319, Sep. 1996.

[7] B. Fahs, W. Y. Ali-Ahmad, and P. Gamand, "A Two-Stage Ring Oscillator in 0.13-um CMOS for UWB Impulse Radio," *IEEE Trans. Microw. Theory Tech.*, vol. 57, pp. 1074–1082, May 2009.

[8] B. Lindoff, "Using a direct conversion receiver in EDGE terminals-a new DC offset compensation algorithm," in *Proceedings of the IEEE PIMRC*, 2000, pp. 959–963.

[9] H.-J. Song, J.-Y. Kim, K. Ajito, N. Kukutsu, and M. Yaita, "50-Gb/s Direct Conversion QPSK Modulator and Demodulator MMICs for Terahertz Communications at 300 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 62, pp. 600–609, Mar. 2014.

[10] L.-C. Liu, M.-H. Ho, and C.-Y. Wu, "A medradio-band low-energy-per-bit CMOS OOK transceiver for implantable medical devices," in *Proc. of the IEEE BioCAS*, 2011, pp. 153–156.

[11] K. W. Li, L. L. K. Leung, and K. N. Leung, "Low power injection locked oscillators for MICS standard," in *Proc. of the IEEE BioCAS*, 2009, pp. 1–4.

 ISBN: 978-1-61208-433-6 