Two-stage Wideband Class-E Power Amplifier in a 130 nm CMOS Process

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***Abstract*—A wideband switching-mode power amplifier (SMPA) provides an optimum solution to cover multiple wireless standards with high efficiency and a high level of integration in a low-cost CMOS process. In this paper, a single-ended two-stage PA operating at 2.5 GHz in 130 nm CMOS technology is presented. The main-stage comprises a class-E PA based on finite DC-feed inductance, which provides high output resistance and can, therefore, cover a wide frequency range. A class-E driver with interstage matching is used to drive the main-stage PA in order to obtain large overall power gain with an optimum PA performance. The main and the driver stages are operated at 3.3 V and 1.3 V, respectively. Simulations indicate that the PA provides peak output power of 23.0 dBm and peak power added efficiency (PAE) of 64.0 %. From 2.15 GHz to 3.1 GHz, an output power of more than 20.5 dBm with a gain of 16.5 dB and PAE of more than 50.0 % are simulated.**

***Index Terms*—Wideband, class-E, load transformation network (LTN), switching-mode power amplifier (SMPA), power added efficiency (PAE).**

I. INTRODUCTION

The upcoming wireless technology is in motion to provide high data rate with wider coverage capabilities. From mobile equipment manufacturers perspective, this development brings several challenges since these advancements are linked to high power dissipation and high costs of the mobiles. Hence, it demands the design of high performance circuits with high efficiency to increase the battery life in a low cost CMOS process. The power amplifier (PA) is one of the most critical components of the RF front-end as it is the most power hungry element and defines the overall efficiency of a transceiver. Improving PA efficiency significantly impacts battery life and thus a comprehensive effort is being made to implement highly efficient CMOS PAs [1].

Switching-mode power amplifiers (SMPAs) are nonlinear class of PAs and have the capability to obtain high efficiency, ideally 100 % at RF and microwave frequencies. The active device is used as an ON/OFF switch such that for any time instant, a nonoverlapping voltage and current exist at the device output. Each class of SMPA, namely class-D [2], E [3], F [4] and F^{-1} [5] requires specific harmonic impedance termination at the output of the active device in order to prevent power dissipation. This eventually limits the operational bandwidth of a SMPA.

Introduction of next generation wireless communication standards increases the demand on both mobile equipments and base stations. A mobile terminal is required to cover the existing and also the upcoming standards to reduce the form factor and fabrication cost with minimum hardware effort. Several approaches for multiple band coverage have been proposed in literature. One solution is a multiband multiharmonic LTN using transmission-lines and/or multiple tuned LC circuits [6]- [7]. But, these are not feasible for mobile terminals due to their huge chip area requirements and the high associated cost.

The broadband design seems to be the most suitable approach to cover multiple bands which employs one active device as a switch and a wideband LTN [8]. It does not require any tuning element which results in an area efficient LTN and the PA can be fully integrated on-chip with a reasonable amount of die area.

A class-E PA based on finite DC-feed inductance instead of a conventional RF choke (RFC) provides wider bandwidth because it offers a higher optimum resistance, R_E, for the same output power and supply voltage [9]. In this paper, a two stage class-E PA using finite DC-feed inductance in 130 nm CMOS technology is presented. The main-stage is driven with a class-E PA to enhance the overall gain and PA efficiency. In simulation, the circuit provides 23.0 dBm peak output power with 64.0 % peak PAE. For a frequency range from 2.15 GHz to 3.1 GHz, the amplifier delivers an output power of 20.5 dBm and PAE of more than 50.0 %.

II. CLASS-E POWER AMPLIFIER

The class-E PA exploits the soft-switching property to provide high efficiency at high frequencies. It incorporates the drain-source capacitance, C_{DS} of the transistor in the LTN to eliminate the power losses associated with its discharging over the transistor in every RF cycle. This results in zero-voltage switching (ZVS) and zero-derivative switching (ZDS) which means at device turn on, there is no capacitor charge and no capacitor current at the device output [3].

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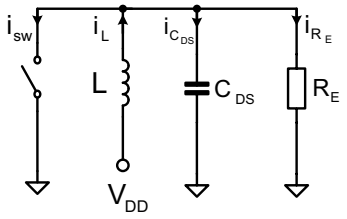

Fig. 1. Equivalent circuit of a class-E PA based on finite DC-feed inductance.

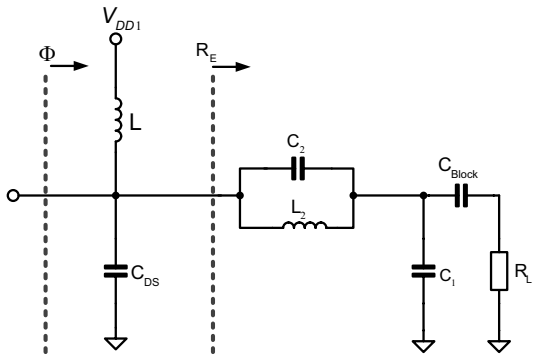

Fig. 2. Class-E LTN based on a finite DC-feed inductance and using the optimised second harmonic impedance termination network.

A. Load transformation network based on finite DC-feed inductance

The equivalent circuit of a class-E LTN using finite DC-feed inductance is shown in Fig. 1. The ZVS and ZDS conditions can be fulfilled by using only the LC_{DS} tank, whose resonant frequency is 1.41 times the operating frequency, f_0. The operation principle along with the equations for R_E, L and C_{DS} for a given output power, P_{out}, are detailed in [9]. The load phase angle, Φ, at the device drain at f_0 is given by:

$$\Phi = tan^{-1}\left(\frac{R_E}{\omega_0 L} - \omega_0 R_E C_{DS}\right) = 34.24^o\,, \qquad (1)$$

where impedances at all other harmonic frequencies are assumed to be capacitive. The LC_{DS} tank gives the accurate load angle and, thus, one can obtain the nominal class-E output waveforms at the transistor output. Since there is no imaginary part in the LTN as compared to the typical class-E conditions with an RFC, the optimum impedance can be written as:

$$Z_E(nf_0) = \begin{cases} R_E\,(1+j0)\,, & \text{if } n = 1 \\ \infty, & \text{if } n = 2, 3, .. \end{cases} \qquad (2)$$

A class-E PA using finite DC-feed inductance results in a relatively high R_E, which relaxes the impedance transformation ratio at f_0 and, therefore, also allows wider bandwidth. Secondly, the finite DC-feed inductor has a high self-resonance frequency (f_{SR}), which permits the designer to implement PAs for high frequency applications. In addition, the inductors can be integrated on-chip and, therefore, the total cost of the PA may be reduced.

B. Optimised second harmonic load circuit

The influence of harmonic termination on amplifier efficiency decrease with increasing order, whereas, second harmonic theoretically has the highest impact on efficiency. In order to filter out the second harmonic content, the parallel tank, L_2C_2, resonating at $2f_0$ is added to the circuit in Fig. 1. This leads to an optimised second harmonic load circuit for a class-E PA [10], as shown in Fig. 2.

The parallel tank L_2C_2 is inductive at f_0 and can be sized using LC_{DS} in combination with C_1 to get the nominal class-E conditions at f_0. As L_2C_2 resonates at $2f_0$, the value of L_2 is smaller than the series inductance used in a conventional class-E LTN. This is not only good for integration but it also extends the frequency range of the LTN. The values for the optimised second harmonic load circuit, illustrated in Fig. 2, are given by the expressions [10]:

$$C_1 = \frac{1}{2\pi f_0 R_L}\sqrt{\frac{R_L}{R_E} - 1}\,, \qquad (3)$$

$$L_2 = \frac{3R_E}{8\pi f_0}\sqrt{\frac{R_L}{R_E} - 1}\,, \qquad (4)$$

$$C_2 = \frac{1}{4(2\pi f_0)^2 L_2}\,, \qquad (5)$$

where R_L is the $50\,\Omega$ load.

III. Design and Implementation

Using the concept discussed in Section II, a two-stage class-E PA was implemented. The design starts with a class-E PA as a main-stage amplifier followed by a class-E driver and an interstage matching network.

A. Main-stage class-E PA

A class-E LTN with finite DC-feed inductance was designed using Fig. 2 for an output power, P_{out} = 0.7 W at 2.5 GHz. The transistor was biased at V_{DD_1} = 3.3 V and V_{GS_1} = 400 mV. This leads to an R_E of $21.5\,\Omega$, L of 0.93 nH and C_{DS} of 2.17 pF. The transistor was scaled to 2.3 mm for this design. The output capacitance of this transistor is smaller than the desired value, therefore, an external capacitance is added to provide nominal class-E conditions.

The fundamental impedance at the transistor drain is simulated to be $(27.0 + \mathrm{j}\,14.5)\,\Omega$, which corresponds to a load angle, $\Phi = tan^{-1}(\frac{14.5}{27.0}) \approx 28.2^o$, while other harmonics are capacitive. The achieved impedances at the fundamental and harmonic frequencies are in good comparison with the class-E switching conditions as depicted in Fig. 3.

Peak PAE of 64.8 % and peak output power of 23.6 dBm are simulated as shown in Fig. 4. The second and third harmonic frequencies are suppressed by 26.8 dBc and 36.6 dBc, respectively. Fig. 5 illustrates the simulated time-domain voltage and current waveforms at the device output, which approximate ideal class-E characteristics. In Fig. 6, amplifier performance

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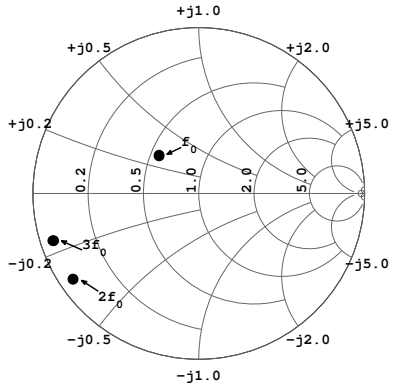

Fig. 3. Simulated output impedance of the designed class-E LTN based on finite DC-feed inductance.

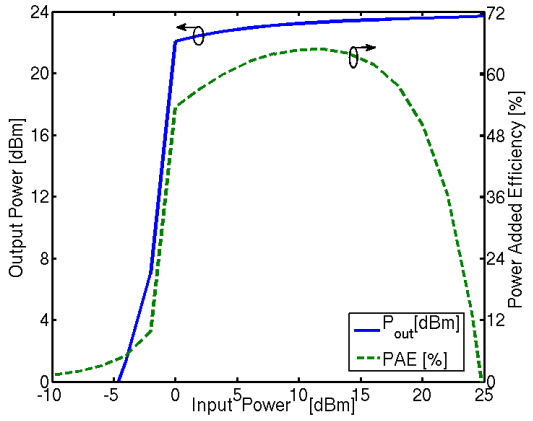

Fig. 4. Simulated output power and PAE of the designed class-E PA with finite DC-feed inductance.

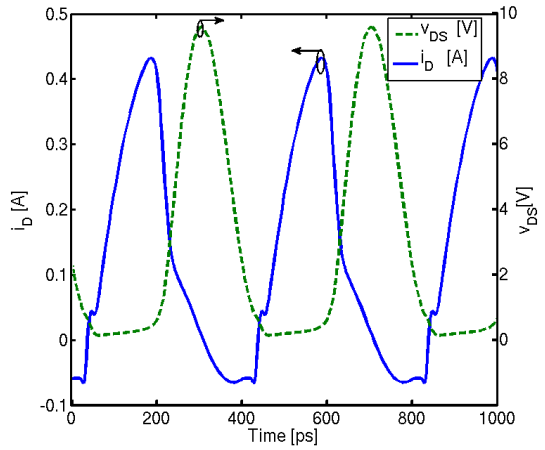

Fig. 5. Simulated time-domain current and voltage waveforms at the transistor's output of the class-E PA with finite DC-feed inductance.

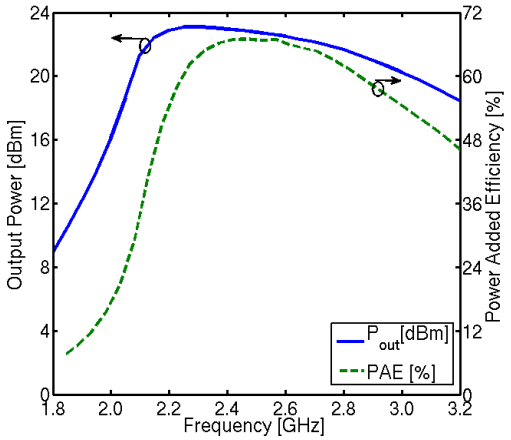

Fig. 6. Simulated output power and PAE versus frequency of the designed class-E PA with finite DC-feed inductance at P_{in} = 11 dBm.

against input frequency is highlighted. The main-stage PA attains more than 50.0 % PAE, more than 19 dBm of output power with an associated power gain greater than 8.0 dB from 2.15 GHz to 3.15 GHz.

B. Class-E driver stage

The driver stage consists of a class-E amplifier with an interstage matching network cascaded to the previously designed main-stage amplifier, as shown in Fig. 7. The class-E driver fulfills the class-E conditions as the tank L_3C_3 is tuned to $1.41f_0$. Secondly, the gate-source capacitance, C_{GS}, of the main-stage transistor is resonated out with L_4 at $2f_0$. It results in an approximately half-sinusoidal voltage waveform to operate the main transistor as a switch. Due to this, the PA operates only in the active region and the large negative swing of the input voltage is eliminated. Fig. 8 shows the simulated time-domain voltage waveforms at the output and input of the main transistor and also at the output of the class-E driver.

Simulated PAE and output power of the two-stage class-E PA are shown in Fig. 9. Peak PAE of 64 % and peak output power of approximately 23.0 dBm is obtained. One can clearly see that due to the driver and inter stage matching network, the amplifier performance is basically unchanged over a wide range of input powers. Fig. 10 illustrates the PA performance against input frequency. The designed amplifier provides PAE greater than 50 %, output power of more than 20.5 dBm and a power gain of more than 16.5 dB over a relative bandwidth of more than 36.2 %, i.e. from 2.15 GHz - 3.1 GHz.

Simulated performance of the SMPA is summarised in Table I. Following figure-of-merits (FOMs) are used to compare the performance of designed amplifier with other published two-stage CMOS SMPA designs:

$$FOM_1 = PAE \cdot Freq\ [\text{Hz}]^{0.25} P_{out}\,, \tag{6}$$

$$FOM_2 = PAE \cdot Freq\ [\text{Hz}]^{0.25} BW\,, \tag{7}$$

where BW is the relative bandwidth. In [12], inductors have large values which consume significant chip area. For this work, all the biasing inductors can be realised by bond wires, whereas an on-chip inductor, L_2 = 1.18 nH. Hence, the implemented two-stage amplifier has an area-efficient design.

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TABLE I
PERFORMANCE COMPARISON OF THE PRESENTED DESIGN WITH OTHER TWO-STAGE CMOS SMPAS

Ref.	Tech. [nm]	V_{DD1} [V]	V_{DD2} [V]	Freq. [GHz]	Max Output [dBm]	Max PAE [%]	-3 % PAE, BW [GHz]	FOM_1	FOM_2
[11]*	180	2.0	-	1.9	16.3	70.0	1.87 - 1.96 (4.7 %)	6.28	6.87
[12]	180	2.5	1.8	2.4	23.0	73.0	2.22 - 2.57 (14.6 %)	32.3	23.6
This work	130	3.3	1.3	2.5	23.0	64.0	2.34 - 2.84 (19.3 %)	28.6	27.6

* Measurement

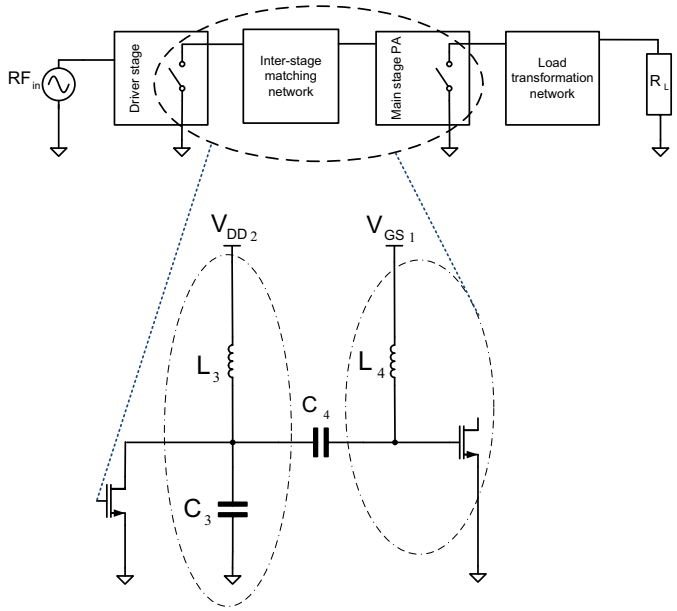

Fig. 7. Driver and interstage matching network for a two-stage class-E PA based on finite DC-feed inductance.

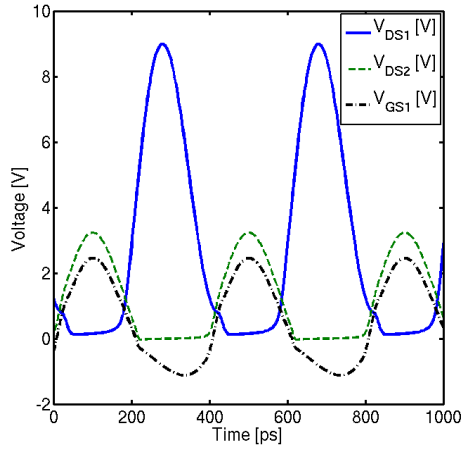

Fig. 8. Simulated time-domain voltage waveforms at the output and input of main-stage transistor and at the output of class-E driver.

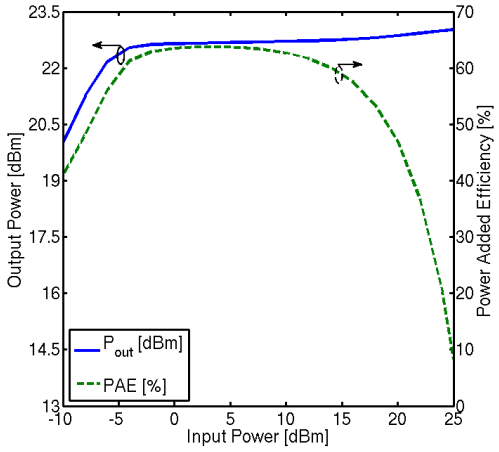

Fig. 9. Simulated output power and PAE of the designed two-stage class-E PA with finite DC-feed inductance.

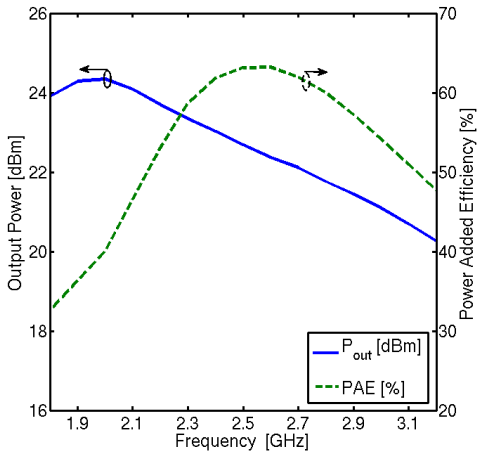

Fig. 10. Simulated output power and PAE versus frequency of the designed two-stage class-E PA with finite DC-feed inductance at P_{in} = 4 dBm.

IV. CONCLUSION

An efficient and wideband two-stage class-E PA in CMOS 130 nm process has been designed. The main-stage amplifier is based on class-E load network using finite DC-feed inductance. This approach leads to high optimum resistance, which facilitates wideband operation. Secondly, the use of finite DC-feed inductance has less resistive losses, high f_{SR} and, therefore, high efficiency. A class-E driver also using finite DC-feed inductance with interstage matching feeds the

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main-stage class-E PA with a waveform approaching a half sinusoidal voltage. The benefit of the circuit is an improvement in the overall PA performance since there is no negative voltage swing.

Simulation results show that the amplifier can deliver 23.0 dBm peak output power at peak PAE of 64.0 % to a 50 Ω load at 2.5 GHz from 3.3 V supply. The two-stage PA obtains an optimum wideband performance with output power and PAE more than 20.5 dBm and 50.0 %, respectively, for a power gain greater than 16.5 dB, within a frequency range from 2.15 GHz to 3.1 GHz. The mentioned bandwidth covers WLAN, Bluetooth and LTE applications.

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REFERENCES

[1] Y. Ding and R. Harjani "A high-efficiency CMOS +22-dBm linear power amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1895-1900, Sep. 2005.

[2] T. Nakatani, J. Rode, D. F. Kimball, L. E. Larson and P. M. Asbeck, "Digital polar transmitter using a watt-class current-mode class-D CMOS power amplifier," *IEEE J. Radio Frequency Integrated Circuits Symp.*, pp. 1-4, 2011.

[3] N. O. Sokal and A. D. Sokal, "Class E - A new class of high efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, pp. 168-176, Jun. 1975.

[4] F. H. Raab, "Maximum efficiency and output of class-F Power amplifier." *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1162-1166, Jun. 2001.

[5] Y. Y. Woo, Y. Yang and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 1969-1974, May 2006.

[6] D. Kalim and R. Negra, "Concurrent planar multiharmonic dual-band load coupling network for switching-mode power amplifiers," *Proc. IEEE MTT-S Int. Microw. Symp.*, pp. 1-4, Jun. 2011.

[7] R. Negra, A. Sadeve, S. Bensmida, F. M. Ghannouchi, "Concurrent Dual-band Class-F Load Coupling Network for Applications at 1.7 and 2.14 GHz," *IEEE Trans. on Circuits and Systems-II*, vol. 55, no. 3, pp. 259-263, Mar. 2008.

[8] A. Mazzanti, L. Larcher, R. Brama and F. Svelto, "A 1.4 GHz-2 GHz wideband CMOS class-E power amplifier delivering 23 dBm peak with 67 % PAE," *IEEE J. Radio Frequency Integrated Circuits Symp.*, pp. 425-428, 2005.

[9] A. V. Grebennikov and H. Jaeger, "Class-E with parallel circuit-A new challenge for high-efficiency RF and microwave power amplifiers," *IEEE MTT-S Dig.*, pp. 1627-1630, 2002.

[10] R. Negra and W. Bächtold, "Lumped-element load-network design for class-E power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, pp. 2684-2690, Jun. 2006.

[11] C. -C. Ho, C. -W. Kuo, C. -C. Hsiao and Y. -J. Chan, "A fully integrated class-E CMOS power amplifier with class-F driver stage ," *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, pp. 211-214, Jun. 2003.

[12] T. Wang, "Optimised class-E RF power amplifier design in bulk CMOS," *MSc.Thesis*, University of Texas, Arlington, Dec. 2007.

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