Assessment of High-Frequency Peformance Potential of Graphene Field-Effect Transistors

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***Abstract*—We assess high frequency performance potential of graphene field-effect transistors (FETs) down to a channel length of 10nm by using self-consistent ballistic and dissipative quantum transport simulations. The results indicate that with a thin high-κ gate insulator, the intrinsic ballistic cut off frequency f_T is above 5THz at a gate length of 10nm. Inelastic phonon scattering in graphene FETs lowers both f_T and the unitary power gain frequency f_{MAX}, mostly due to decrease of the transconductance. f_{MAX} and f_T are severely degrading in presence of source and drain contact resistance. To achieve optimum extrinsic f_{MAX} performance, careful choice of DC bias point in quasi-saturation regime and gate width is needed. Modeling of dissipative quantum transport is based on implementation of parallel simulation algorithms for the self-consistent Born approximation in the non-equilibrium Green's function (NEGF) formalism.**

Keywords-graphene transistors, RF performance, quantum transport simualtion

I. INTRODUCTION

Extraordinary electronic transport properties like high mobility and high saturation velocity make graphene attractive for radio frequency (RF) electronics applications [1]. Although the zero bandgap of 2D graphene leads to a low on-off ratio not desired for digital electronics applications, RF electronics applications do not require a large on-off ratio. Scaling down the channel length plays a critically important role for boosting the RF performance of a field-effect transistor (FET), and aggressive channel length scaling of graphene FET has been experimentally pursued. Recent experiments have demonstrated graphene transistors with intrinsic cut-off frequency projected to be at the hundreds of GHz range at sub 100nm channel scale [2-3]. The issues of the ultimate channel scaling, role of inelastic phonon scattering and performance potential of the unitary power gain frequency of graphene RF transistors, however, remain unclear.

II. APPROACH

Graphene FETs were simulated by solving the quantum transport equation using the non-equilibrium Green's function (NEGF) formalism with the Dirac Hamilton, self-consistently with a two-dimensional Poisson equation. Quasi-static approximations are used to assess its high-frequency performance [4]. Dissipative quantum transport due to inelastic phonon scattering, such as scattering due to polar optical phonons of the gate insulator and the intrinsic optical phonon of graphene, is modeled by using parallel simulation implementation of the self-consistent Born approximation in the NEGF formalism [5].

III. RESULTS AND DISCUSSIONS

We first analyze the small signal parameters of graphene FETs with channel scaling down to 5nm.The ideal performance limits for graphene FETs are studied by running ballistic simulations. The potential profile of the device at V_G =-0.6V and V_D =0.5V is also shown in Fig. 1(c). To model scattering, the effect of optical phonon scattering for $\hbar\omega$=180meV and $\hbar\omega$=55meV on device characteristics is included. The elastic scattering by acoustic phonons and charge impurities in high quality graphene has a much longer mean free path than inelastic phonon scattering. Therefore, elastic scattering is not considered as part of this study, focused on channel length scaling in sub 100nm regime. The small signal equivalent model for graphene FETs is shown in Fig. 1(b) where g_m is the transconductance, g_{ds} is the output conductance, R_g is the gate resistance, R_S (R_d) is the source (drain) contact resistance, C_{gs} is the small signal gate to source capacitance, C_{gd} is the small signal gate to drain capacitance and C_{ps} (C_{pd}) is the parasitic capacitance. The model is similar to that of conventional silicon MOSFETs, however, with the element parameters being determined by device physics of graphene transistors. The small signal parameters are extracted by running quasi static simulations for channel lengths down to 5nm. The small quasi static approximations are valid for graphene FETs when the frequency of interest is lower than the intrinsic cut-off frequency. The channel scaling behaviors of the unity current gain frequency f_T and unity power gain frequency f_{MAX} are studied under ballistic limit as well as in presence of optical phonon scattering. The rest of section addresses the effect of parasitic source and drain contact resistance on f_T and f_{MAX}.

Figure 2(a) shows the I_D-V_D characteristics at V_G=-0.6V. A kink behavior with a quasi-saturation region is observed in graphene FETs even at L_g=20nm.This quasi-saturation behavior is due to the drain Fermi level aligning with the Dirac point profile in the channel , followed by onset of ambipolar regime. The low density of states around the Dirac

 ISBN: 978-1-61208-214-1

point gives rise to decrease in current increment and explains the saturation observed for voltages where drain Fermi level is in vicinity of conduction band in channel. Since the density of states is low in a very small energy range around Dirac point, graphene FETs do not exhibit complete saturation seen in conventional silicon MOSFETs. The minimum output conductance needed for RF performance is exhibited in this quasi-saturation regime. The minimum output conductance simulated for ballistic condition is $g_{ds}\approx 5.96\times10^{3}\mu S/\mu m$. The value of the minimum output conductance is lowered in presence of optical phonon scattering. The minimum output conductance simulated for $\hbar\omega$=180meV and $\hbar\omega$=55meV is $g_{ds}\approx 4.92\times10^{3}\mu S/\mu m$ and $g_{ds}\approx 4.71\times10^{3}\mu S/\mu m$ showing 17.5% and 20.9% decrease respectively from ballistic value. The decrease of the minimal g_{ds} in presence of scattering affects the unity power gain frequency of GFETs.

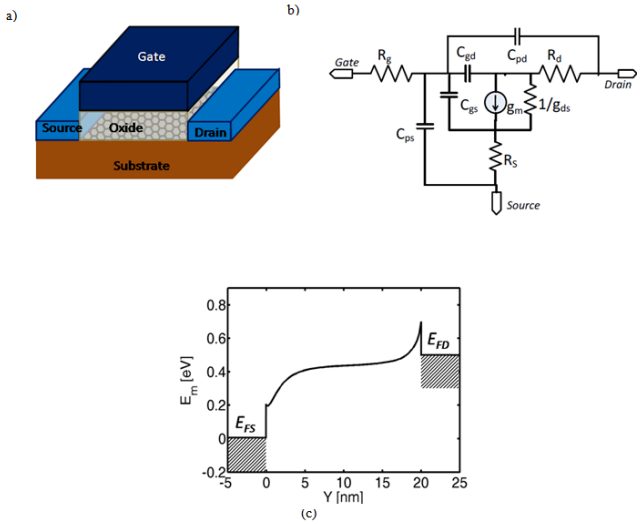

Figure 1. (a) Device structure for the modeled graphene FET. Pd is used as the contact material, Al_2O_3 is used as the insulator material, and its thickness is 2nm. (b) Small-signal equivalent circuit of GFET where g_m is the transconductance, g_{ds} is the output conductance, R_g is the gate resistance, R_s (R_d) is the source (drain) contact resistance, C_{gs} is the small signal gate to source capacitance, C_{gd} is the small signal gate to drain capacitance and C_{ps} (C_{pd}) is the parasitic capacitance . (c) Band profile of the GFET at V_D = -0.5V and V_G = -0.6V. The channel length is 20 nm and E_{FS} (E_{FD}) is the source (drain) Fermi level.

Figure 2(b) shows the I_D-V_G characteristics at V_D=-0.5V. In presence of optical phonon scattering the transconductance is degraded .The maximum simulated transconductance for ballistic condition is $g_m\approx 7.228\times10^{3}\mu S/\mu m$. While, the maximum simulated transconductance for $\hbar\omega$=180meV and $\hbar\omega$=55meV are $g_m\approx 4.669\times10^{3}\mu S/\mu m$ and $g_m\approx 4.3281\times10^{3}\mu S/\mu m$ showing 35.5% and 40.2% degradation respectively from ideal ballistic behavior.

The small signal analyses for graphene FETs is carried out using the equivalent circuit shown in Fig. 1(b) . The effect of parasitic capacitance has already been studied as part of earlier study. The small signal analyses require careful choice of DC bias conditions to get maximum value of f_T and f_{MAX}. Since graphene FETs exhibit quasi-saturation behavior, g_{ds} value is minimum only for very small drain bias voltage range. Therefore, the optimum DC bias point for simulations to ensure maximum f_T and f_{MAX} is chosen by running quantum quasi static simulations for g_{ds} as functions of V_D at different V_G values. Optimum bias point is taken to be a g_{ds} minima point in g_{ds} variation with drain voltage V_D at given gate voltage V_G . It can be extracted from Fig. 2(c). The minima point for g_{ds} is also dependent on V_G value chosen. Fig. 2(c) shows the g_{ds} minima point shifts to right from $V_D\approx$-0.3V at V_G=-0.4V to $V_D\approx$0.45V for V_G=- 0.6V in ballistic simulations. Similar behavior is replicated in presence of phonon scattering. Therefore, bias points are carefully chosen to be V_D=-0.5V and V_G=-0.6V which are optimized bias point values with minimum value of g_{ds} for all channel lengths from 50nm to 5nm under ballistic as well as in presence of scattering .

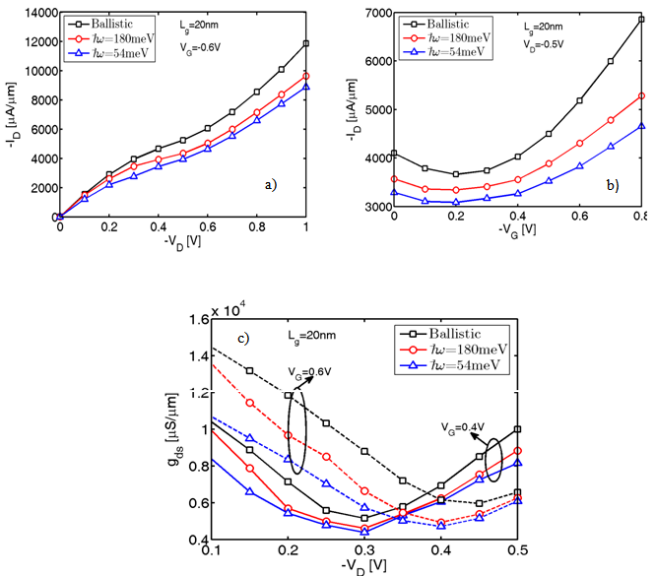

Figure 2. I-V characteristic of the GFET as shown in Fig.1(a) at the ballistic limit and with scattering. Inelastic phonon scattering is modeled for two different phonon energies $\hbar\omega$=54meV and $\hbar\omega$=180meV. The gate length is L_g=20nm. . (a) I_D versus V_D at V_G =-0.6V. (b) I_D versus V_G at V_D = 0.5V. (c) Output Conductance g_{ds} as a function of drain voltage, V_D at V_G =- 0.4V and- 0.6V, respectively.

Next part focuses on studying scaling of the small signal parameters at with the channel length under ballistic and scattering conditions. The gate to drain capacitance, C_{gd} and gate to source capacitances C_{gs} are calculated by running quasi static simulations at V_D=-0.5V and V_G=-0.6V. At a channel length above about 10nm, both C_{gd} as shown in Fig. 3(a) and C_{gs} as shown in Fig. 3(b) approximately linearly increases as the channel length increases. Scattering has a small effect on the values of the intrinsic capacitances compared to its effect on the transconductance. The total gate capacitance is the

 ISBN: 978-1-61208-214-1

serial combination of the gate insulator capacitance and the quantum capacitance, and it is estimated that the gate insulator capacitance is a more dominant factor than the quantum capacitance for the modeled device at this bias point.

The output conductance, g_{ds} increases with decrease of the channel length as shown in Fig. 3(c). The increase of the output conductance is due to the electrostatic short channel effects becoming more prominent at shorter channel lengths. Fig. 3(d) shows the transconductance g_m, as a function of the channel length. As the channel length scales from 50nm to 15nm, the ballistic transconductance only decreases very slightly from the value of about 8118µS/µm. As the channel length scales down to 5nm, the transconductance, however, drops significantly due to electrostatic gate effect already explained as part of earlier study. Similar electrostatic gate affected degradation of g_m below 15nm is observed in even in presence of inelastic phonon scattering. However, at gate lengths above 15nm, g_m decreases in presence of inelastic phonon scattering with increase in gate length. This is attributed to scattering becoming stronger at larger gate lengths. Since f_T as well as f_{MAX} are dependent on g_m, the degradation of g_m due to scattering is not favorable.

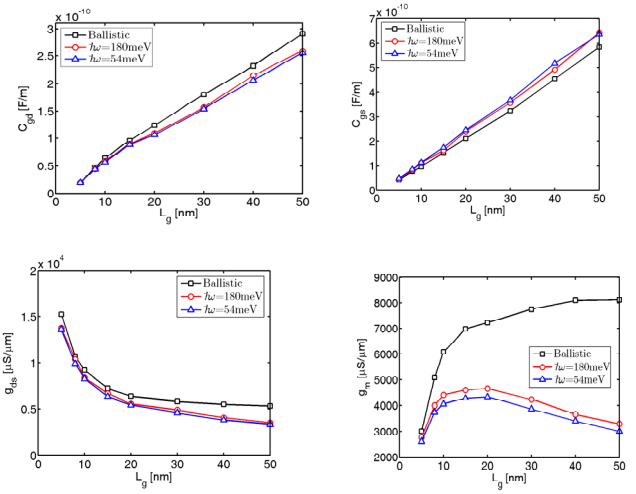

Figure 3. Extracted circuit parameters from quantum device simulations as a function of the gate length at V_D =-0.5V and V_G = -0.6V at the ballistic limit and in the presence of inelastic scattering with two different phonon energies $\hbar\omega$=54meV and $\hbar\omega$=180meV . (a) Small signal gate to drain capacitance C_{gd} (b) small signal gate to source capacitance C_{gs} (c) output Conductance g_{ds} and (d) transconductance g_m as function of channel length L_g.

Next, we examine the dependence of the unity current gain frequency f_T on channel length and scattering. Figure 4(a) shows that the intrinsic f_T increases with decrease in channel length down to 5nm due to smaller intrinsic gate capacitance Since g_m is degraded in presence of scattering, the same effect is manifested in lower f_T values in the presence of inelastic phonon scattering. The decrease in transconductance below 15nm is not reflected in f_T because the decrease in C_{gd} and C_{gs} with channel length outpaces the decrease in transconductance as shown part of earlier study[15]. The intrinsic unity power gain frequency, f_{MAX} as a function of channel length is examined in Fig. 4(b). Below 10nm, f_{MAX} falls off with decrease in channel length. This can be explained due to strong dependence of f_{MAX} on output conductance, g_{ds} and gate resistance R_g, which increase with the decrease in channel length .

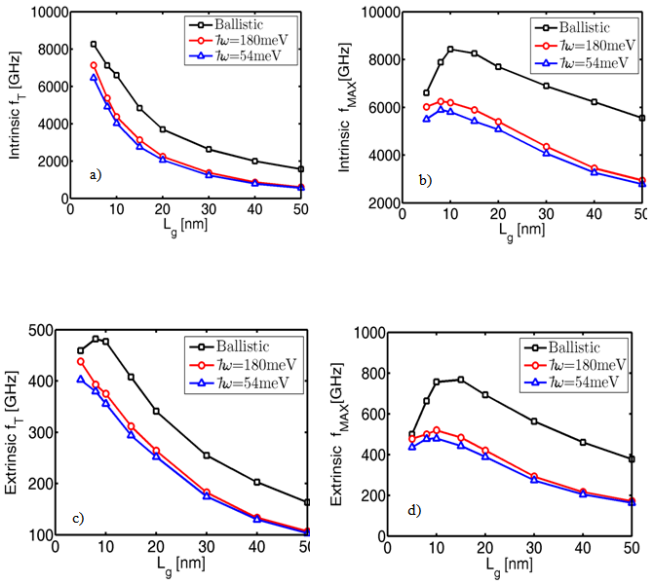

Figure 4. RF figures of merit of GFET vs. the gate length at V_D = -0.5V and V_G= -0.6V at the ballistic limit and in the presence of inelastic phonon scattering with phonon energies of $\hbar\omega$=54meV and $\hbar\omega$=180meV. (a) Intrinsic unity current gain frequency (the cutoff frequency) f_T (b) intrinsic unity power gain frequency (the maximum oscillation frequency) f_{MAX} , which is computed with zero source/drain parasitic capacitance and resistance (c) extrinsic unity current gain frequency f_T and (d) extrinsic unity power gain frequency f_{MAX} as a function of the gate length. The extrinsic frequencies are computed by considering a parasitic source and drain resistance of R_s=R_d = $500\Omega - \mu m$.

The RF performance is also limited by the parasitic contact resistance, which can limit the performance of FETs in real applications. Next, we study the extrinsic performance of graphene FETs including source and drain contact resistances in small signal equivalent model as shown in Fig. 1(b). However, the parasitic capacitance, C_{ps} (C_{pd}) shown in small signal model is assumed to be zero in all simulations. The effect of parasitic capacitance has already been studied as part of earlier study. The contact resistances are taken to be 500Ω-µm. The chosen value for contact resistance is typical for metal-graphene contacts reported in experiments at room temperature. Figure 4(c) shows extrinsic unity current gain frequency f_T in presence of source and drain contact resistances. The extrinsic f_T is less than intrinsic f_T shown in Fig. 4(b) by a factor of 15. Similarly extrinsic f_{MAX} is degraded

 ISBN: 978-1-61208-214-1

by a factor of 10 as shown in Fig. 4(d). Thus, the source and drain parasitic resistance can lower the RF performance of graphene FETs significantly. Therefore, the channel scaling should be complemented with reduced parasitic source and drain resistances to obtain good RF performance of graphene FETs.

It is found that better gate design can also improve f_{MAX} performance. The power gain frequency f_{MAX} is highly sensitive to the width of gate. We next studied graphene FETs performance with metal gate as shown in Fig. 5 for gate widths of 1μm and 10μm. The gate resistance for metal is calculated with R_{sh}=0.33 Ω/□ [24], α=1/3 is a constant for distributed gate resistance[25] and L_g =20nm. Changing gate width from *1*μm to *10*μm degrades the unity power gain frequency values considerably. Thus careful choice of gate width along with DC bias point is necessary to improve extrinsic f_{MAX} performance. In practice, width is limited by drain current and reducing the width is not feasible. The decreased gate resistance to improve extrinsic f_{MAX} performance can be realized by using multi-finger gates.

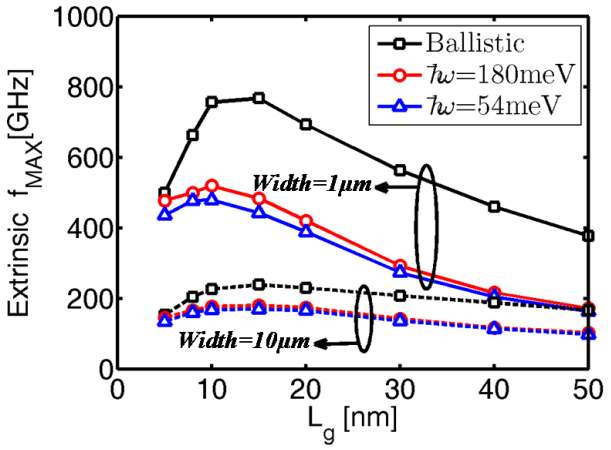

Figure. 5. The extrinsic unity power gain frequency f_{MAX} vs. channel length at the ballistic limit and in the presence of inelastic phonon scattering with phonon energies of $\hbar\omega$=54meV and $\hbar\omega$=180meV for transistor width =*1*μm(solid lines) and *10*μm(dashed lines). The modeled GFET with a channel length of 20nm is biased at V_D = -0.5V and V_G = -0.6V. The length of the gate is fixed at 20nm. The sheet resistivity of metal gate used here is 0.33 Ω/□.

IV. SUMMARY

In summary, the channel length scaling behavior of graphene FETs is studied to analyze RF performance metrics under ideal ballistic conditions and in presence of optical phonon scattering. The simulated intrinsic unity current gain frequency f_T increases to value of 5THz around L_g =10nm . However, the intrinsic power gain frequency, f_{MAX} is less than the unity current gain frequency. Including inelastic phonon scattering lowers both f_T and f_{MAX} due to degradation in g_m . Including the source and drain parasitic resistance lowers both unity current gain frequency as well as power gain frequency by several factors. Since drain and gain contact resistance is always present in real circuits, proper choice of the contact material is necessary to utilize full RF potential of graphene FETs. It is also proposed that careful choice of DC bias point and gate width is needed to get improved power gain frequency performance of graphene FETs.

REFERENCES

[1] K. S. Novoselov et al., "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666–669, 2004.

[2] L. Liao, J. Bai, R. Cheng, Y. Lin, S. Jiang, Y. Qu, Y. Huang, and X. Duan, "Sub-100nm channel length graphene transistors," *Nano Lett*., vol. 10, pp. 3952-3956, 2010.

[3] Y. Wu et al., "RF perfomance of short channel graphene field-effect transistor," *Tech. Dig. of Int. Electron Device Meeting* (IEDM), pp. 226–228, 2010.

[4] J. Chauhan and J. Guo, "Assessmnet of high frequency performance limits of graphene field-effect transistors," *Nano Research,* Vol. 4, p. 571, 2011.

[5] S. Datta, "Quantum transport: atom to transistor," Cambridge University Press, 2005.

 ISBN: 978-1-61208-214-1