Dry Film Resist Microfluidic Channels on Printed Circuit Board and its Application as Fluidic Interconnection for Nanofluidic Chips: Fabrication Challenges

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***Abstract*—Nowadays, nanofluidic chips are usually fabricated with silicon and/or glass. A simple and reliable integration packaging method that provides fluidic interconnection to the outside world has not been yet fully developed. The use of PCB material as substrate to create dry film resist microfluidic channels is the core technology to provide such an integration method. The feasibility and potential of the proposed packaging method is demonstrated in this work.**

Keywords-dry film resist; fluidic interconnection; printed circuit board; nanofluidic channels, integration

I. INTRODUCTION

Microfluidic devices fabricated with dry film resist (DFR) and silicon (Si) and/or glass substrate have been reported [2, 3, 5]. Moreover, nanofluidic devices are usually fabricated with silicon and/or glass [1, 3, 7, 8, 9]; even if nanoimprint technologies are used to fabricate them, a rigid substrate (usually glass) is required [10, 11].

The use of silicon and/or glass to build fluidic systems elevates their cost [6]. Furthermore, the reliable fluidic connection of nanofluidic devices to the outside world still needs to be optimized in order to reduce costs and simplify the fabrication process.

A low-cost fabrication method for microfluidic channels as fluidic interconnection for nanofluidic chips is here presented. Printed circuit board (PCB) material is proposed as the substrate to laminate DFR for the fluidic interconnections.

Following this approach, the fluidic chip can be kept small thus decreasing its cost. Furthermore, the low-cost PCB facilitates the fluidic and electrical connections to the outside world allowing the integration of micro- and nanodevices in a simple and fast way.

In this work, the principle of the packaging integration technology is explained. In Section III, the physical properties of the materials used are presented. In Section IV, the fabrication process is detailed. Then, the challenges associated with the fabrication process are treated; first the challenges associated with the fabrication of DFR fluidic channels on PCB, then, the challenges associated with the use of different materials as a substrate. Finally, the devices are tested against leakage and the compatibility of the materials is studied by means of a thermal shock test in order to determine delamination.

II. PRINCIPLE

The key material enabling the use of DFR microfluidic channels on PCB for its use as the fluidic interconnection of nanofluidic chips is a nonconductive adhesive (NCA). Figure 1 shows a schematic of the concept.

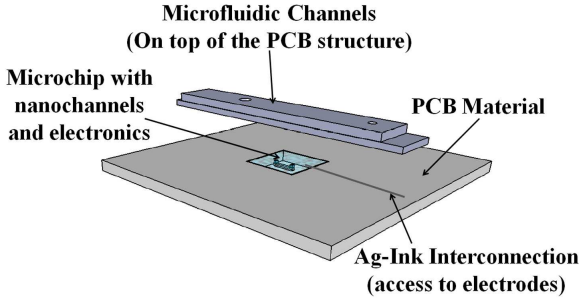

Figure 1. Schematic of the interconnection of nanofluidic chips by means of dry film resist channels on top of PCB material.

The already fabricated nanofluidic chips are inlaid on the PCB material by means of a NCA. The fluidic chip(s) together with the PCB material compose the substrate.

Finally, the lamination of dry film resist on top of the substrate allows fabricating the microfluidic channels that interconnect the nanofluidic chips to the outside world.

Concerning the electric access to the nanofluidic chip(s), ink-jet printed interconnection lines can be applied between the electronic contacts of the fluidic chips and the pads on the PCB. This latter topic however is not treated in this paper.

III. MATERIALS

TMMF dry film resist poses a unique stability when in contact with alkaline solutions and acids [3, 5] and provides high resolution and aspect ratios [2, 5] making it the resist of choice for the fabrication of microfluidic channels.

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The DFR used to fabricate the microfluidic channels is TMMF S2030, a permanent photoresist for MEMS from Tokyo Ohka Kogyo Co., Ltd. This negative photoresist is composed 5% of antimony compound and 95% of epoxy resin [2, 3].

Furthermore, the PCB material used as mechanical support for the whole system is Rogers RO4003C, a glass reinforced hydrocarbon laminate with low roughness characteristics.

Table 1 shows the physical characteristics of TMMF S2030 and Rogers RO4003C.

TABLE I. PHYSICAL PROPERTIES OF TMMF S2030 AND ROGERS RO4003C [2, 13]

Physical Properties of TMMF S2030 and Rogers RO4003C		
Physical Property	***TMMF S2030***	***Rogers RO4003C***
Coefficient of thermal expansion (ppm/°C)	65	X 11 Y 14 Z 46
Transition glass temperature (°C)	230	>280
Moisture absorption (%)	1.8	0.06
Dielectric constant	3.8	3.38±0.005
Transparency (nm)	400-600	-
Breaking strength (MPa)	60.3	-
Young modulus (MPa)	2100	26.889

The NCA used to glue the fluidic chip to the PCB material is a colorless epoxy-based adhesive with a glass transition temperature (Tg) of 45 °C and a coefficient of thermal expansion (CTE) of 56 ppm/°C when below the glass transition temperature, and 211 ppm/°C when above the glass transition temperature.

IV. FABRICATION PROCESS

The very first step to proceed to the fabrication of the TMMF microfluidic channels on top of PCB material for the fluidic interconnection of nanochips is to form the substrate composed by the PCB and the fluidic chip(s). Figure 2 illustrates this process.

According to Figure 2, to align the PCB material and the nanofluidic chip a double side Kapton tape is rolled in a silicon wafer or glass (a). The PCB and the chip are mounted on the Kapton tape (b). The epoxy-based adhesive is dispensed in the space between the PCB material and the chip (c). The materials are placed in an oven or hot plate at 80 °C for 3 hours to cure the adhesive (d). When the adhesive is totally cured, the materials are left at room temperature for a while to allow them to cool down. The new substrate consisting of the chip inlaid in the PCB material is removed from the Kapton tape (e).

The second stage of the fabrication process consists in laminating the TMMF microfluidic channels on top of the formed substrate. Figure 3 shows the flowchart for this process.

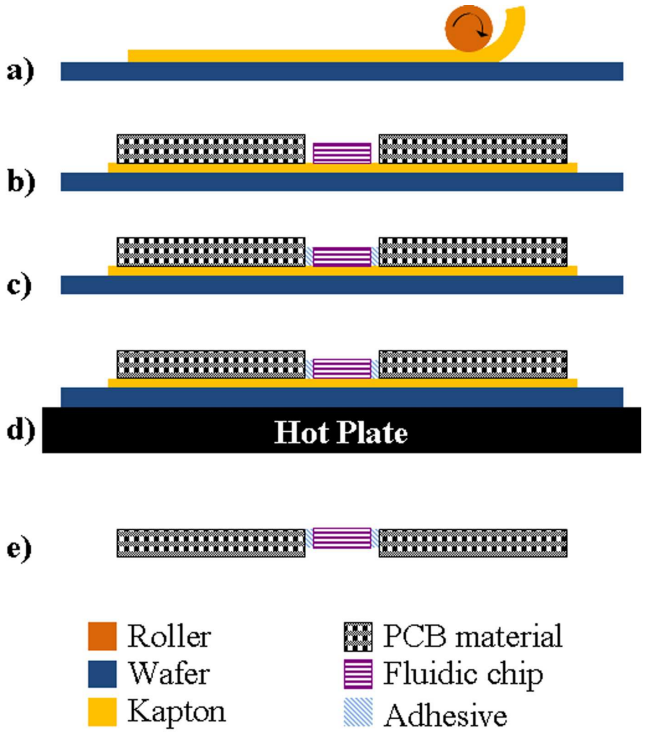

Figure 2. PCB material and nanofluidic chip leveling process flow chart.

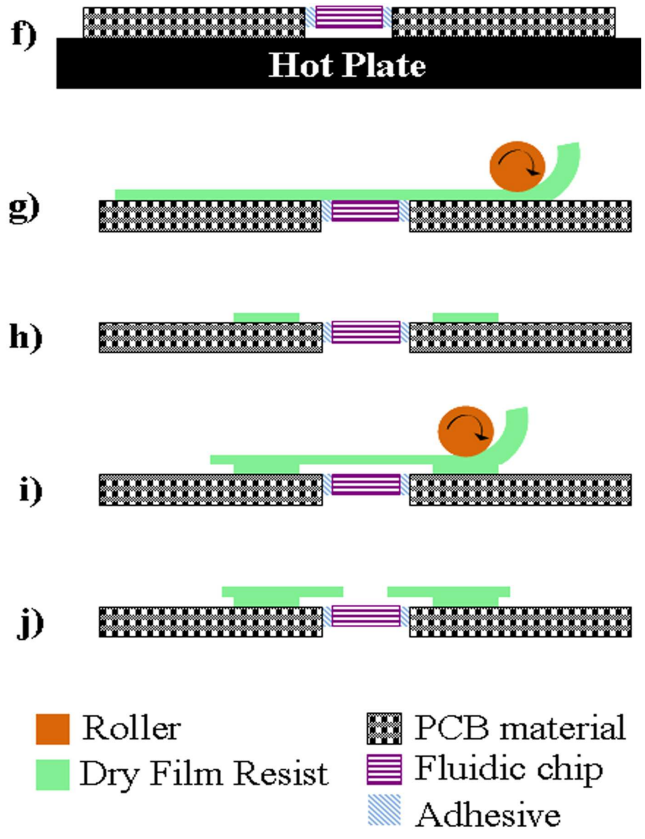

Figure 3. TMMF microfluidic channels lamination on top of the formed substrate.

The substrate is cleaned with ethanol, dried on a hotplate for 2 hours at 120 °C (f). This will avoid that the humidity absorbed by the PCB material affects the DFR lamination process. An oxygen plasma treatment is performed to the substrate in order to improve the adhesion between the TMMF resist and the formed substrate.

The substrate is kept at 45 °C. One of the polyethylene terephthalate (PET) protective layers is removed from the DFR and the TMMF resist is laminated on the substrate (g). The other PET layer is removed after the sample has cooled down. A soft baking step is performed at 90 °C during 5 minutes. The exposure is performed after the sample cools down to room temperature. A post exposure baking step is performed with the same temperature and time as the soft baking step. The TMMF is developed with PGMEA after the sample has cooled down to room temperature (i). A second layer of TMMF is laminated at 45 °C in order to close the microfluidic channels. The second layer is exposed after lamination without removing the remaining PET layer. The sample is cured at room temperature during one day. The PET layer is removed and access holes to the channel are punched with the help of a needle (j). Tests are conducted.

V. CHALLENGES ASSOCIATED WITH THE FABRICATION PROCESS

Here, the challenges encountered are grouped by:

- Challenges associated with the lamination of TMMF on PCB material.
- Challenges associated with the TMMF lamination on top of the fluidic chips.

A. TMMF and Rogers

The challenges associated with the processing of TMMF resist on Rogers materials are: pinholes in the photoresist, trapped bubbles between the resist and the PCB material, cracks in the photoresist, and closed channels.

a) Pinholes: TMMF might present pinholes after the soft baking step.

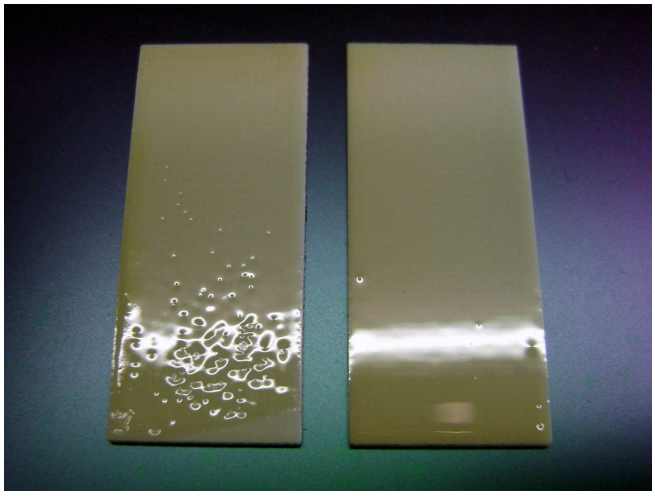

Figure 4. PCB material immersed under water prior to TMMF lamination (left) and PCB material dried at 120 °C prior to TMMF lamination (right). The presence of pinholes on the TMMF resist after soft baking is influenced by the moisture absorbed by the PCB.

Experiments were conducted, and up to some extent, the pinholes can be decreased by using a plasma treatment, nevertheless, the crucial factor determining their presence is the moisture absorbed by the PCB material.

Figure 4 shows two PCB materials where TMMF was laminated and soft baked. In the sample on the left side, the PCB material was immersed in water during 2 hours and its surface was dried with nitrogen prior to TMMF lamination. In the specimen on the right, the PCB material was placed on a hotplate during 2 hours at 120 °C in order to evaporate the absorbed moisture prior to TMMF lamination.

b) Trapped bubbles and cracks: Conducted experiments show that if the baking times are either higher or lower than the optimal time and the PCB material contains humidity absorbed from the atmosphere, trapped bubbles and cracks will form in the photoresist structures. The formation of trapped bubbles is directly related to the humidity absorbed by the PCB material and the use of inadequate baking times. The formation of cracks is related to the thermal stresses that result from a forced cooling down of the specimens after the baking steps and improper baking times. Furthermore, the humidity absorbed by the PCB material promotes the formation of cracks.

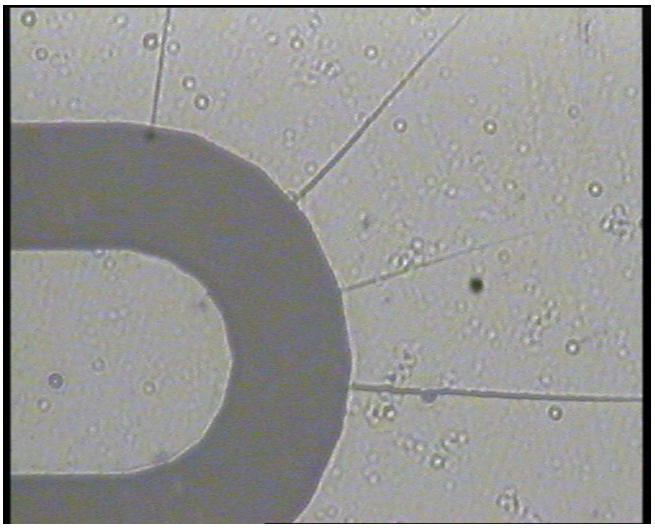

Figure 5. Trapped bubbles between the TMMF resist and the PCB material and cracks due to the humidity absorbed by the PCB material and the improper baking times used for processing of the TMMF.

Figure 5 shows trapped bubbles between the TMMF and the PCB material as well as cracks in the dry film resist structures. The PCB material used for this experiment was not dried prior to TMMF lamination. Moreover, the baking times used in the processing were not optimal.

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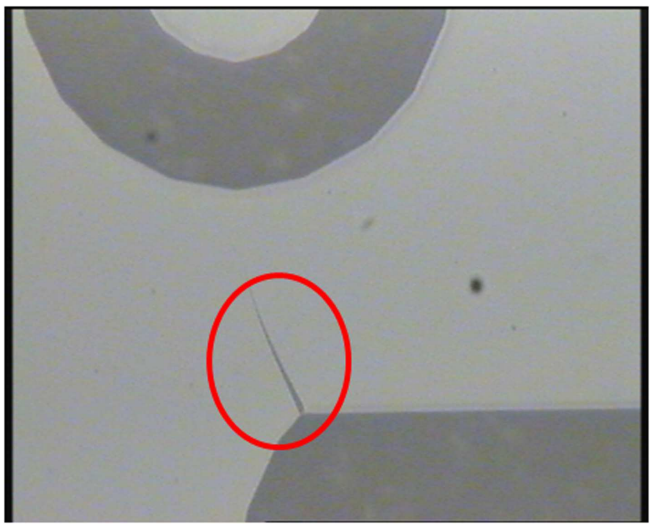

Figure 6. Cracks in the TMMF structures with angles close to 90 °C. The circle in the image points the crack.The cracks are caused by the use of not optimal baking times.

Figure 6 shows a crack in the photoresist structure, but no trapped bubbles. The PCB material used for this experiment was dried prior to TMMF lamination, nevertheless, the baking times were not optimal.

c) Closed channels: The exposure time should be controlled accurately when working with Rogers' materials. The effects of an underexposed resist, as Figure 7 shows, are well known. On the other hand, overexposure can result in partially or totally closed fluidic channels.

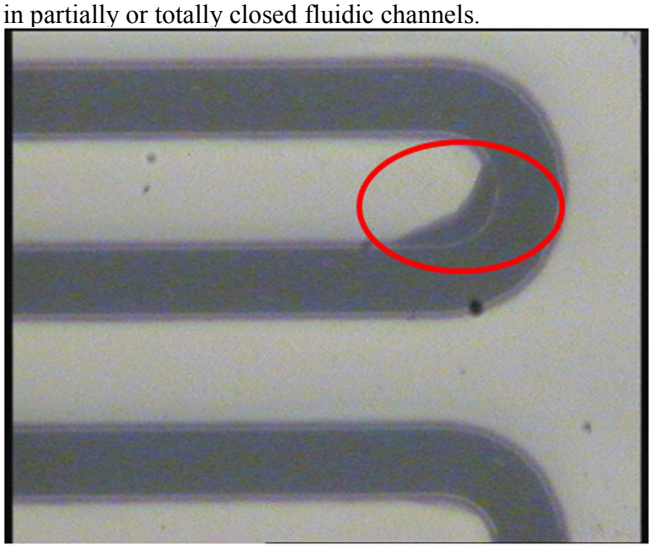

Figure 7. Effects of insufficient exposure time. The circle points an obvios underexposure effect on the TMMF structure.

Scattering and diffraction of ultraviolet (UV) light during exposure is unavoidable when using a nontransparent material. Furthermore, the white color of the PCB material makes reflection of the waves a bigger problem.

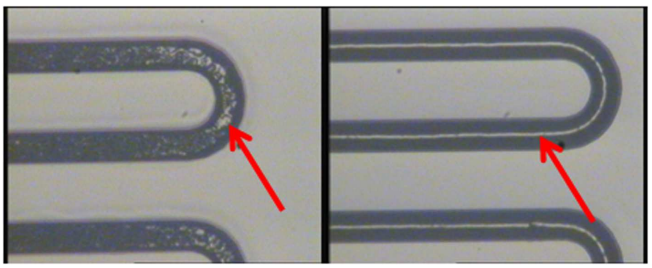

Figure 8. Closed channels on PCB material due to overexposure of the TMMF resist. The arrow in the left image points the effects of an overexposure of 2 seconds. The arrow in the right image points the effects of an overexposure of 6 seconds.

The more a sample is overexposed, the more closed the channels will be. Figure 8 shows a sample overexposed by 2 seconds (left) and a sample overexposed by 6 seconds (right).

B. TMMF and the nanofluidic chips

Nanofluidic chips are usually made of glass and/or silicon. PCB material and Si poses different thermal characteristics. The thermal conductivity of the PCB material is approximately 0.71 W/m/°K [13] and the thermal conductivity of Si is around 140 W/m/°K [12]. Due to the thermal characteristics of the materials, heat transport at the baking steps is not a problem for the PCB material but it is for the Si fluidic chip.

The most common problem associated with the lamination of TMMF on silicon is cracks due to heat transport at the baking steps and the CTE [3]. Figure 9 illustrates this problem.

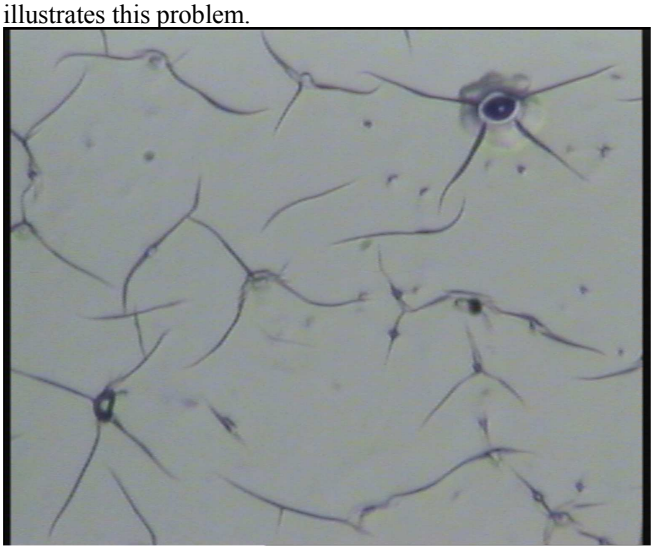

Figure 9. Cracks in the TMMF resist due to the CTEs difference between silicon and the TMMF resist.

When the PCB material and the fluidic chip are of almost the same thickness, the microfluidic chip will conduct heat around 25 times more than the PCB material. Therefore, placing the substrate directly at 90 °C during the baking steps will originate cracks on the TMMF laminated over the fluidic chip. To solve this, the temperature needs to be ramped (2 °C/min) starting at 55 °C during the baking steps,

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when the temperature reaches 90 °C the samples are baked 5 minutes. Afterwards the hot plate's temperature is set to 25 °C and the sample is removed from the hot plate when the 25 °C is reached.

Furthermore, if the fluidic chip is considerably thinner than the PCB material, the substrate can be placed directly at 90 °C. In this case, the thermal conductivity of the air between the chip and the hot plate will limit the heat flux to the chip, avoiding the presence of cracks on the TMMF.

VI. EXPERIMENT SETUP

In order to test the feasibility of the proposed interconnection technology, a leakage test was conducted to the devices together with a reliability test.

The leakage test consists of injecting a rodhamine + ethanol + di water solution in the TMMF channels through one of the inlets. A visual inspection follows to detect any leakage. Special attention is given to the interconnection area between the different materials. Figure 10 shows the mentioned interconnection area before closing the TMMF channels.

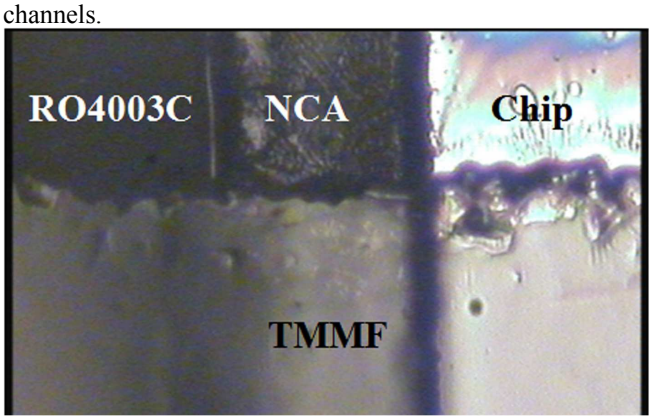

Figure 10. Close up of the interface between the different materials that form the fluidic interconnections to the nanofluidic chips.

The reliability test consists of a thermal shock test based on the MIL–STD–883C. The purpose of this test is to accelerate the appearance of delamination and cracks. The test consists of 15 cycles where each cycle is composed by a high temperature and a low temperature step. The high temperature step is performed at 100 °C (+10 °C, -2 °C) and the low temperature step at 0 °C (+2 °C, -10 °C). Each step is performed for 5 minutes. The liquid used to perform the test is water. After completing the test, a visual inspection is performed at a magnification no greater than 3x [4].

VII. RESULTS

In this section, the results are presented in three subsections. First the results concerning the lamination of TMMF on PCB material are presented. Then the leakage test results are exposed. Finally, the results concerning the compatibility of the different materials and the reliability of the packaging method are presented.

A. *TMMF resist channels on PCB material*

To obtain good results fabricating microfluidic channels on PCB materials some factors should be kept in mind. The baking times provided by the companies are optimal, nevertheless, different materials conduct the heat in a different rate, and therefore, the material temperatures might deviate from the prescribed temperature, especially when using a hot plate. Furthermore, PCB materials are more reflective than silicon or glass; because of this the exposure time should be tuned accurately, if channels of less than <20 µm are desired, this parameter is critical.

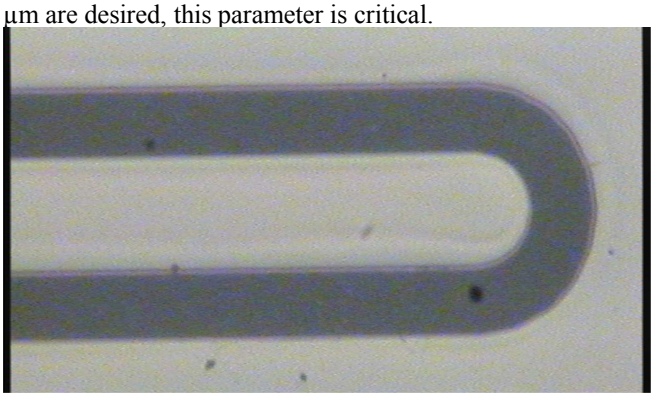

Figure 11. Microfluidic channels on PCB material. The image shows the results of optima processing parameters (exposure and baking times).

Figure 11 shows a TMMF structure on PCB material fabricated with optimal exposure and baking times.

B. *Leakage test*

Concerning the leakage test, Figure 12 shows a device with the packaging technology presented in this work.

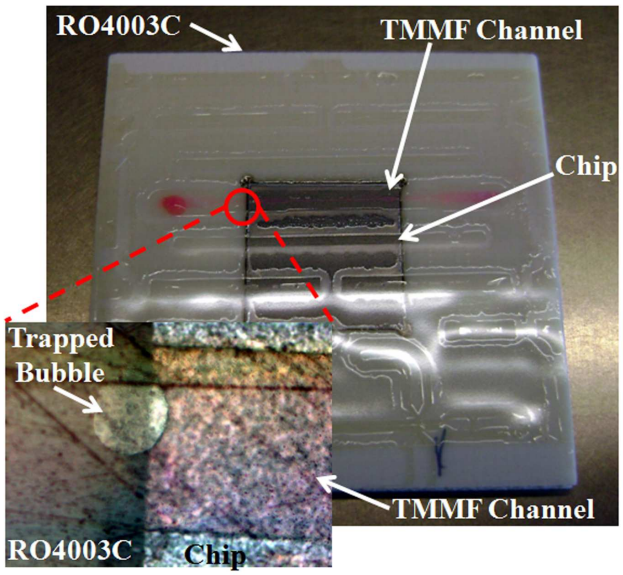

Figure 12. TMMF microfludic channels on PCB material as fluidic interconnections for nanofluidic chips. The small image in the lower left corner zooms in at the interface of the different materials that compose the device; it shows no leakage of the rodhamine solution.

The pink liquid flowing through the TMMF channel is a solution of rodhamine + ethanol + di water. It is possible to

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observe that no leakage occurs. The small image at the lower corner in the left was obtained with a 1X71 Olympus inverted microscope equipped with a los noise self cooling CCD camera (color view II, Olympus); it shows, with 10x magnification, the area where the different materials interconnect. It is possible to observe the liquid solution flowing through the TMMF channel without leakage.

C. *Reliability test*

Figure 13 shows a device without closed channels after the thermal shock test.

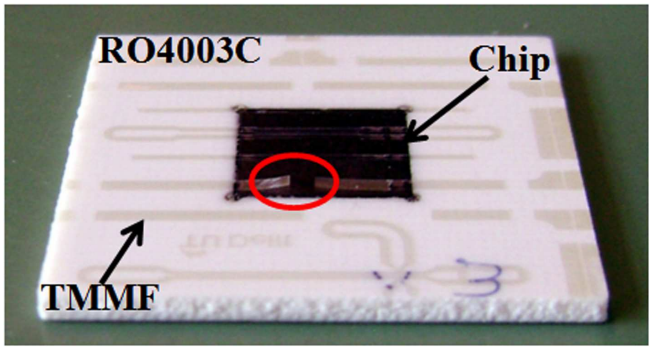

Figure 13. TMMF delamination on top of the Si chip after the thermal shock test. The circle points at the place where the delamination occurs.

The red circle makes emphasis on a failure result from the test. Delamination of TMMF occurs on top of the fluidic chip. From the 3 tested specimens, the failure was observed only in the specimen from Figure 13.

VIII. CONCLUSION AND FURTHER WORK

The use of TMMF resists for the fabrication of microfluidic channels on PCB as fluidic interconnections of nanofluidic chips to the outside world is feasible, providing of simplicity the fabrication process.

The thermal shock reliability test showed that the use of high temperature conditions could bring delamination problems mainly at the interface TMMF–Si chip. This means that the strength of the TMMF microfluidic interconnections decreases and so the probability of leakage increases.

Further work includes the study of the usability of ink-jet printing to create the electrical interconnections between the fluidic chip electrodes and the PCB tracks. The PCB in turn can carry the necessary electronics for control and read-out. This will enable the PCB as the core for the integration of micro- and nanofluidic chips together with the electronics into a complex system.

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