A Novel Realization of Sequential Reversible Building Blocks

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Abstract—**With phenomenal growth of high speed and complex computing applications, the design of low power and high speed logic circuits have created tremendous interest. Reversible computing has emerged as a solution for future computing. A number of combinational circuits have been developed but the growth of sequential circuits was not significant due to feedback and fan-out was not allowed. However allowing feedback in space, sequential logic blocks have been reported in literature. The target technology is likely on quantum computing devices. Reversible flip-flops are the most significant and basic memory elements that will be the target building block of memory for the forthcoming quantum computing devices. This paper proposes a novel reversible gate and its quantum realization. The design of reversible flip-flops, Serial In Parallel Out (SIPO) shift register and shift counter is shown by using our proposed gate and basic reversible gates. The proposed design of sequential reversible circuits has significant improvement over earlier designs in terms of quantum cost and hardware complexity. It is expected that it will enhance the growth of sequential reversible circuit. The proposed gate is also parity preserving gate. This characteristic of the gate may also be useful in fault tolerant sequential circuit design.**

Keywords-reversible computing; sequential circuit; flip-flops; quantum computation.

I. INTRODUCTION

Heat dissipation and high power consumption are one of the most important issues in the digital circuit design. Conventionally, the logic elements are irreversible in nature. According to R. Landauer's principle [1], irreversible logic computation results in energy dissipation due to heat loss. Each bit of information dissipates at least KTln2 energy at which the operation is performed. In early 1973, C. H. Bennett [2] had shown that the problem of heat dissipation of VLSI (Very Large Scale Integrated) circuits can be overcome by using reversible logic. Due to this fact, the loss of information and consequently dissipation of energy in computational operation is significantly lower than conventional logic. Thus, reversible logic and its applications have spread in various technologies like low power CMOS (Complementary Metal-oxide Semiconductor) design, optical information processing, quantum computing, nanotechnology, etc.

In the design of reversible logic circuits, research was limited to the design of combinational circuits, due to the convention that feedback is not allowed in reversible computing. However, in one of the well known fundamental paper, T. Toffoli [3] has shown that feedback can be allowed in reversible computing. According to T. Toffoli," a sequential network is reversible if its combinational part (i.e., the combinational network obtained by deleting the delay elements and thus breaking the corresponding arcs) is reversible." In 1982, Edward Fredkin [4] has used this concept to propose the first design of the reversible sequential circuit called the JK latch having the feedback loop from the output to input. Recently, A. Banerjee et al. [5] have redefined that feedback is allowed in space but not in time. Hence, the development of reversible sequential circuits has begun.

In the current literature, the significant work can be found on the efficient design of combinational reversible circuits such as full adders, BCD (Binary Coded Decimal) adders, encoder and multiplexers and several synthesis methods have been proposed [6]. In last few years, the design of sequential reversible circuits has attracted the attention of researchers in the area of optimization and synthesis.

A Reversible Gate is a p-input, p-output (denoted by p*p) circuit that produces a unique output pattern for each possible input pattern. There is a one to one correspondence between the input and output vectors. Any reversible logic design should minimize the following optimization parameters:

a) Gate Counts: The total number of gates used in a circuit.

b) Garbage Outputs: These Outputs are not used in output functions, but are required to maintain the reversibility. The garbage outputs are defined for a circuit not for a gate.

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c) Constant Inputs: Constants are the input lines that are either set to zero or one in the circuit's input side.

d) Quantum Cost: Each reversible gate has a cost associated with it called the Quantum Cost. The quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates or quantum logic gates required in its design. The computational complexity of a reversible gate can be represented by its quantum cost. The quantum costs of all reversible 1×1 and 2×2 gates are taken as unity.

e) Hardware Complexity: The total number of logic operations in a circuit is known as hardware complexity. In hardware complexity, the terms are:

α = A two input EX-OR gate calculation

β = A two input AND gate calculation

δ = A NOT calculation

Basically, it refers to the total number of AND, OR and EXOR operation in a circuit.

However, the gate count is not a good metric of optimization as reversible gates are of different type having different computational complexity. Hence, the optimization of quantum cost is the major metric in the design of sequential reversible circuits. A. Banerjee et al. [7] have addressed that if a set of reversible quantum gates organized in a black box then it can be visualized as a new gate. Reduction of these parameters should be the main design focus in sequential reversible circuits. The basic reversible gates as Toffoli Gate [3] (CCNOT gate), Feynman Gate (CNOT Gate) [8] and Fredkin Gate [4] will be used in the designing of sequential reversible circuits.

In this work, we are proposing a novel parity preserving reversible gate and its quantum realization by using quantum cost optimization algorithm [7]. Further, our propose gate is used in the realization of reversible flip-flops and shift counter.

The next sections of this paper are as follows. Section II provides the related work in the past. Section III provides the details about the proposed reversible gate and its quantum realization. Section IV provides reversible design of flip-flops. The reversible design of SIPO shift register and shift counter is described in section V. Section VI has the discussion on results. Section VII concludes the work.

II. RELATED WORK

In 2005, the first attempt on the design of reversible flip-flop was H. Thapiyal et al. [9]. In this work, the Fredkin, Feynman and New Gate was used as AND, NOT and NOR Gate respectively. In the designing of reversible flip-flop, the conventional design of a flip-flop was used. In 2006, J. E. Rice [10] has proposed all the reversible flip-flops (except R-S) using R-S latch. For the designing of reversible flip-flops, Toffoli and Feynman Gate were used as CCNOT and CNOT gate respectively. S. K. S. Hari et al. [11] have addressed reversible flip-flops by using basic reversible Fredkin and Feynman gates. The reversible flip-flops were proposed by A. Banerjee et al. [5] in 2007. For the construction of reversible flip-flops, Toffoli gate (CCNOT Gate), Feynman (CNOT gate) and NOT were used. A novel concept on the designing of reversible flip-flops was proposed by Min-Lun Chuang et al. [12] in 2008. In this work, all reversible latches (except the SR latch) and their corresponding flip-flops were proposed. In 2011, the reversible D flip-flop and shift registers [13] and T flip-flop were addressed by V. Rajmohan et al. [14]. Two Sayem Gates and one Fredkin Gate were used for the designing of reversible T flip-flop.

At last but not least, in 2012, reversible J-K and D flip-flop were proposed by Lafifa Jamal et al. [15] using basic reversible Fredkin and Double Feynman gates. Recently, the design of reversible T flip-flop was proposed by Shubham Gupta et al. [16] using a new gate named SVS gate.

Thus, from a careful survey of the existing works on reversible sequential circuits, it can be concluded that most of these work considered the optimization of number of reversible gates and garbage outputs, while ignoring the important parameters of quantum cost and hardware complexity.

Our goal is to describe the quantum realization of the proposed reversible gate and optimize the design of reversible sequential circuits in terms of all important parameters, viz., the gate counts, quantum cost, garbage outputs and hardware complexity. Normally, two or three parameters are optimized in earlier designs but we have considered all above parameters shown significant improvement in most of the cases using our proposed reversible gate. The low cost shift counter is also designed using the proposed reversible D flip-flop and basic reversible gates.

III. PROPOSED REVERSIBLE PARITY PRESERVING GATE AND ITS QUANTUM REALIZATION

The section describes our proposed parity preserve gate named "Pareek" gate and its quantum realization.

A. Proposed Reversible Parity Preserving Gate

We propose a new 4×4 parity preserve reversible circuit, called Pareek gate. The block diagram of the proposed gate is shown in Fig. 1.

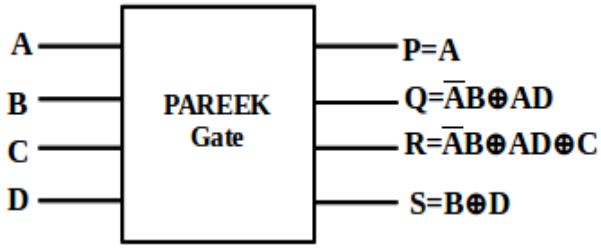

Figure 1. Proposed parity preserving reversible pareek gate

The truth table of proposed parity preserving Pareek Gate is shown in Table I.

The output P (=A) is copied directly from input A, this input to output line is called control line where as other lines are called target lines. The gate produces three outputs, namely, Q, R and S on target lines as defined in Fig. 1. The outputs are verified manually through the truth table.

TABLE 1. TRUTH TABLE OF THE PROPOSED REVERSIBLE GATE

Input				Output			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	1	1	1
1	0	1	0	1	0	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

It is observed that the parity of the input bits is equal to the parity of the output bits in each row of the Table I. Hence, the gate also preserves the parity. This characteristic can further be used in fault tolerant design of reversible sequential circuit. However, we propose the low cost design of reversible sequential building blocks using this gate.

B. Quantum Realization of Proposed Gate

The quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates or quantum logic gates required in its design. The computational complexity of a reversible gate can be represented by its quantum cost. The quantum costs of all reversible 1×1 and 2×2 gates are taken as unity. Any reversible gate can be realized using the 1×1 NOT gate, and 2×2 reversible gates such as Controlled-V and Controlled-V^+ and the Feynman gate which is also known as the Controlled NOT gate (CNOT). Thus, it can said that the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V^+ and CNOT gates required in its implementation. The quantum cost of proposed reversible gate is calculated by an optimization algorithm [7].

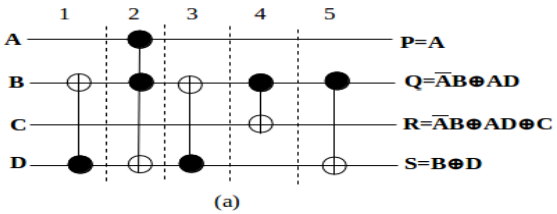

Figure 2. (a) Realization of proposed gate using Toffoli and CNOT gate

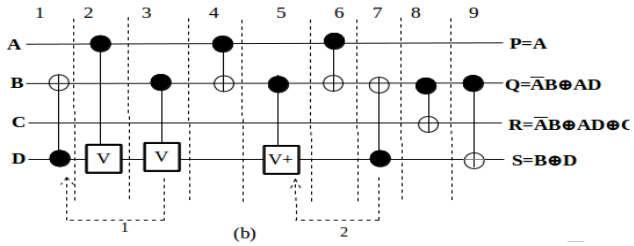

Figure 2. (b) Quantum realization of proposed gate

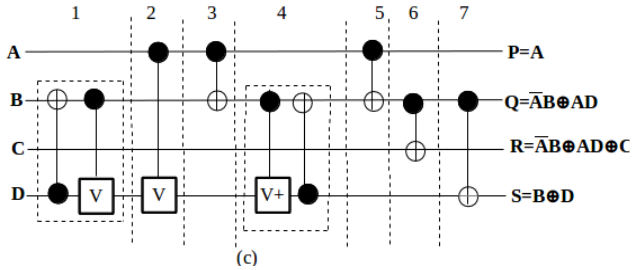

Figure 2. (c) Optimized quantum realization of proposed gate

In Fig.2 (a), the proposed Pareek gate is realized using one Toffoli gate and four CNOT gates. Then, Toffoli and CNOT gates are substituted by quantum primitives and moving rule is applied (the movements are shown by arrows), so its direct linear cost is (1×5) + (4×1) =9, which is shown in Fig.2 (b). New gates are introduced (dashed boxes) in Fig.2 (c) to yield quantum cost of Pareek gate as 7.

IV. PROPOSED REVERSIBLE FLIP-FLOPS

A flip-flop is a circuit that has two stable states and can be used to store state information. It is the basic storage element in sequence logic. The design of reversible flip-flops is proposed in this section.

A. Proposed Reversible D flip-flop

We propose the realization of D Flip-flop using our proposed reversible gate. The reversible design is shown in Fig. 3 and the corresponding block diagram is shown in Fig.4.

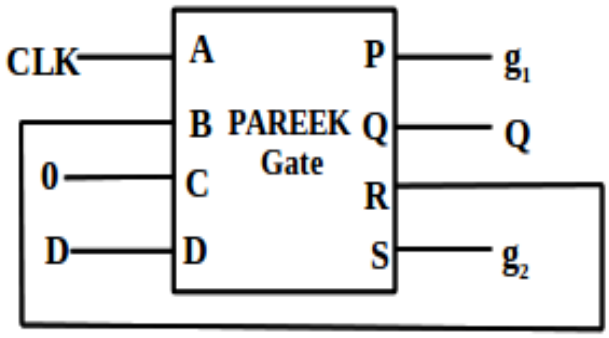

Figure 3. Proposed Realization of Reversible D flip-flop

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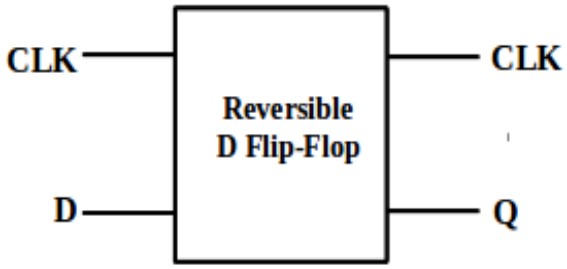

Figure 4. Proposed Block Diagram of Reversible D Flip-Flop

Due to the proposed parity preserving gate, the realization of reversible D flip-flop is also parity preserving.

B. Proposed Reversible R-S flip-flop

The reversible design of R-S flip-flop is shown in Fig. 5.

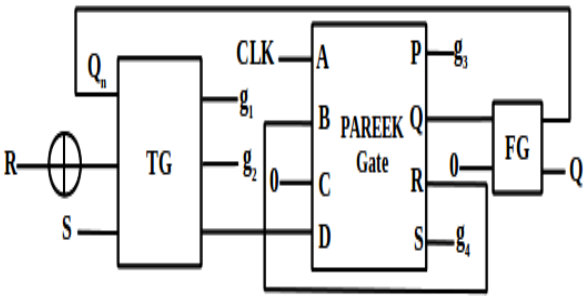

Figure 5. Proposed Realization of Reversible R-S Flip-Flop

The realization of R-S Flip-flop is proposed using our proposed reversible gate, Feynman and Toffoli Gate.

C. Proposed Reversible J-K flip-flop

A J-K flip-flop is a refinement of the R-S flip-flop in that the indeterminate state of the R-S type is defined in the J-K type. The reversible design is shown in Fig. 6.

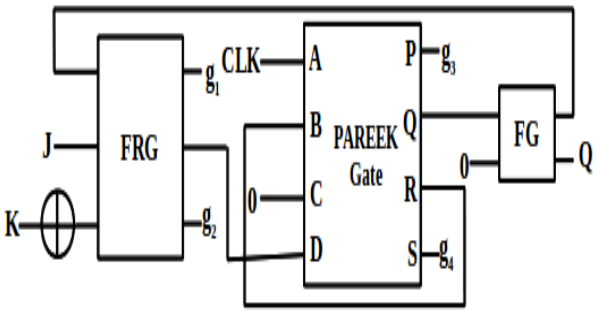

Figure 6. Proposed Realization of Reversible J-K Flip-Flop

The proposed reversible J-K Flip-flop is realized using our proposed reversible gate, Fredkin and Feynman Gate.

D. Proposed Reversible T flip-flop

The T flip-flop is a single-input version of the J-K flip-flop. The reversible design of proposed T flip-flop is shown in Fig.7.

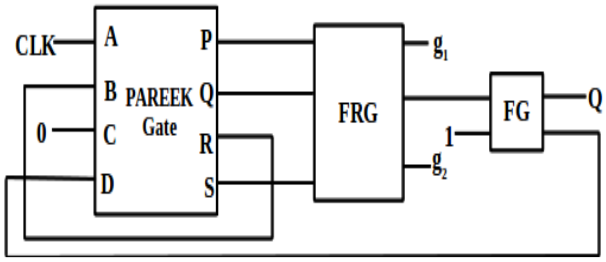

Figure 7. Proposed Realization of Reversible T Flip-Flop

T Flip-flop is realized using our proposed reversible gate, Fredkin and Feynman Gate.

V. DESIGN OF PROPOSED REVERSIBLE SIPO SHIFT REGISTER & SHIFT REGISTER COUNTER

The shift register is an indispensable functional device in a digital system. A register capable of shifting binary information either to the right or to the left is called shift register. In a shift register, the flip-flops are connected in such a way that the bits of a binary number are entered into the shift register, shifted from one position to another and finally shifted out.

Shift register can be arranged to form counters. Shift register counters use feedback, whereby the output of the last flip-flop in the shift register is connected back to the first flip-flop.

This section provides the reversible design of Serial In and Parallel Output (SIPO) shift register and shift register counter by using our proposed reversible gate.

A. Proposed Reversible SIPO Shift Register

A 4-bit Serial in parallel out shift register consists of one serial input, and outputs are taken from all the flip-flops parallel. In this register, data is shifted in serially but shifted out in parallel. The reversible design of SIPO shift register using proposed D flip-flop is shown in Fig. 8.

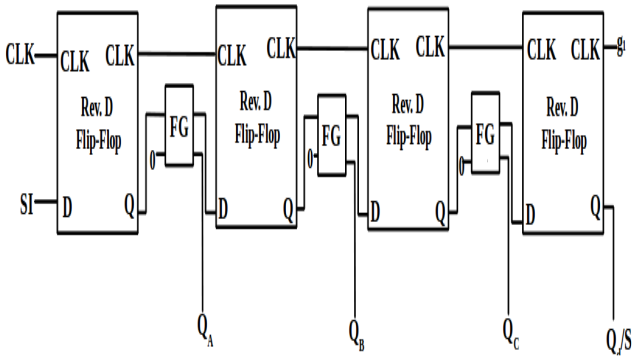

Figure 8. Proposed Realization of Reversible SIPO Shift Register

The serial input is provided to the SI input of the reversible left-most flip-flop while the outputs Q_A, Q_B, Q_C, Q_D are available in parallel from the Q output of the flip-flops.

B. Proposed Reversible Shift Counter (Johnson Counter)

In shift counter, the inverted true output (Q) of the last flip-flop is connected back to the serial input of the first flip-flop. Fig. 9 shows reversible design of shift counter using proposed reversible D flip-flop.

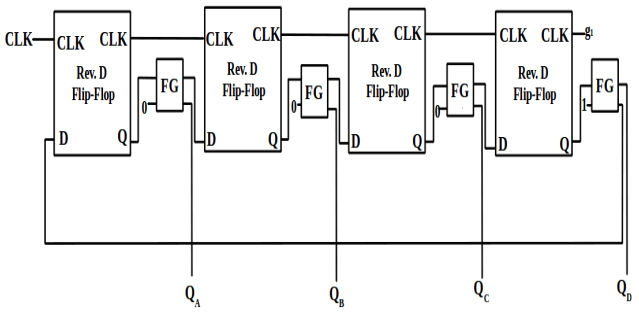

Figure 9. Proposed Realization of Reversible Shift Counter

The output of each reversible flip-flop (Q) is connected to the D input of the next stage. However, the inverted output of the last flip-flop.

VI. DISCUSSION ON RESULTS

Table 2 to Table 7 shows statistics and comparison of our new proposed design of sequential elements against the proposed designs by various researchers. We use the optimization parameters like gate counts, garbage output, constant input, quantum cost and hardware complexity as the cost functions to measure the quality of the design.

The row for "Improvement Percentage" (IP) is the percentage factor of {100-(Proposed Design/Existing Design)*100} %. For example, for a D flip-flop design, our realization has 1 gate while Existing Design [10] has 11 gates. Thus, the ratio is {100-(1/11)*100} % = 91%. The cost of constant input, quantum cost and hardware complexity is not summarized by all the researchers of their reversible sequential elements. We count these numbers based on their designs and show them in tables.

TABLE 2. STATISTICS & COMPARISON OF REVERSIBLE D FLIP-FLOP OVER VARIOUS OPTIMIZATION PARAMETERS

	Gate Count	Garbage Output	Constant Input	Quantum Cost	Hardware Complexity
Existing Design[10]	11	12	12	47	16α+24β+5δ
Existing Design[11]	4	3	2	12	6α+8β+2δ
Existing Design[12]	5	3	2	13	6α+8β+3δ
Existing Design[13]	1	2	1	8	4α+4β+δ
Proposed Design	***1***	***2***	***1***	***7***	***3α+2β+δ***
IP w.r.t.[10]	91%	83.3%	91.6%	85%	Improved
IP w.r.t.[11]	75%	33.3%	50%	41.6%	Improved
IP w.r.t.[12]	80%	33.3%	50%	46%	Improved
IP w.r.t.[13]	0%	0%	0%	12.5	Improved

TABLE 3. STATISTICS & COMPARISON OF REVERSIBLE R-S FLIP-FLOP OVER VARIOUS OPTIMIZATION PARAMETERS

	Gate Count	Garbage Output	Constant Input	Quantum Cost	Hardware Complexity
Existing Design[5]	9	6	5	33	8α+6β+δ
Existing Design[9]	6	8	6	18	10α+12β+8δ
Proposed Design	***4***	***4***	***2***	***13***	***5α+3β+δ***
IP w.r.t.[5]	55%	33%	60%	60%	Improved
IP w.r.t.[9]	33%	50%	66%	27%	Improved

TABLE 4. STATISTICS & COMPARISON OF REVERSIBLE J-K FLIP-FLOP OVER VARIOUS OPTIMIZATION PARAMETERS

	Gate Count	Garbage Output	Constant Input	Quantum Cost	Hardware Complexity
Existing Design[10]	12	14	13	52	17α+26β+5δ
Existing Design[11]	6	6	4	22	10α+16β+4δ
Existing Design[12]	7	4	3	27	7α+9β+2δ
Proposed Design	***4***	***4***	***2***	***13***	***6α+6β+3δ***
IP w.r.t.[10]	66%	71%	84%	75%	Improved
IP w.r.t.[11]	33%	33%	50%	41%	Improved
IP w.r.t.[12]	42%	0%	33%	51%	Improved

TABLE 5. STATISTICS & COMPARISON OF REVERSIBLE T FLIP-FLOP OVER VARIOUS OPTIMIZATION PARAMETERS

	Gate Count	Garbage Output	Constant Input	Quantum Cost	Hardware Complexity
Existing Design[10]	13	14	14	53	18α+26β+5δ
Existing Design[11]	5	3	2	13	7α+8β+2δ
Existing Design[14]	3	3	2	17	9α+8β+2δ
Proposed Design	***3***	***2***	***2***	***13***	***6α+6β+2δ***
IP w.r.t.[10]	76%	85%	85%	75%	Improved
IP w.r.t.[11]	40%	33%	0%	0%	Improved
IP w.r.t.[14]	0%	33%	0%	23%	Improved

TABLE 6. STATISTICS & COMPARISON OF REVERSIBLE SIPO SHIFT REGISTER OVER VARIOUS OPTIMIZATION PARAMETERS

	Gate Count	Garbage Output	Constant Input	Quantum Cost	Hardware Complexity
Existing Design[13]	7	5	7	35	19α+16β+4δ
Proposed Design	***7***	***5***	***7***	***31***	***15α+8β+4δ***
IP w.r.t.[13]	0%	0%	0%	11%	Improved

TABLE 7. STATISTICS OF REVERSIBLE SHIFT REGISTER COUNTER OVER VARIOUS OPTIMIZATION PARAMETERS

	Gate Count	Garbage Output	Constant Input	Quantum Cost	Hardware Complexity
Proposed Design	***8***	***5***	***8***	***32***	***16α+8β+4δ***

According to the statistics in Table 2 to Table 7, the implementation cost of our designs is lower than designs of all the existing designs in literature.

VII. CONCLUSIONS

In this paper, we have proposed a complete set of reversible sequential elements corresponding to available irreversible sequential designs. Our proposed reversible flip–flop and shift register realization are significantly improved over existing reversible realization in terms of gate count, garbage output, constant input, quantum cost and hardware complexity. We have also proposed low cost shift register counter design using our proposed gate. We have also proposed a quantum realization of our proposed gate. With this implementation, the power consumption of these reversible designs can be controlled and kept significantly low. Our proposed gate is parity preserving. This characteristic of the gate can also be used in fault tolerant sequential circuits designs which is still unexplored area of research.

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