Novel High Speed and Robust Ultra Low Voltage CMOS NP Domino Carry Gate

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***Abstract*—In this paper, a novel design of an Ultra Low voltage Carry Gate shall be presented. The main objective is to target the robustness of the presented ciruits. We shall also imply as to what extent these circuits can be improved and what their benefits, compared to conventional topologies, are. The design presented, compared to a conventional CMOS carry gate, is area efficient and high speed. The relative delay of a ULV carry gate lies at less than 3% compared to conventional CMOS carry gate. The circuits are simulated using the TSMC 90nm process technology and all transistors are of the Low Threshold Voltage (lvt) type.**

***Index Terms*—ULV; Carry Gate; NP domino.**

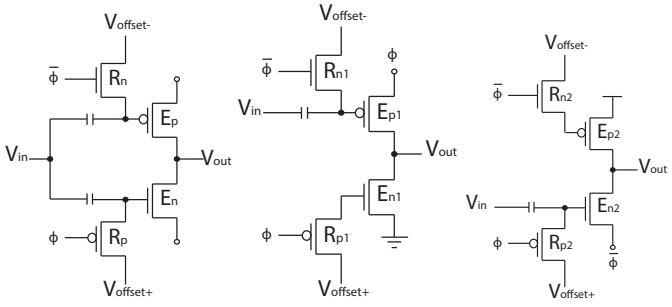
I. INTRODUCTION

As the semiconductor industry grows, the demand for Ultra Low Voltage (ULV) circuits is increasing. These circuits are being implemented in VLSI where different kind of functions are combined on one chip. The Arithmetic Logic Units (ALU)s are one of the many circuits that are implemented in the VLSI chips. Since an adder is an important part of the ALU, the speed of the adder used, is important for the ALU performance. The speed of the adder is determined by the propagation delay of the carry chain. Although high speed conventional carry circuits like Carry Look Ahead, Dual rail domino carry, CPL, etc., are well established design topologies, their performance at ULV suffers from degradation [1]. Several approaches are proposed for the improvement of performance [2][3] but the design presented in this paper is influenced by [4]. This paper shall present a new high speed NP domino ULV carry design. To highlight the improvement, the results shall be compared to conventional domino design such as Dual Rail Domino carry. Both the carry circuits are implemented in a 32-bit carry chain in order to show as to what extent one is better than the other, regarding their speed and power.

Section I-A presents a general introduction to the ULV circuits presented in [5]. Section II presents different configurations of ULV carry designs and gives an explanation on how it works. Section III presents the performance of the proposed ULV carry gate compared to the conventional carry gate.

A. ULV Inverter

1) Evaluation and Precharge Phase: A simple ULV inverter model is presented in the Figure 1a. A ULV Semi-Floating gate circuit design consists of two phases, an evaluation phase, determined by the evaluation transistors E_n and E_p, and a precharge phase determined by the precharge transistors R_n and R_p. As seen in the Figure 1a $\overline{\phi}$ is applied to R_n and



(a) A simple SFG-ULV inverter (b) P-type inverter (c) N-type inverter

Fig. 1. SFG NP ULV domino inverter

ϕ is applied to R_p. In such a circuit, the precharge phase occurs when ϕ=0 and the circuit enters evaluation phase when ϕ=1. During the precharge phase, the input floating nodes are charged to a desired level i.e logical 1 or V_{DD} for the E_n floating gate and logical 0 or Ground (GND) for the E_p floating gate. No input transition occurs during the precharge phase. However, once the clock shifts from logical 0 to 1 and has reached a stable value of 1, an input transition may occur, which determines the logical state of the circuit's output. We can configure the circuit in an NP domino fashion by engaging E_n to $\overline{\phi}$ (where $\overline{\phi}$=1 during the precharge phase) and E_p to V_{DD}. Such a configuration yields a precharge level of logical 1 and is called an N-type circuit. On the other hand, if we engage E_n to GND and E_p to ϕ we can obtain a precharge level of 0. Such a configuration is called a P-type circuit.

Considering the example of N-type inverter, we know that the output of N-type is precharged to 1. Once ϕ shifts from 0 to 1, circuit enters the evaluation phase. During the evaluation phase, there are two possible situations. If no input transition occurs, the output shall remain unchanged and hold its value to 1. Indicating that no work is to be done. However, if an input transition occurs and input is brought to 1 the E_{n2} shall be turned on and the output shall be brought to logical 0 or close to 0. This indicates that the only work to be done during the evaluation phase is to bring the output from 0 to 1 when an input transition occurs.

We have seen that the only work that is to be done, during the evaluation phase, is to bring the output to the logical 0 when an input transition occurs. This suggests that E_{p2} does

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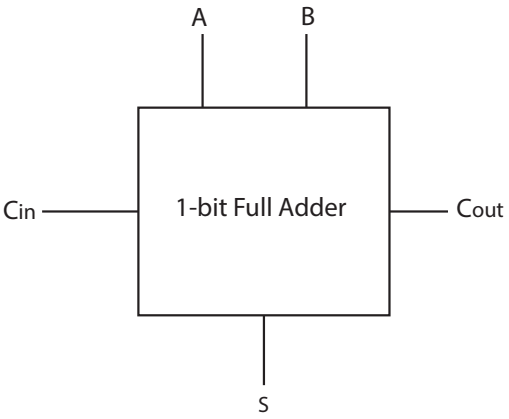


Fig. 2. 1 bit full adder

not require an input transition at any stage. Therefore, we can remove the input capacitor of E_{p2}. Such a configuration can be called pseudo SFG ULV inverter and is shown in Figure 1c. An equivalent P-type Pseudo SFG ULV inverter is shown in Figure 1b. This will lead to load reduction and hence higher speed. However, we may encounter some robustness issues with respect to noise margin due to leakage current.

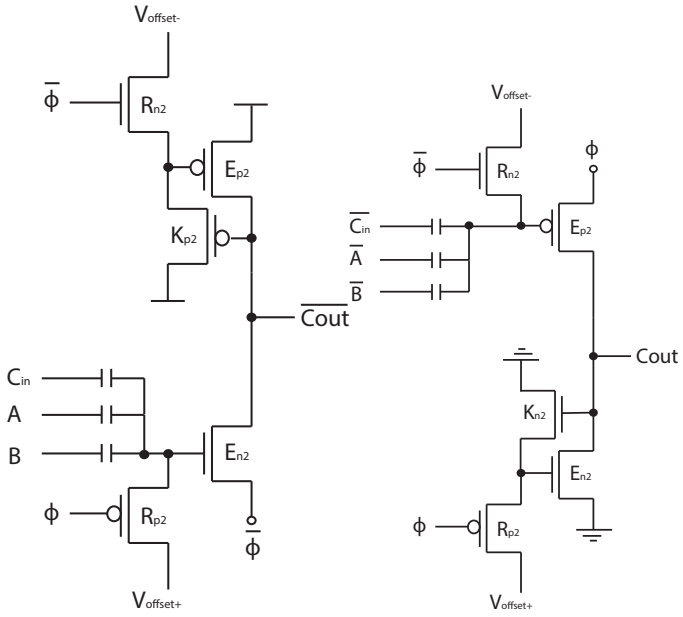
II. Methods

$$C_{out} = A \cdot B + (C_{in} \cdot (A \oplus B)) \quad (1)$$

The output of a carry circuit is generated using two inputs and a carry bit from the previous stage, if available (carry bit at the least signficant bit is always zero so it has no previous carry), as shown in figure 2. Equation (1) shows an arithmetic approach to carry generation where A and B is the input signal and C_{in} is the carry bit from the previous stage. There are two parts of this equation, one is generated internally, $A \cdot B$, and can be called carry generation (CG), the other one is dependent on the carry bit from the previous stage, $(C_{in} \cdot (A \oplus B))$, and is known as carry propagation (CP). The speed of any carry chain depends on the second part of this equation, because it has to wait for the carry bit from the previous stage to arrive. Inputs A and B both arives simultaneously at any stage of an N bit carry chain. Most conventional designs use two seperate parts for CG and CP but the design presented in this paper differ from the most designs as it is able to generate both CG and CP by applying all the inputs to a single transistor. This technique is called Multiple valued Logic (MVL) where classical truth value, logical 1 and 0, are replaced by finit or infinite logical values. It has a potential to decrease the chip area and total power dissipation[6].

A. Non-Differential Carry Gate

The Static Ultra Low Voltage Carry (SULVC) is a modified version of the ULV N-P domino inverter shown in section I-A. The carry circuit uses a keeper as proposed in [5] and



(a) N type SULVC (b) P type SULVC

Fig. 3. SULVC circuit

3 capacitors in parallel at the input gate providing the input logic for the circuit. The circuit is designed to make the A and B signal cancel each other out when A and B have contrasting values to allow the carry input signal to determine the carry output in this case. Because of the cancellation requirement between the A and B signals they need to arrive as equally sized rising or falling transitions, this can be acheived by utilizing level-to-edge converters or a logic style with a VDD/2 precharge level.

If both A and B are rising, the floating node will rise causing a falling transition on the carry output of the N-type circuit regardless of the carry input signal. If they are both falling, the carry input signal can not elevate the floating node voltage enough to cause a transition, leaving the carry output at precharge level. If A and B are not equal, their two transitions cancels each other out and the floating node remains at precharge level until a possible rising edge occurs on Cin. A P-type equivalent of the circuit is shown in Figure 3 (b) where all signals and logic are the inverse of those in the N-type circuit. For both circuits, a transition on the output indicates carry propagation and they can both be characterized as a carry generate circuit corresponding with the truth table shown in Table I, the transition logic for the N-type circuit can be seen in Table II.

During the precharge phase, the voltage level of the floating node is set to ground for the P-type circuit and V_{DD} for the N-type and can only be changed by the inputs through the capacitors in the evaluation phase. In these circuits, when used in CPAs (Carry Propagate Adder), C_{in} can arrive later than A and B when the carry bit has to propagate through the chain of carry circuits. This introduces the challenge of keeping the output precharge value during the evaluation phase in case no

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TABLE I. TRUTH TABLE FOR A CARRY CIRCUIT

Inputs			Output
A	B	C_{in}	C_{out}
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	1

TABLE II. TRANSITION TRUTH TABLE FOR N-TYPE SULVC

Inputs			Output
A	B	C_{in}	$\overline{C_{out}}$
↓	↓	0	1
↓	↑	0	1
↑	↓	0	1
↑	↑	0	↓
↓	↓	↑	1
↓	↑	↑	↓
↑	↓	↑	↓
↑	↑	↑	↓

carry signal arrives. As Figure 4 shows, the floating node of the P-type circuit is precharged to 0V. This causes the transistor E_{p2} in Figure 4 (b) to conduct and the output will drift and may eventually cause an incorrect output value as shown in Figure 5 at 70ns. The drifting effect is countered with the K_{n2} and K_{p2} keeper transistors but the effect limits the length of the evaluation pase and therby the number of carry circuits that can be put in a chain and the maximum number of bits an adder based on the circuit can process in one clock cycle. The maximum achieved number of bits acheived varies with the supply voltage as shown in Figure 6 and at 300mV a 32-bit carry chain can be implemented.

The transistor sizing is adjusted to accommodate the change in NMOS/PMOS mobility difference with changed supply voltage. In these simulations the NMOS evaluation transistor size is kept minimum sized and the PMOS evaluation transistor

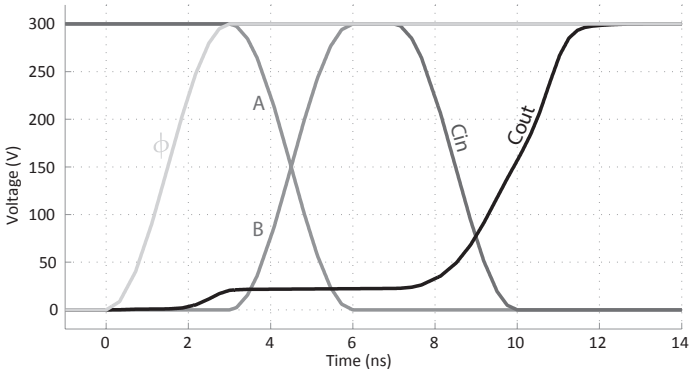


Fig. 4. *Carry input and output for SULVC gate. Supply voltage at 300mV*

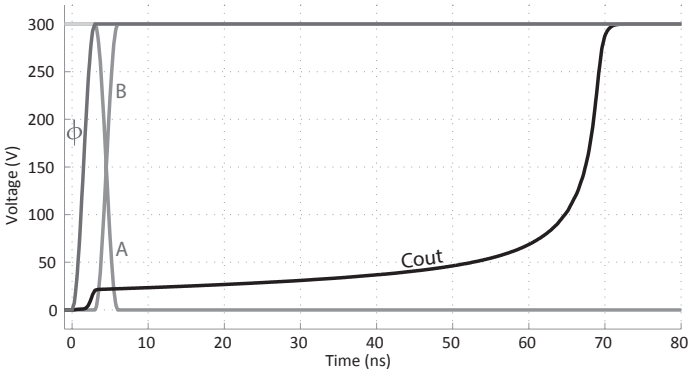


Fig. 5. Drifting problem of the SULVC output.

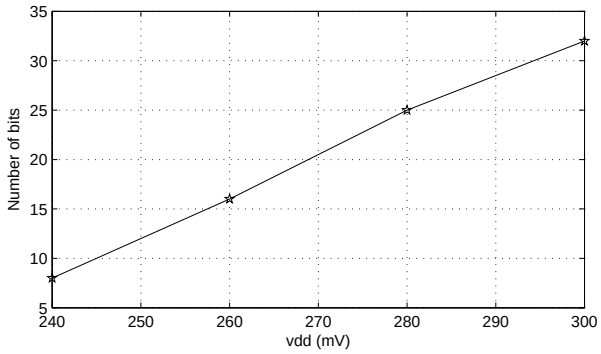


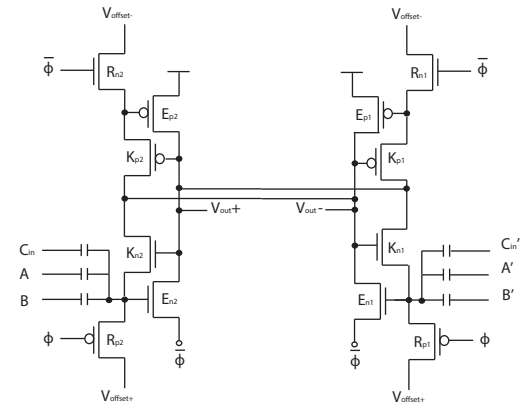
Fig. 6. Number of carry circuits or bit obtained from carry chain when supply voltage is varied

length is changed to match the NMOS drive strength.

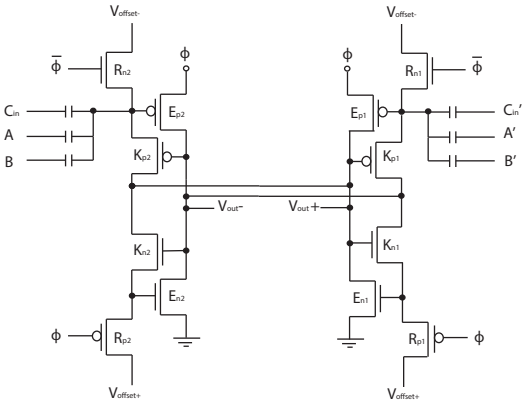
B. Differential Carry Gate

In order to overcome the challenges with robustness and drifting of the SULVC circuit, a differential approach is a possible solution. A Static Differential Ultra Low Voltage Carry (SDULVC) as shown in Figure 7 is designed in exactly the same manner as the SULVC, however with differential inputs and outputs. The differential nature of the circuit makes it less prone to drifting and eliminates the need for level-to-edge converters it can be sized to allow a single edge without causing an output transition. The outputs of the proposed circuit are precharged to the same level during the precharge phase, however it yields a differential output during the evaluation phase. So, instead of employing an inverter to obtain the carry bit we can read it from the opposite end of the circuit, i.e. in an N-type SDULVC if inputs A B and C are applied to E_{n2} output can be read from V_{out-}. Figure 7 demonstrates the design of an SDULVC circuit. The backgate of the keeper transistors of these circuits are connected to the floating gate to achieve maximum robustness.

$$V_{fg} = V_{initial} + k_{in} \cdot V_{in} \text{where } k_{in} = \frac{\sum_{i=1}^{n} C_{innHigh_i}}{C_{total}} \quad (2)$$

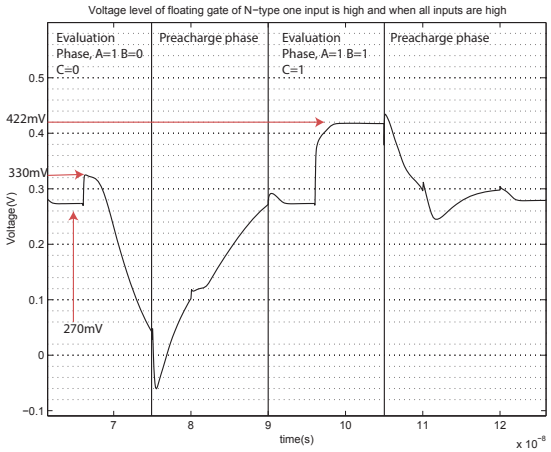


(a) N type SDULVC

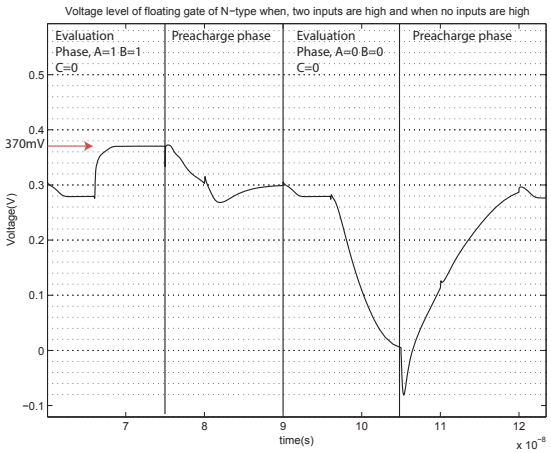


(b) P type SDULVC

Fig. 7. SDULVC circuit



(a) Voltage level of input floating gate of an N-type SDULVC/SDULVC when A=1 B=0 and C=0, and when A=1 B=1 C=1



(b) Voltage level of input floating gate of an N-type SDULVC/SDULVC when A=1 B=1 and C=0, and when A=0 B=0 C=0

Fig. 8. Voltage level of floating gate of N-type at supply voltage of 300mV

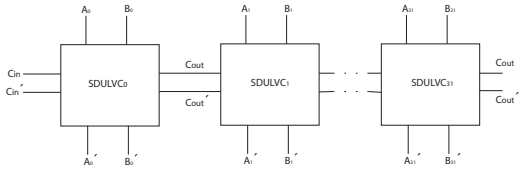


Fig. 9. 32 bit ULV carry chain

The variable 'i' in (2) denotes the index of the input and the 'n' denotes fan-in. $V_{initial}$ is the precharge voltage level of the floating gate. C_{inHigh} is a combination of input capacitors with a high (rising) input.

Considering an example of an N-type SDULVNC we can calculate the voltage level of the floating gate using (2). We assume that the diffusion capacitance is equal to the input capacitance and that the supply voltage is equal to the input voltage. The load capacitance introduced by the keeper's back-gate connection to the floating node should also be considered and is in this paper assumed to be equal to the input capacitor as well.

Our calculation in (2) gives us a theoretical idea of the voltage level at V_{fg} (floating gate voltage). In the real world the capacitance size might not be exactly the same as our assumption and depends on transistor size and many other factors like process variation and mismatch. The simulation results of the voltage levels for the floating gate in the Figure 8 shows that the floating node is precharged to 270mV. Equation (2) yields an analytical result for the floating gate input of 330 mV, 390mV and 450 mV for one, two and three high inputs, respectivly. The simulation results in Figure 8a shows that the voltage level of the floating node gets to 330mV for a single rising input transition and to 420mV when all inputs are high. These results are marginally different from the calculated values. This is possibly due to the assumptions on capacitance sizes. Figure 8a shows that if only one input gets high, the keeper transistor turns on and discharges the floating node. The reason for this is that the transition at the input, i.e. 60mV, is not sufficient to produce enough current at the output. Figure 8b shows the results for two high inputs and all low inputs.

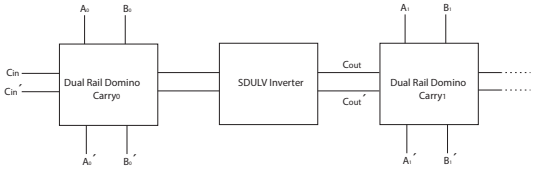
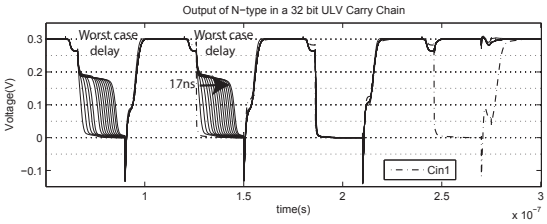
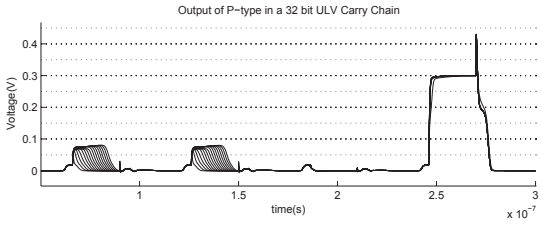


Fig. 10. Implementation of hybrid Dual rail domino carry



(a) output ULV carry chain N-type



(b) output ULV carry chain P-type

Fig. 11. Simulation result of 32 bit ULV carry chain at a supply voltage of 300mv

III. Simulation

A. 32 bit SDULVC chain

A 32 bit ULV carry chain is implemented using 32 SDULVC circuits connected in a chain or NP domino fashion shown in Figure 9. Figure 11 shows the simulation response of a 32 bit ULV carry chain. The propagtion delay of this carry chain is 17ns. In order to compare the SDULVC to other carry gate topologies, a dual rail domino carry gate designed in a hybrid fashion, i.e. instead of utilizing conventional inverters at the output, the Static Differential ULV inverter presented in [7] and a conventional NP Domino Dual Rail carry is used. Compared to the hybrid dual rail domino carry (HDRDC) chain shown in the Figure 10 the SDULVC chain is almost 10× faster and compared to a Conventional Dual Rail Domino Carry (CDRDC) this is closer to 35×. These numbers are based on the propagation delay for the carry bit through the chain, which is 166ns for the hybrid dual rail domino carry and 636ns for the conventional dual rail domino carry, all at 300 mV.

The robustness of the SDULVC can be analyzed by looking at the simulation response shown in Figure 11b. The plot for the worst case delay scenario, i.e. A=1, B=0, C=0, exhibits that due to a delayed carry bit and the early arrival of inputs, A and B, a marginal transition at the output occurs. However, once the carry bit has arrived, the output shifts to its final value. Average transition at the output for a P-type and N-type SDULVC when waiting for the carry bit is between 70mV and 100mV. This can be seen as a problem for the noise margin and power consumption. The output manages to return to the right final value due to synchronisation of keeper signals with the input. Therefore, the issue of noise margin can be ignored by concluding that the final value can be read at the end of the evaluation phase.

TABLE III. DIMENSIONS OF HYBRID DUAL RAIL DOMINO CARRY GATE

	Supply voltage variation	Width of dual rail domino evaluation transitor/Width of SDULVN evaluation transitor	Length of dual rail domino evaluation transitor/Length of SDULVN evaluation transitor	Width of dual rail domino precharge transitor/Width of SDULVN precharge transitor	Length of dual rail domino precharge transitor/Length of SDULVN precharge transitor
Size 1	270mv-400mv	4×	3.3×	1×	1×
Size 2	220mv-400mv	6.67×	8.3×	3.33×	35×

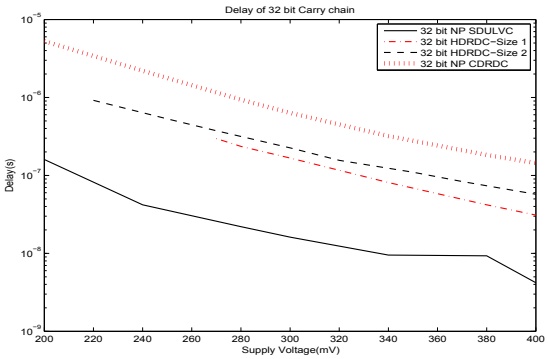


Fig. 12. Delay of 32 bit SDULVC and hybrid dual rail domino at varried supply voltage

Figure 12 shows the delay of an SDULVC chain compared to an HDRDC and a CDRDC chain. Table III shows that the transistor size has to be increased in order to increase the ON current of the device [8] and be able to decrease the supply voltage for HDRDC. Table IV shows the minimum operating frequency required for the clock to simulate SDULVC, HDRDC and CDRDC at different supply voltages.

B. PDP and EDP of SDULVC chain

PDP charachteristics of a circuit highlights its efficiency with respect to power consumtion. A low PDP means a more

TABLE IV. TABLE IV: MINIMUM CLOCK OPERATING FREQUENCY FMIN REQUIRED BY THREE TOPOLOGIES

Supply Voltage (mV)	f_{min} for SDULVC (MHz)	f_{min} for HDRDC-Size 1 (MHz)	f_{min} for HDRDC-Size 2 (MHz)	f_{min} for CDRDC
200	1.6	-	-	0.08
220	-	-	-	-
240	3.125	-	-	0.217
250	-	-	0.83	-
270	-	1.66	1.225	-
280	6.25	-	-	0.5
300	8.33	2.3	2	0.769
320	-	-	2.27	-
340	16.66	5.5	3.33	1.562
380	21	10	5.55	2.5
400	23.8	60	7.692	3.33

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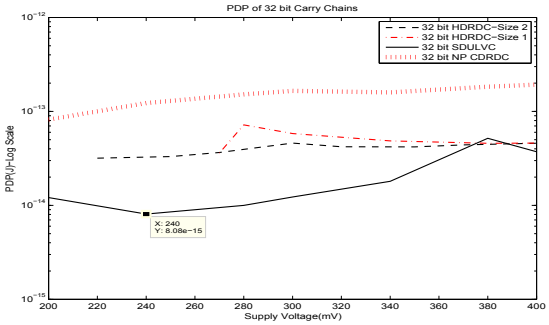

Fig. 13. PDP of 32 bit carry chains

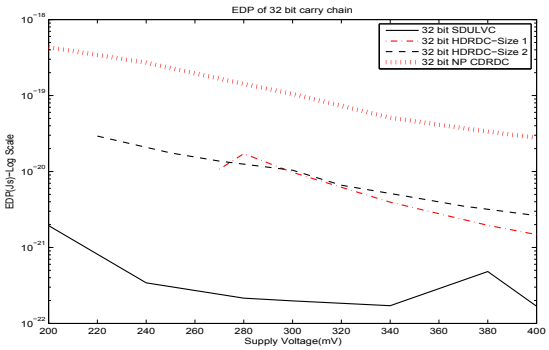

Fig. 14. EDP of 32 bit carry chains

energy efficient circuit. Although the ULV circuits presented in this paper are power hungry, it still manages to maintain its PDP at approximately the same level as conventional circuits where the power consumption is lower. The average power of the HDRDC and the SDULVC is $0.347\mu W$ and $1.28nW$ respectively at a supply voltage of 300 mV. This indicates that the power consumption of HDRDC is up to $3\times$ better than ULV circuits. However, at the same supply voltage the ULV circuit is $10\times$ faster than the HDRDC. Therefore, the ULV circiuts are still more energy efficient. Figure 13 shows PDP of three different 32 bit carry chain topologies at varied supply voltage. The minimum energy point of the 32 bit SDULVC carry chain is found at 240 mV.

Another important charachteristic of any circuit is EDP. It demonstrates enhanced speed of any circuit with respect to its energy effieciency. It is obvious that circuits with better propagation delay shall stand out in this characteristic. Figure 14 shows the EDP of three carry chains and the evident performance advantages of SDULVC circuits.

IV. Conclusion

In this paper, a new ULV carry circuit has been presented and performance enhancements have been demonstrated. The ULV carry circuits are better than conventional topologies in both speed and energy efficiency, shown by comparing the SDULVC to the HDRDC and CDRDC circuit topologies. A credible conclusion is that a static differential dynamic ULV carry circuit is a favorable choice when speed and robustness at low voltages are important.

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