Novel High-Speed and Ultra-Low-Voltage CMOS NAND and NOR Domino Gates

Yngvar Berg
Institute of Microsystems Technology
Vestfold University College
Horten, Norway
Email: Yngvar.Berg@hive.no

Omid Mirmotahari
Department of Informatics
University of Oslo
Oslo, Norway
Email: omidmi@ifi.uio.no

***Abstract*—In this paper we present novel ultra-low-voltage and high-speed CMOS NAND and NOR gates. For supply voltages below $500mV$ the delay for an ultra-low-voltage NAND2 gate is approximately 10% of a complementary CMOS inverter. Furthermore, the delay variations due to mismatch are much lesser than for conventional CMOS. Differential domino gates for AND2/NAND2 and OR2/NOR2 operation are presented. Ultra-low-voltage pass transistors are presented which can be used as latching gates. The ultra-low-voltage gates presented are going to be used for implementation of low-voltage and high speed adders.**

***Keywords*-Low-Voltage, High-Speed, NAND2, NOR2, CMOS, Floating-Gate**

I. INTRODUCTION

The aggressive scaling of device dimensions to achieve greater transistor density and circuit speed results in substantial subthreshold and gate oxide tunneling leakage currents. Energy efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In recent years, the power problem has emerged as one of the fundamental limits facing the future of CMOS integrated circuit design. On one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very-high-speed circuits.

Depending upon the application, there are numerous methods that can be used to reduce the power consumption of VLSI circuits [1], [2], these can range from low-level measures based upon fundamental physics, such as using a lower power supply voltage or using high-threshold voltage transistors; to high-level measures such as clock-gating or power-down modes. The power consumption in digital circuits, which mostly use complementary metal-oxide semiconductor (CMOS) devices, is proportional to the square of the power supply voltage; therefore, voltage scaling is one of the important methods used to reduce power consumption. In order to achieve a high transistor drive current and thereby improve the circuit performance, the transistor threshold voltage V_t must be scaled down in proportion to the supply voltage. However, a decrease in the transistor threshold voltage V_t results in significant increase in the subthreshold leakage current.

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) and Low-Power (LP) logic [3]. However, in modern CMOS technologies there are significant gate leakages which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances, either poly-poly, MOS or metal-metal, to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [3]. There are several approaches to FG CMOS logic [4], [5]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits[5].

In this paper we focus on implementation of low-voltage and high-speed Boolean gates. In section II an extended description of the ULV inverter [6] is given. In section III ULV NOR and NAND gates are presented and ULV latching pass transistors ate described in section IV. Alternative implementations for Boolean gates are presented in section V and a conclusion is given in section VI.

II. ULTRA-LOW-VOLTAGE SEMI-FLOATING-GATE LOGIC

The ULV logic styles presented in this paper are related to the ULV domino logic style presented in [6]. The main purpose of the ULV logic style is to increase the current level for low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra loads represented by the floating capacitors are lesser than extra load given by increased transistor widths. The capacitive inputs lower the delay through increased transconductance while increased transistor widths only reduce parasitic delay.

The simple dynamic edge and level ULV inverters [6] are shown in Figure 1. In order to retain a logic 1 a) when the input remain at logic 0 the width of the pMOS precharge transistor E_p is 4 times the minimum width while the nMOS evaluate transistor has minimum width. The width of the pMOS evaluate transistor in b) is 2 times minimum and the

 ISBN: 978-1-61208-213-4

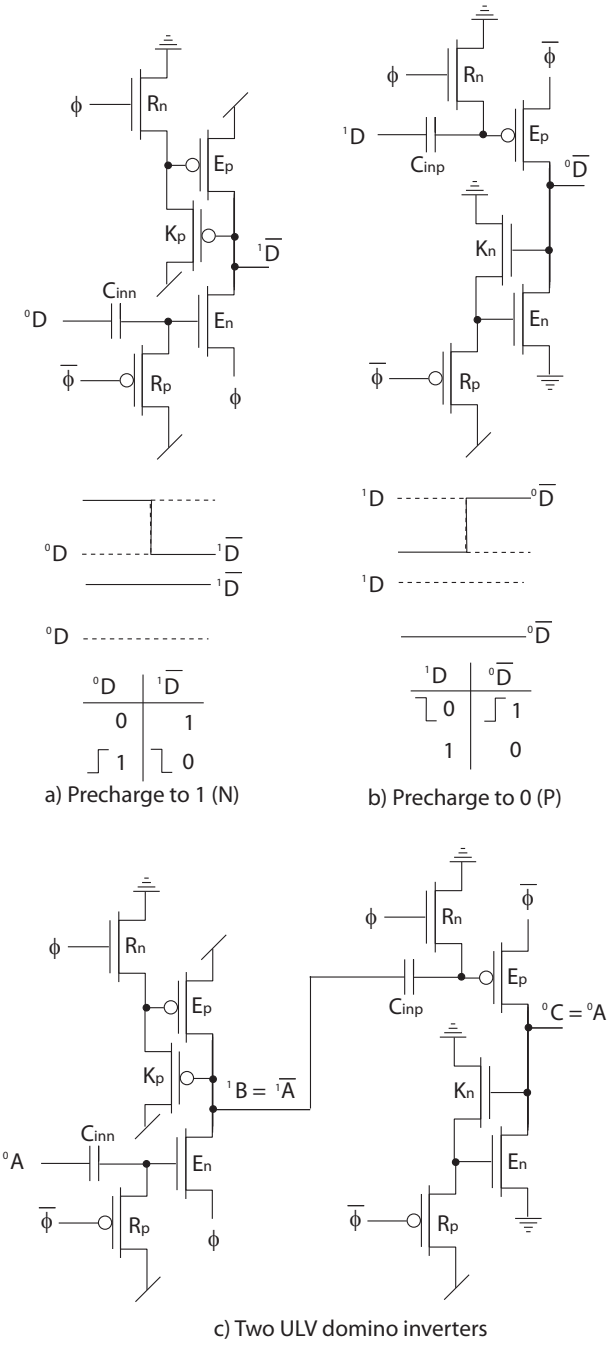

Figure 1. *ULV domino inverters.*

precharge nMOS transistor E_n is also 2 times minimum. The ULV domino gates in this report are ratioed logic and the size of the precharge transistors may be increased to secure required robustness or noise margin. The time constant of a false falling or rising voltage is however always significantly larger than the time constant for an active output edge, i.e. the problem will only be evident in very long domino chains. The recharge and evaluation mode of the ULV logic are

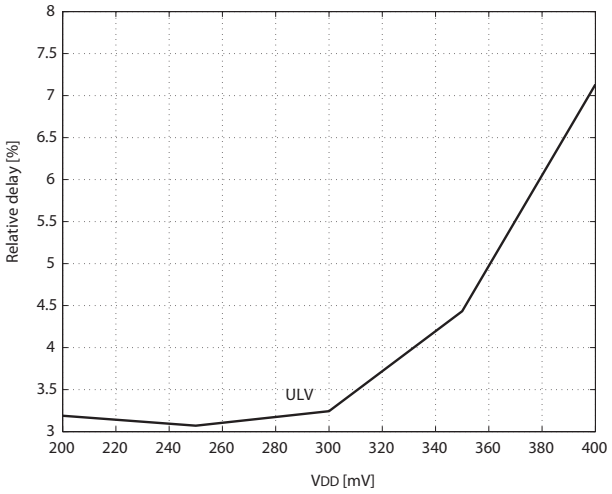

Figure 2. *Delay for ULV logic styles relative to a CMOS inverter.*

characterized by:

- **Recharge.** The precharge and recharge phase starts when ϕ switches from 0 to 1. The recharge transistors, labeled R, are turned ON and will recharge the gate of the evaluating transistors labeled E. More specifically, the gate of the nMOS evaluating transistors will be forced to V_{DD} and the gate of the pMOS evaluating transistors will be recharged to gnd.
- **Precharge.** $\phi = 1$. The output of the inverter in Figure 1 will be driven to V_{DD} or 1 and the inverter in b) will be precharged to 0.
- **Evaluate.** In the evaluation phase, determined by $\phi = 0$, the recharge transistors are turned OFF and the gate of the evaluating transistors are temporarily floating allowing an input transition to affect the current running through the transistors.

The ULV logic styles may be used in critical subcircuits where high-speed and low supply voltage is required. The ULV logic styles may be used together with more conventional CMOS logic. A ULV high speed serial carry chain [7] has been presented using a simple dynamic ULV logic [8]. In this paper we exploit an NP domino ULV static differential logic style.

We define a signal D precharged to 0 as ${}^0D$ and a signal precharged to 1 as ${}^1D$. We Apply a clock signal to power the inverter, i.e. either ϕ to E_n and V_{DD} to E_p, or $\overline{\phi}$ to E_p and GND to E_n and precharge to 1 or 0 respectively. The gate resembles NP, i.e. precharge to 0 and precharge to 1, domino logic. In order to hold the precharged value until an input transition arrives the E transistor connected to a supply voltage is made stronger than the other E transistor. The function of the inverter can be described as ${}^0D \rightarrow \overline{{}^1D}$ and ${}^1D \rightarrow \overline{{}^0D}$.

Relative delays for ULV inverters compared to Standard

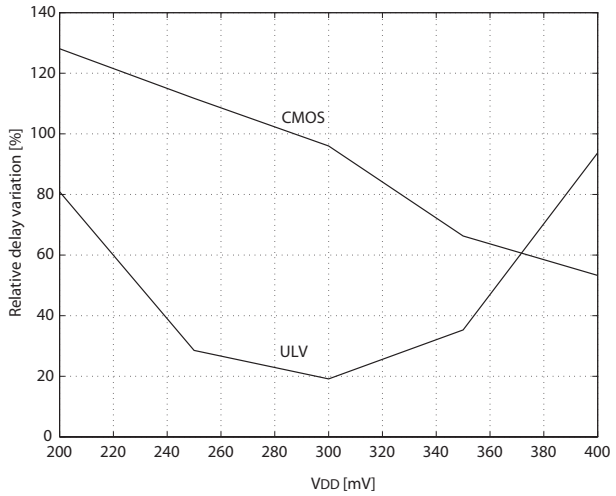

Figure 3. *Delay variation due to process mismatch.*

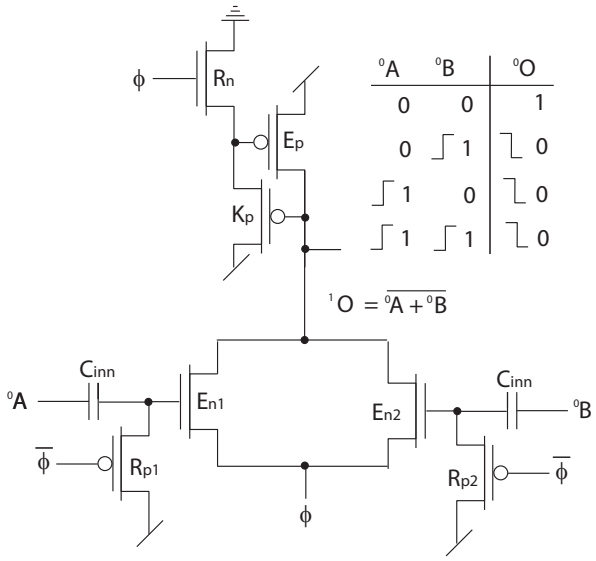

Figure 4. *ULV domino NOR2 gate.*

CMOS inverter are shown in Figure 2. For supply voltages in the region from 200 to 400 the delays of the different ULV logic styles presented are less than 8% of standard CMOS delay. The main target for the logic style presented is $300mV$ which will yield 96% delay reduction compared to standard CMOS. A typical application for the ULV logic styles are low voltage serial adders. For a supply voltage equal to $300mV$ we may apply a 32-bit carry chain using the ULV logic with the same delay as a one-bit standard CMOS carry gate. Delay for different ULV inverters relative to complementary CMOS inverter are shown in Figure 2. The delay improvement is more significant for the proposed ULV inverters than for the original ULV inverters for supply voltages below $320mV$ due to reduced capacitive load.

The ULV logic style is defined by the applied terminal inputs as shown in TABLE I. The ON and OFF currents of a complementary CMOS inverter is given by the effective gate source voltages V_{DD} and $0V$ respectively. Assuming $\frac{Cin}{C_T} = 0.5$ where C_T is the total capacitance seen by a floating gate, we may estimate the delay, dynamic and static power and noise margins of the different ULV logic styles relative to a complementary CMOS inverter.

Monte Carlo simulation is performed including process mismatch and the results in terms of delay variations are shown in Figure 3. For the ULV logic style the mismatch of the clock drivers (standard CMOS inverters) are included. The delay variations of the clock drivers will be equal to the standard CMOS inverters which is significantly larger than the ULV inverters. Hence, the delay variations of the clock drivers will not affect the delay variations significantly.

III. ULV NOR AND NAND GATES

The ULV domino NOR2 gate is shown in Figure 4. The function is defined by $^1O = \overline{^0A + ^0B}$ and reveals a Boolean NOR2 function. The function can be defined in terms of edges and in this context the function is OR2, i.e. for any input edges the output will provide an edge. In order to retain a logic 1 when both inputs remain at logic 0 the width of the pMOS precharge transistor E_p is 8 times the minimum width. The increased width of the precharge transistor and the added parallel evaluate transistor will increase the delay by close to a factor 2 compared to an ULV domino inverter. The worst case scenario is when one and only one of the inputs ^0A or ^0B switches to 1 and the other remains at 0.

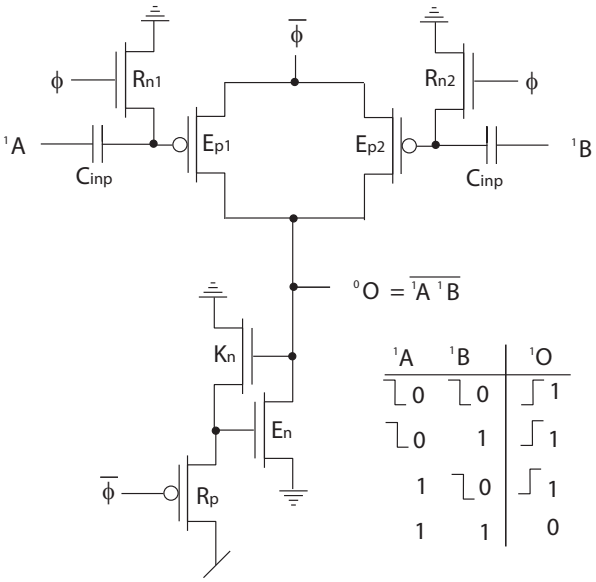

Figure 5. *ULV domino NAND2 gate.*

The ULV domino NAND2 gate is shown in Figure 5. The function is defined by $^0O = \overline{^1A^1B}$ and reveals a Boolean NAND2 function. The function can be defined in terms of

ΔV	E_p	E_n	$V_{gs}\ I_{ON}$	$V_{gs}\ I_{OFF}$	NM'	Relative delay	Comment
V_{DD}	$\overline{\phi}$	GND	$\frac{3V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	$\approx 5\%$	Precharge to 0
$-V_{DD}$	V_{DD}	ϕ	$\frac{3V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	$\approx 5\%$	Precharge to 1

Table I

ULV logic styles. ΔV is the output voltage swing. The simple model for the noise margin NM' is given by the ratio of the ON current and the OFF current given by the effective gate to source voltage. The capacitive division factor, $\frac{Cin}{C_T}$ where C_T is the total capacitance seen by a floating gate is assumed to be 0.5. The delay is relative to a standard complementary CMOS inverter.

edges and in this context the function is OR2, i.e. for any input edges the output will provide an edge.

IV. ULV PASS TRANSISTORS

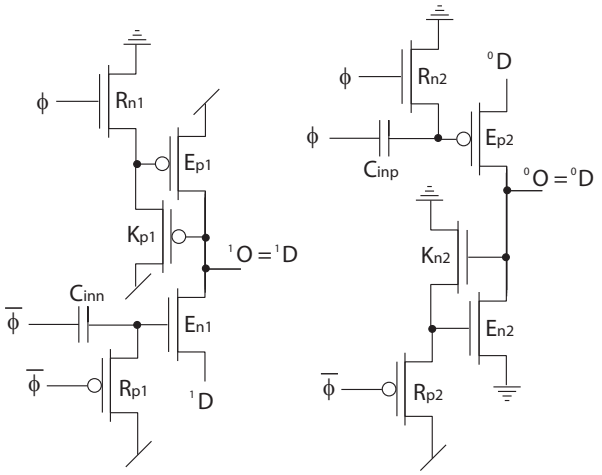

Figure 6. *ULV latching pass transistors.*

Precharge pass transistors are shown in Figure 6. The circuits can be used in ULV latches and Flip-Flops. The evaluate transistors E_{n1} and E_{p2} are powered by the input signals ${}^1D$ and ${}^0D$, and the inputs signals are pushed to the output by the clock (edge) $\overline{\phi}$ and ϕ. The delay from the input to the output of the pass transistor gate is less than for an inverter. By using a combination of the ULV domino inverter and the ULV pass transistor we can implement different Boolean functions.

V. ALTERNATIVE BOOLEAN CIRCUITS

In this section we employ both ULV domino inverters and ULV pass transistors. The Boolean functions are implemented using two ore more stages. Furthermore, the Boolean function of the gates can be defined in terms of standard Boolean logic levels or in terms of signal edges.

By using the evaluate transistor both as an inverting device and a pass transistor as shown in Figure 7 the ULV gates can be used as AND and OR gates. The Boolean function of the OR gate on the left is ${}^1O = {}^1A + {}^1B$. We assume that $\overline{{}^0A}$ is generated by an ULV domino inverter as shown in Figure 1 b). The OR gate provide a Boolean OR function.

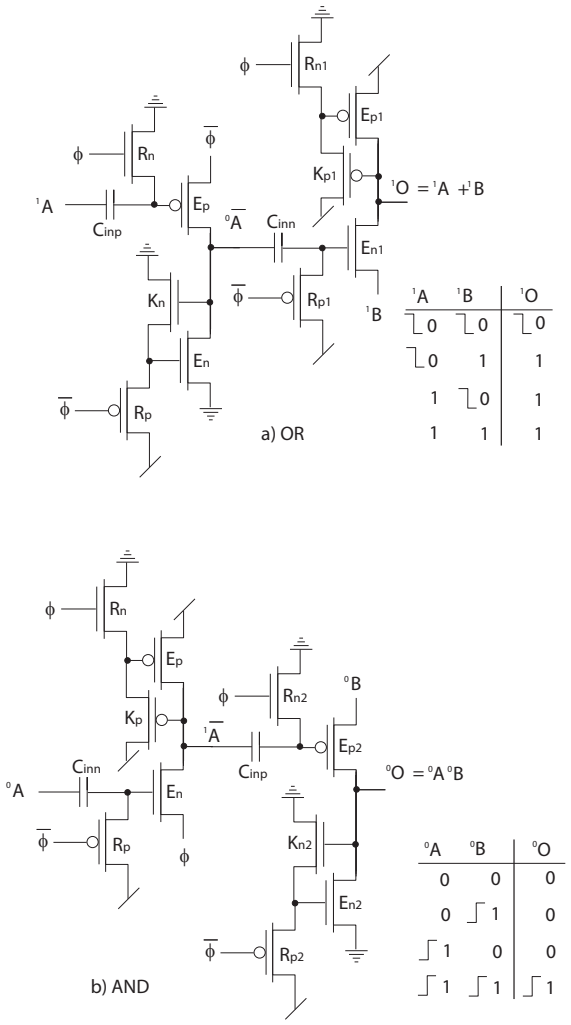

Figure 7. *ULV domino and pass transistor AND2 and OR2 gates.*

The function can also be defined in terms of edges. In this context the function is AND, i.e. an output transition will occur if and only if both input provide edges. For the AND gate on the left the function is given by ${}^0O =^0 A^0B$. In the edge context the function is still AND.

An alternative NOR2 gate is shown in Figure 8 and an alternative NAND2 gate is shown in Figure 9. These gates are slightly different than the previous gates. Both inputs are connected to the gate by floating capacitors which will

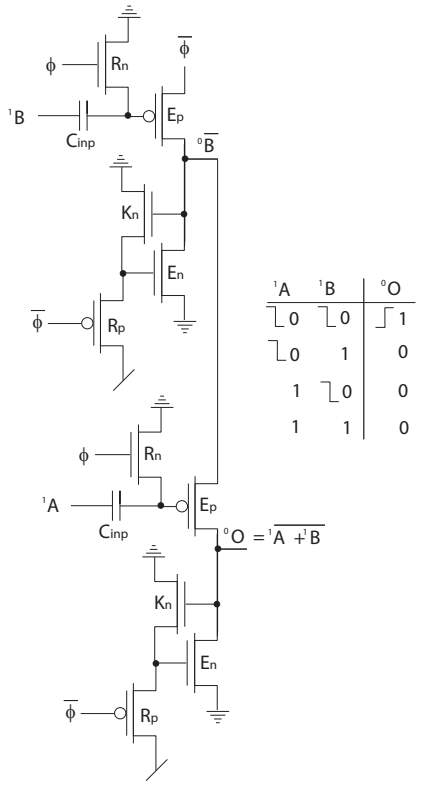

Figure 8. *Alternative ULV domino NOR2 gate.*

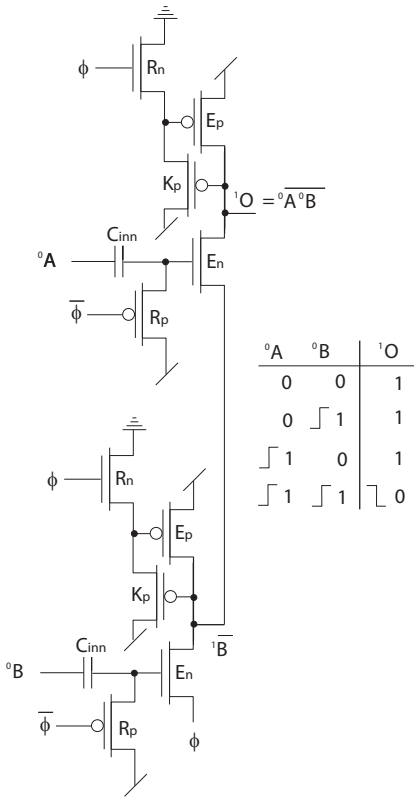

Figure 9. *Alternative ULV domino NAND2 gate.*

Logic style	C_{load}	$delay$	Comment
Figure 1	$8C$	$\approx 4\%$	Inverter
Figure 4	$13C$	$\approx 7\%$	NOR2
Figure 5	$13C$	$\approx 7\%$	NAND2
Figure 6	$7C$	$\approx 3\%$	Pass
Figure 7	$10C + 9C$	$\approx 10\%$	AND2
Figure 8	$7C + 8C$	$\approx 7\%$	NAND2

Table II
Capacitive load and worst case relative delay for a supply voltage equal to $200mV$ (compared to a CMOS inverter). C is equivalent to the gate or parastic diffusion capacitance of a minimum-sized transistor.

prevent draining current from the gates providing the input signals. These gates will be more symmetrical in terms of delay from each input to the output. The delay from the inputs to the output of the gates shown in 7 are different, i.e. the delay from the inputs ${}^0B$ and ${}^1B$ are significantly less than from the ${}^0A$ and ${}^1A$. This asymetrical property is helpful when the delay for the inputs is different due to different signal paths. If the gate is used in a carry chain the carry signal should be provided through a pass transistor as shown in 7.

Capacitive load and relative delay compared to a standard CMOS inverter for the different gates proposed are presented in Table II. The delay of the ULV domino inverter is lesser than 4% compared a CMOS inverter for supply voltages less than $330mV$ as shown in Figure 2. The delay of the ULV pass transistor is less than for the ULV domino inverter. The different implementations of the Boolean gates are equal in terms of delay and close to two times the delay of the ULV domino inverter.

VI. Conclusion

Different ultra-low-voltage domino NAND and NOR gates have been presented. The ULV two-input domino Boolean gates are high-speed, i.e. the delay compared to a CMOS inverter is less than 10%. The delay variation of the ULV gates due to process mismatches is much less than for a CMOS inverter operating at the same supply voltage. The ultra-low-voltage gates presented are going to be used to implement low-voltage and high-speed adders. Preliminary results show that the delay for the ULV NAND2 and NOR2 gates are less than 10% of the delay for a complementary CMOS inverter for ultra low supply voltages.

References

[1] Chandrakasan A.P. Sheng S. Brodersen R.W.: “Low-power CMOS digital design” , *IEEE Journal of Solid-State Circuits*, Volume 27, Issue 4, April 1992 Page(s):473 - 484

[2] Verma N. Kwong J. Chandrakasan A.P.: “Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits” , *IEEE Transactions on Electron Devices*, Vol. 55, NO. 1, January 2008 Page(s):163 - 174

[3] Y. Berg, D. T. Wisland and T. S. Lande: “Ultra Low-Voltage/Low-Power Digital Floating-Gate Circuits”, *IEEE Transactions on Circuits and Systems*, vol. 46, No. 7, pp. 930–936,july 1999.

[4] K. Kotani, T. Shibata, M. Imai and T. Ohmi. “Clocked-Neuron-MOS Logic Circuits Employing Auto-Threshold-Adjustment”, *In IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 320-321,388, 1995.

[5] T. Shibata and T. Ohmi. “ A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations”, *In IEEE Transactions on Electron Devices*, vol 39, 1992.

[6] Y. Berg an O. Mirmotahari: “Ultra Lw-Voltage and High Speed Dynamic and Static Precharge logic”, *In Proc. of the 11th Edition of IEEE Faible Tension Faible Consommation.* June 6-8, 2012, Paris, France.

[7] Y. Berg “Ultra Low Voltage Static Carry Generate Circuit”, *In Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, Paris, may 2010.

[8] Y. Berg: “Static Ultra Low Voltage CMOS Logic”, *In Proc. IEEE NORCHIP Conference*, Trondheim, NORWAY, november 2009.

 ISBN: 978-1-61208-213-4